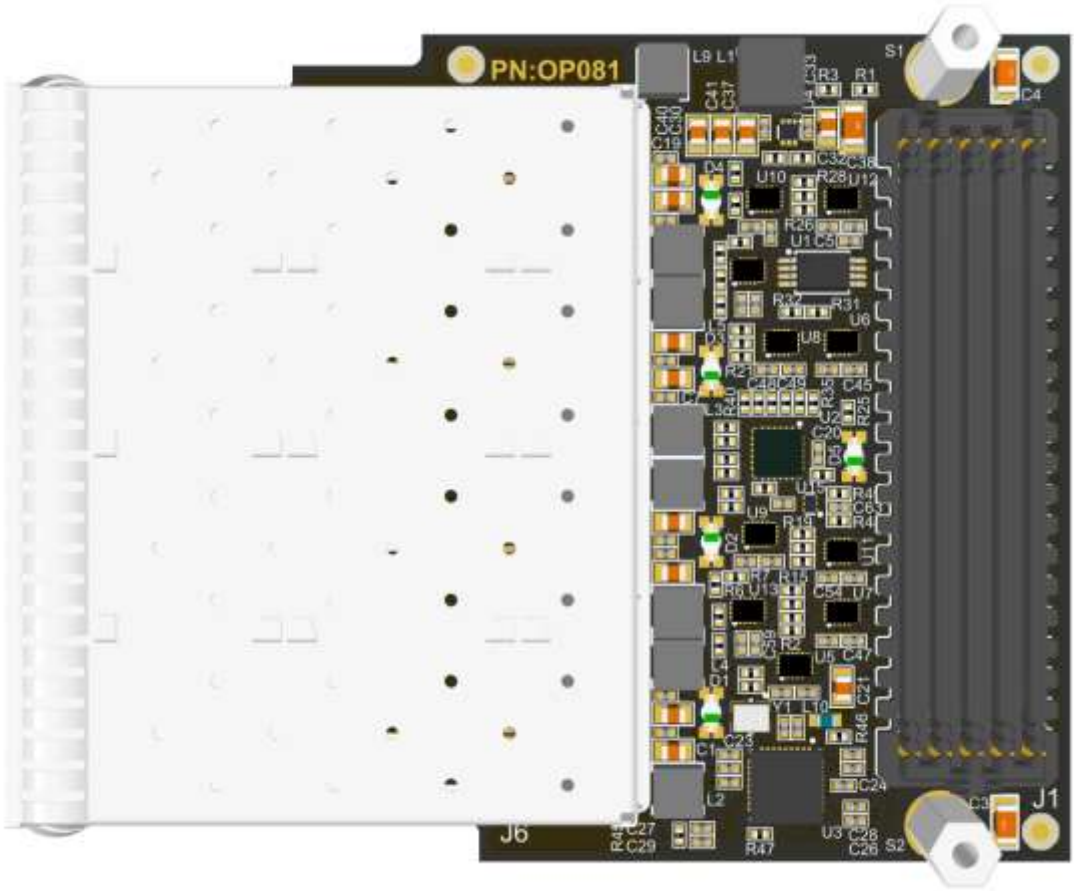
Quad SFP28 FMC

Overview

Description

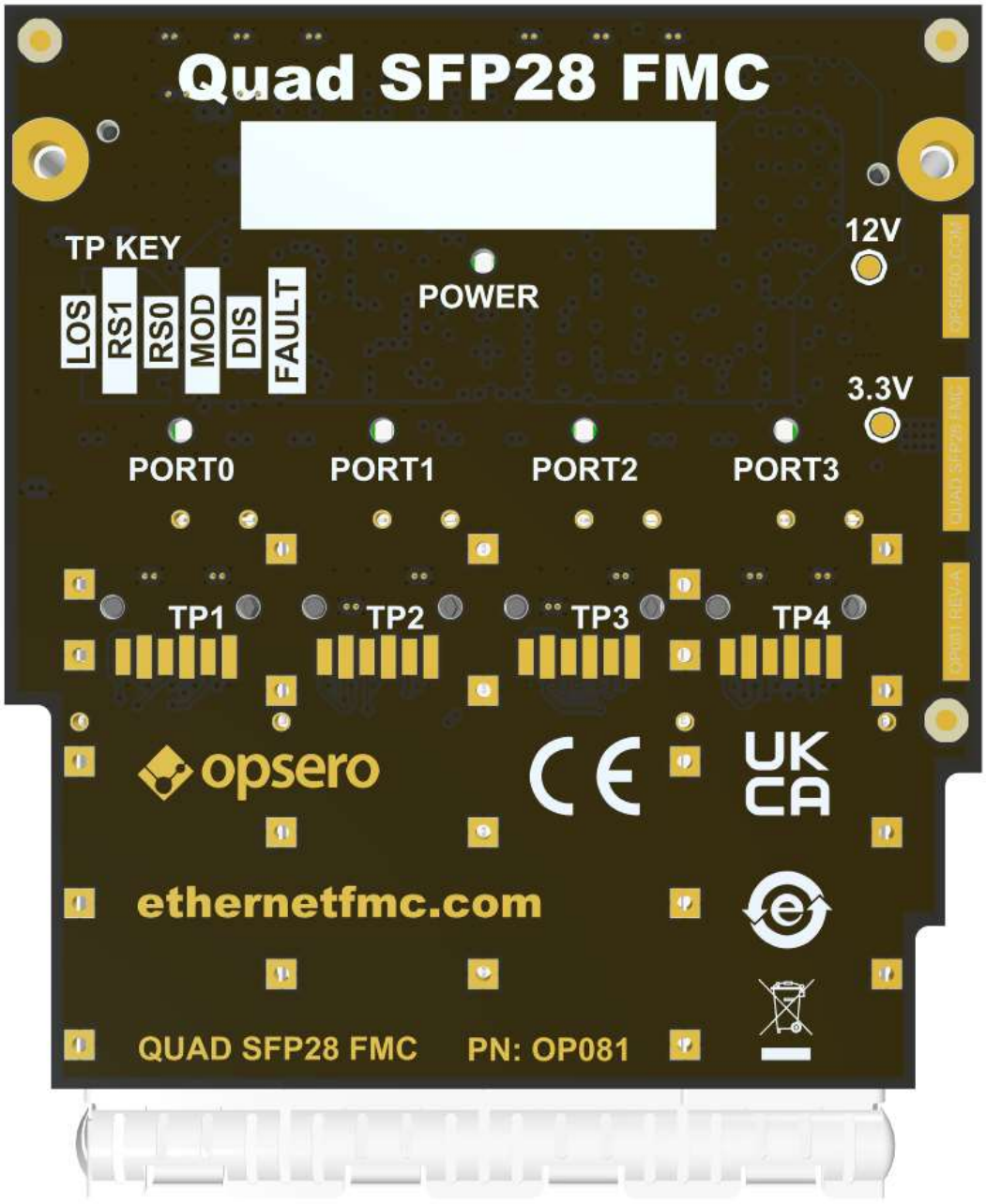
The Quad SFP28 FMC is an add-on expansion board (FPGA Mezzanine Card) for FPGA and SoC-based development boards. It has four SFP28 module slots, allowing the connection of up to four SFP, SFP+ or SFP28 modules to the carrier development board. The mezzanine card features a jitter-attenuating clock multiplier, supporting Synchronous Ethernet applications, and uses level translators to support a wide range of FPGA I/O voltages from 1.2VDC to 3.3VDC.

Top view



Quad SFP28 FMC top

Bottom view



Quad SFP28 FMC bottom

Application Example

Quad SFP28 FMC with ZCU106

Features

- 4x SFP28 slots compatible with SFP, SFP+ and SFP28 modules
- Jitter-attenuating clock multiplier with support for recovered clock and SyncE applications
- Supports a wide range of I/O voltages (VADJ): 1.2V-3.3V
- High pin count FMC connector
- FMC pinout conforms to VITA 57.1 FMC Standard
- Testpoints to aid debugging
- Example designs with sources for several development boards
- Standalone and PetaLinux example designs

Ordering

The Quad SFP28 FMC can be purchased from the following suppliers:

Vendor	Part name	Part number
Opsero	Quad SFP28 FMC	OP081
Digi-Key	Quad SFP28 FMC	OP081

Included with the Quad SFP28 FMC are 2x machine screws for fixing the mezzanine card to the carrier board.

Pin Configuration

Pinout table

The Quad SFP28 FMC has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

Pin	Pin name	Net	Description
A1	GND	GND	Ground
A2	DP1_M2C_P	DP1_M2C_P	Port 1 SFP RX positive
A3	DP1_M2C_N	DP1_M2C_N	Port 1 SFP RX negative
A4	GND	GND	Ground
A5	GND	GND	Ground
A6	DP2_M2C_P	DP2_M2C_P	Port 2 SFP RX positive
A7	DP2_M2C_N	DP2_M2C_N	Port 2 SFP RX negative
A8	GND	GND	Ground
A9	GND	GND	Ground
A10	DP3_M2C_P	DP3_M2C_P	Port 3 SFP RX positive
A11	DP3_M2C_N	DP3_M2C_N	Port 3 SFP RX negative
A12	GND	GND	Ground
A13	GND	GND	Ground

A14	DP4_M2C_P	N/C	Not connected
A15	DP4_M2C_N	N/C	Not connected
A16	GND	GND	Ground
A17	GND	GND	Ground
A18	DP5_M2C_P	N/C	Not connected
A19	DP5_M2C_N	N/C	Not connected
A20	GND	GND	Ground
A21	GND	GND	Ground
A22	DP1_C2M_P	DP1_C2M_P	Port 1 SFP TX positive
A23	DP1_C2M_N	DP1_C2M_N	Port 1 SFP TX negative
A24	GND	GND	Ground
A25	GND	GND	Ground
A26	DP2_C2M_P	DP2_C2M_P	Port 2 SFP TX positive
A27	DP2_C2M_N	DP2_C2M_N	Port 2 SFP TX negative
A28	GND	GND	Ground
A29	GND	GND	Ground
A30	DP3_C2M_P	DP3_C2M_P	Port 3 SFP TX positive
A31	DP3_C2M_N	DP3_C2M_N	Port 3 SFP TX negative
A32	GND	GND	Ground
A33	GND	GND	Ground
A34	DP4_C2M_P	N/C	Not connected
A35	DP4_C2M_N	N/C	Not connected
A36	GND	GND	Ground
A37	GND	GND	Ground

A38	DP5_C2M_P	N/C	Not connected
A39	DP5_C2M_N	N/C	Not connected
A40	GND	GND	Ground
B1	CLK_DIR	N/C	Not connected
B2	GND	GND	Ground
B3	GND	GND	Ground
B4	DP9_M2C_P	N/C	Not connected
B5	DP9_M2C_N	N/C	Not connected
B6	GND	GND	Ground
B7	GND	GND	Ground
B8	DP8_M2C_P	N/C	Not connected
B9	DP8_M2C_N	N/C	Not connected
B10	GND	GND	Ground
B11	GND	GND	Ground
B12	DP7_M2C_P	N/C	Not connected
B13	DP7_M2C_N	N/C	Not connected
B14	GND	GND	Ground
B15	GND	GND	Ground
B16	DP6_M2C_P	N/C	Not connected
B17	DP6_M2C_N	N/C	Not connected
B18	GND	GND	Ground
B19	GND	GND	Ground
B20	GBTCLK1_M2C_P	GBTCLK1_M2C_P	Clock oscillator Si5328 CLKOUT2+ output

B21	GBTCLK1_M2C_N	GBTCLK1_M2C_N	Clock oscillator Si5328 CLKOUT2- output
B22	GND	GND	Ground
B23	GND	GND	Ground
B24	DP9_C2M_P	N/C	Not connected
B25	DP9_C2M_N	N/C	Not connected
B26	GND	GND	Ground
B27	GND	GND	Ground
B28	DP8_C2M_P	N/C	Not connected
B29	DP8_C2M_N	N/C	Not connected
B30	GND	GND	Ground
B31	GND	GND	Ground
B32	DP7_C2M_P	N/C	Not connected
B33	DP7_C2M_N	N/C	Not connected
B34	GND	GND	Ground
B35	GND	GND	Ground
B36	DP6_C2M_P	N/C	Not connected
B37	DP6_C2M_N	N/C	Not connected
B38	GND	GND	Ground
B39	GND	GND	Ground
B40	RES0	N/C	Not connected
C1	GND	GND	Ground
C2	DP0_C2M_P	DP0_C2M_P	Port 0 SFP TX positive
C3	DP0_C2M_N	DP0_C2M_N	Port 0 SFP TX negative
C4	GND	GND	Ground

C5	GND	GND	Ground
C6	DP0_M2C_P	DP0_M2C_P	Port 0 SFP RX positive
C7	DP0_M2C_N	DP0_M2C_N	Port 0 SFP RX negative
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	CLK_LOS_ALARM_T	Not connected
C11	LA06_N	I2C_SW_RST_N_T	Not connected
C12	GND	GND	Ground
C13	GND	GND	Ground
C14	LA10_P	SFP2_RS1_T	Port 2 SFP Rate Select RS1
C15	LA10_N	SFP2_RS0_T	Port 2 SFP Rate Select RS0
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	SFP3_RS1_T	Port 3 SFP Rate Select RS1
C19	LA14_N	SFP3_RS0_T	Port 3 SFP Rate Select RS0
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	SFP3_LOS_T	Port 3 SFP Loss of Signal LOS
C23	LA18_N_CC	SFP3_MOD_ABS_T	Port 3 SFP MOD_ABS
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	N/C	Not connected
C27	LA27_N	N/C	Not connected
C28	GND	GND	Ground

C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)
C35	12P0V_1	12V0	12VDC
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC
C38	GND	GND	Ground
C39	3P3V_1	3V3	Not connected
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	GBTCLK0_M2C_P	Clock oscillator Si5328 CLKOUT1+ output
D5	GBTCLK0_M2C_N	GBTCLK0_M2C_N	Clock oscillator Si5328 CLKOUT1- output
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	SFP0_GRN_LED_T	Port 0 SFP User bicolor LED Green
D9	LA01_N_CC	SFP0_RED_LED_T	Port 0 SFP User bicolor LED Red
D10	GND	GND	Ground

D11	LA05_P	SFP1_GRN_LED_T	Port 1 SFP User bicolor LED Green
D12	LA05_N	SFP1_RED_LED_T	Port 1 SFP User bicolor LED Red
D13	GND	GND	Ground
D14	LA09_P	SFP2_LOS_T	Port 2 SFP Loss of Signal LOS
D15	LA09_N	SFP2_MOD_ABS_T	Port 2 SFP MOD_ABS
D16	GND	GND	Ground
D17	LA13_P	SFP3_GRN_LED_T	Port 3 SFP User bicolor LED Green
D18	LA13_N	SFP3_RED_LED_T	Port 3 SFP User bicolor LED Red
D19	GND	GND	Ground
D20	LA17_P_CC	SFP3_TX_FAULT_T	Port 3 SFP TX fault
D21	LA17_N_CC	SFP3_TX_DISABLE_T	Port 3 SFP TX disable (FPGA to SFP)
D22	GND	GND	Ground
D23	LA23_P	N/C	Not connected
D24	LA23_N	N/C	Not connected
D25	GND	GND	Ground
D26	LA26_P	N/C	Not connected
D27	LA26_N	N/C	Not connected
D28	GND	GND	Ground
D29	TCK	N/C	Not connected
D30	TDI	TDI	Connects to TDO to close JTAG chain

D31	TDO	TDO	Connects to TDI to close JTAG chain
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM
D33	TMS	N/C	Not connected
D34	TRST_L	N/C	Not connected
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC main FMC power supply
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC main FMC power supply
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC main FMC power supply
E1	GND	GND	Ground
E2	HA01_P_CC	N/C	Not connected
E3	HA01_N_CC	N/C	Not connected
E4	GND	GND	Ground
E5	GND	GND	Ground
E6	HA05_P	N/C	Not connected
E7	HA05_P	N/C	Not connected
E8	GND	GND	Ground
E9	HA09_P	N/C	Not connected
E10	HA09_P	N/C	Not connected
E11	GND	GND	Ground
E12	HA13_P	N/C	Not connected
E13	HA13_P	N/C	Not connected

E14	GND	GND	Ground
E15	HA16_P	N/C	Not connected
E16	HA16_P	N/C	Not connected
E17	GND	GND	Ground
E18	HA20_P	N/C	Not connected
E19	HA20_P	N/C	Not connected
E20	GND	GND	Ground
E21	HB03_P	N/C	Not connected
E22	HB03_P	N/C	Not connected
E23	GND	GND	Ground
E24	HB05_P	N/C	Not connected
E25	HB05_P	N/C	Not connected
E26	GND	GND	Ground
E27	HB09_P	N/C	Not connected
E28	HB09_P	N/C	Not connected
E29	GND	GND	Ground
E30	HB13_P	N/C	Not connected
E31	HB13_P	N/C	Not connected
E32	GND	GND	Ground
E33	HB19_P	N/C	Not connected
E34	HB19_P	N/C	Not connected
E35	GND	GND	Ground
E36	HB21_P	N/C	Not connected
E37	HB21_P	N/C	Not connected

E38	GND	GND	Ground
E39	VADJ_1	N/C	Adjustable IO power supply voltage
E40	GND	GND	Ground
F1	PG_M2C	N/C	Not connected
F2	GND	GND	Ground
F3	GND	GND	Ground
F4	HA00_P_CC	N/C	Not connected
F5	HA00_P_CC	N/C	Not connected
F6	GND	GND	Ground
F7	HA04_P	N/C	Not connected
F8	HA04_P	N/C	Not connected
F9	GND	GND	Ground
F10	HA08_P	N/C	Not connected
F11	HA08_P	N/C	Not connected
F12	GND	GND	Ground
F13	HA12_P	N/C	Not connected
F14	HA12_P	N/C	Not connected
F15	GND	GND	Ground
F16	HA15_P	N/C	Not connected
F17	HA15_P	N/C	Not connected
F18	GND	GND	Ground
F19	HA19_P	N/C	Not connected
F20	HA19_P	N/C	Not connected
F21	GND	GND	Ground

F22	HB02_P	N/C	Not connected
F23	HB02_P	N/C	Not connected
F24	GND	GND	Ground
F25	HB04_P	N/C	Not connected
F26	HB04_P	N/C	Not connected
F27	GND	GND	Ground
F28	HB08_P	N/C	Not connected
F29	HB08_P	N/C	Not connected
F30	GND	GND	Ground
F31	HB12_P	N/C	Not connected
F32	HB12_P	N/C	Not connected
F33	GND	GND	Ground
F34	HB16_P	N/C	Not connected
F35	HB16_P	N/C	Not connected
F36	GND	GND	Ground
F37	HB20_P	N/C	Not connected
F38	HB20_P	N/C	Not connected
F39	GND	GND	Ground
F40	VADJ_2	N/C	Adjustable IO power supply voltage
J1	GND	GND	Ground
J2	CLK3_BIDIR_P	N/C	Not connected
J3	CLK3_BIDIR_P	N/C	Not connected
J4	GND	GND	Ground
J5	GND	GND	Ground

J6	HA03_P	N/C	Not connected
J7	HA03_P	N/C	Not connected
J8	GND	GND	Ground
J9	HA07_P	N/C	Not connected
J10	HA07_P	N/C	Not connected
J11	GND	GND	Ground
J12	HA11_P	N/C	Not connected
J13	HA11_P	N/C	Not connected
J14	GND	GND	Ground
J15	HA14_P	N/C	Not connected
J16	HA14_P	N/C	Not connected
J17	GND	GND	Ground
J18	HA18_P	N/C	Not connected
J19	HA18_P	N/C	Not connected
J20	GND	GND	Ground
J21	HA22_P	N/C	Not connected
J22	HA22_P	N/C	Not connected
J23	GND	GND	Ground
J24	HB01_P	N/C	Not connected
J25	HB01_P	N/C	Not connected
J26	GND	GND	Ground
J27	HB07_P	N/C	Not connected
J28	HB07_P	N/C	Not connected
J29	GND	GND	Ground

J30	HB11_P	N/C	Not connected
J31	HB11_P	N/C	Not connected
J32	GND	GND	Ground
J33	HB15_P	N/C	Not connected
J34	HB15_P	N/C	Not connected
J35	GND	GND	Ground
J36	HB18_P	N/C	Not connected
J37	HB18_P	N/C	Not connected
J38	GND	GND	Ground
J39	VIO_B_M2C_1	N/C	Not connected
J40	GND	GND	Ground
K1	VREF_B_M2C	N/C	Not connected
K2	GND	GND	Ground
K3	GND	GND	Ground
K4	CLK2_BIDIR_P	N/C	Not connected
K5	CLK2_BIDIR_P	N/C	Not connected
K6	GND	GND	Ground
K7	HA02_P	N/C	Not connected
K8	HA02_P	N/C	Not connected
K9	GND	GND	Ground
K10	HA06_P	N/C	Not connected
K11	HA06_P	N/C	Not connected
K12	GND	GND	Ground
K13	HA10_P	N/C	Not connected

K14	HA10_P	N/C	Not connected
K15	GND	GND	Ground
K16	HA17_P_CC	N/C	Not connected
K17	HA17_P_CC	N/C	Not connected
K18	GND	GND	Ground
K19	HA21_P	N/C	Not connected
K20	HA21_P	N/C	Not connected
K21	GND	GND	Ground
K22	HA23_P	N/C	Not connected
K23	HA23_P	N/C	Not connected
K24	GND	GND	Ground
K25	HB00_P_CC	N/C	Not connected
K26	HB00_P_CC	N/C	Not connected
K27	GND	GND	Ground
K28	HB06_P_CC	N/C	Not connected
K29	HB06_P_CC	N/C	Not connected
K30	GND	GND	Ground
K31	HB10_P	N/C	Not connected
K32	HB10_P	N/C	Not connected
K33	GND	GND	Ground
K34	HB14_P	N/C	Not connected
K35	HB14_P	N/C	Not connected
K36	GND	GND	Ground
K37	HB17_P_CC	N/C	Not connected

K38	HB17_P_CC	N/C	Not connected
K39	GND	GND	Ground
K40	VIO_B_M2C_2	N/C	Not connected
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not connected
G3	CLK1_M2C_N	N/C	Not connected
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	REC_CLK1_P	Recovered clock positive (LVDS, FPGA to Si5328)
G7	LA00_N_CC	REC_CLK1_N	Recovered clock negative (LVDS, FPGA to Si5328)
G8	GND	GND	Ground
G9	LA03_P	SFP0_TX_FAULT_T	Port 0 SFP TX fault
G10	LA03_N	SFP0_TX_DISABLE_T	Port 0 SFP TX disable (FPGA to SFP)
G11	GND	GND	Ground
G12	LA08_P	SFP1_RS1_T	Port 1 SFP Rate Select RS1
G13	LA08_N	SFP1_RS0_T	Port 1 SFP Rate Select RS0
G14	GND	GND	Ground
G15	LA12_P	SFP1_TX_FAULT_T	Port 1 SFP TX fault
G16	LA12_N	SFP1_TX_DISABLE_T	Port 1 SFP TX disable (FPGA to SFP)
G17	GND	GND	Ground
G18	LA16_P	SFP2_GRN_LED_T	Port 2 SFP User bicolor LED Green

G19	LA16_N	SFP2_RED_LED_T	Port 2 SFP User bicolor LED Red
G20	GND	GND	Ground
G21	LA20_P	N/C	Not connected
G22	LA20_N	N/C	Not connected
G23	GND	GND	Ground
G24	LA22_P	N/C	Not connected
G25	LA22_N	N/C	Not connected
G26	GND	GND	Ground
G27	LA25_P	N/C	Not connected
G28	LA25_N	N/C	Not connected
G29	GND	GND	Ground
G30	LA29_P	N/C	Not connected
G31	LA29_N	N/C	Not connected
G32	GND	GND	Ground
G33	LA31_P	N/C	Not connected
G34	LA31_N	N/C	Not connected
G35	GND	GND	Ground
G36	LA33_P	N/C	Not connected
G37	LA33_N	N/C	Not connected
G38	GND	GND	Ground
G39	VADJ_3	VADJ	Adjustable IO power supply voltage
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not connected

H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	N/C	Not connected
H5	CLK0_M2C_N	N/C	Not connected
H6	GND	GND	Ground
H7	LA02_P	SFP0_RS1_T	Port 0 SFP Rate Select RS1
H8	LA02_N	SFP0_RS0_T	Port 0 SFP Rate Select RS0
H9	GND	GND	Ground
H10	LA04_P	SFP0_LOS_T	Port 0 SFP Loss of Signal LOS
H11	LA04_N	SFP0_MOD_ABS_T	Port 0 SFP MOD_ABS
H12	GND	GND	Ground
H13	LA07_P	SFP1_LOS_T	Port 1 SFP Loss of Signal LOS
H14	LA07_N	SFP1_MOD_ABS_T	Port 1 SFP MOD_ABS
H15	GND	GND	Ground
H16	LA11_P	PL_I2C_SCL_T	PL I2C bus clock SCL
H17	LA11_N	PL_I2C_SDA_T	PL I2C bus data SDA
H18	GND	GND	Ground
H19	LA15_P	SFP2_TX_FAULT_T	Port 2 SFP TX fault
H20	LA15_N	SFP2_TX_DISABLE_T	Port 2 SFP TX disable (FPGA to SFP)
H21	GND	GND	Ground
H22	LA19_P	N/C	Not connected
H23	LA19_N	N/C	Not connected
H24	GND	GND	Ground
H25	LA21_P	N/C	Not connected

H26	LA21_N	N/C	Not connected
H27	GND	GND	Ground
H28	LA24_P	N/C	Not connected
H29	LA24_N	N/C	Not connected
H30	GND	GND	Ground
H31	LA28_P	N/C	Not connected
H32	LA28_N	N/C	Not connected
H33	GND	GND	Ground
H34	LA30_P	N/C	Not connected
H35	LA30_N	N/C	Not connected
H36	GND	GND	Ground
H37	LA32_P	N/C	Not connected
H38	LA32_N	N/C	Not connected
H39	GND	GND	Ground
H40	VADJ_4	VADJ	Adjustable IO power supply voltage

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ (1.2VDC)	+1.14	+1.2	+1.26	V
VADJ (1.5VDC)	+1.425	+1.5	+1.575	V

VADJ (1.8VDC)	+1.71	+1.8	+1.89	V
VADJ (2.5VDC)	+2.375	+2.5	+2.625	V
VADJ (3.3VDC)	+3.135	+3.3	+3.465	V

Notes: * All VADJ pins must be supplied with the same voltage chosen from one of the following levels: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC, +3.3VDC. Note that many carriers have a system controller that will make this choice for you.

Power Consumption

The power consumption of the Quad SFP28 FMC will depend heavily on the SFP+/SFP28 modules being used and the load they are being put under. Power consumption measurements will be added to this section in the near future.

Thermal Information

We have not performed comprehensive thermal testing on the Quad SFP28 FMC, however we recommend that it be operated under ambient temperatures between -40 and 85 degrees C. This advice is based on the recommended ambient operating temperatures of a basket of SFP+/SFP28 modules currently on the market. The active devices on the mezzanine card itself have operating ranges that match or exceed those of typical SFP+/SFP28 modules and are listed in the table below.

DEVICE	MIN	MAX	UNIT
TI, 5A Synchronous Buck Converter, TPS565247DRLR	-40	150	C
TI, I2C Level translator, TCA9416DTMR	-40	125	C
ST, 2K EEPROM, M24C02-FDW6TP	-40	85	C
Skyworks, SyncE Jitter-Attenuating Clock Multiplier, SI5328B-C-GM	-40	85	C
TI, 8-channel I2C Switch with Reset, PCA9548ARGER	-40	85	C
TI, Voltage Translator, SN74AVC4T245RSVR	-40	85	C
Abracon, 114.285MHz Crystal, ABM8-166-114.285MHZ-T2	-40	85	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -40 degrees C, and maximum operating temperature that is greater than 85 degrees C.

I2C (EEPROM) Timing

The serial EEPROM (part number ST, 2K EEPROM, M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz (Fast-mode).

I2C (PL) Timing

The PL I2C bus passes through level translator (TCA9416) and I2C switch (PCA9548). Together they support an I2C clock frequency up to 400kHz (Fast-mode).

Device	Standard-mode 100kHz	Fast-mode 400kHz	Fast-mode Plus 1MHz
Level translator TCA9416	✔	✔	✔
Switch PCA9548	✔	✔	✘

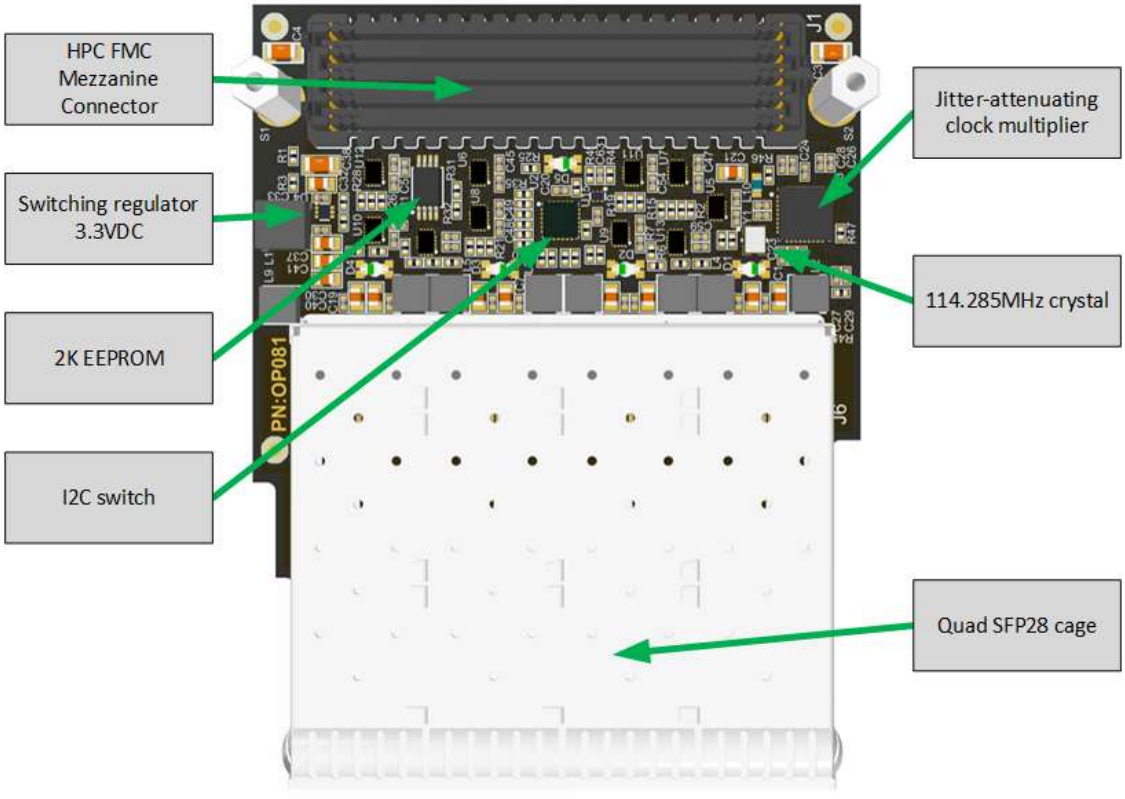
Certifications

- RoHS
- CE

Detailed Description

Hardware Overview

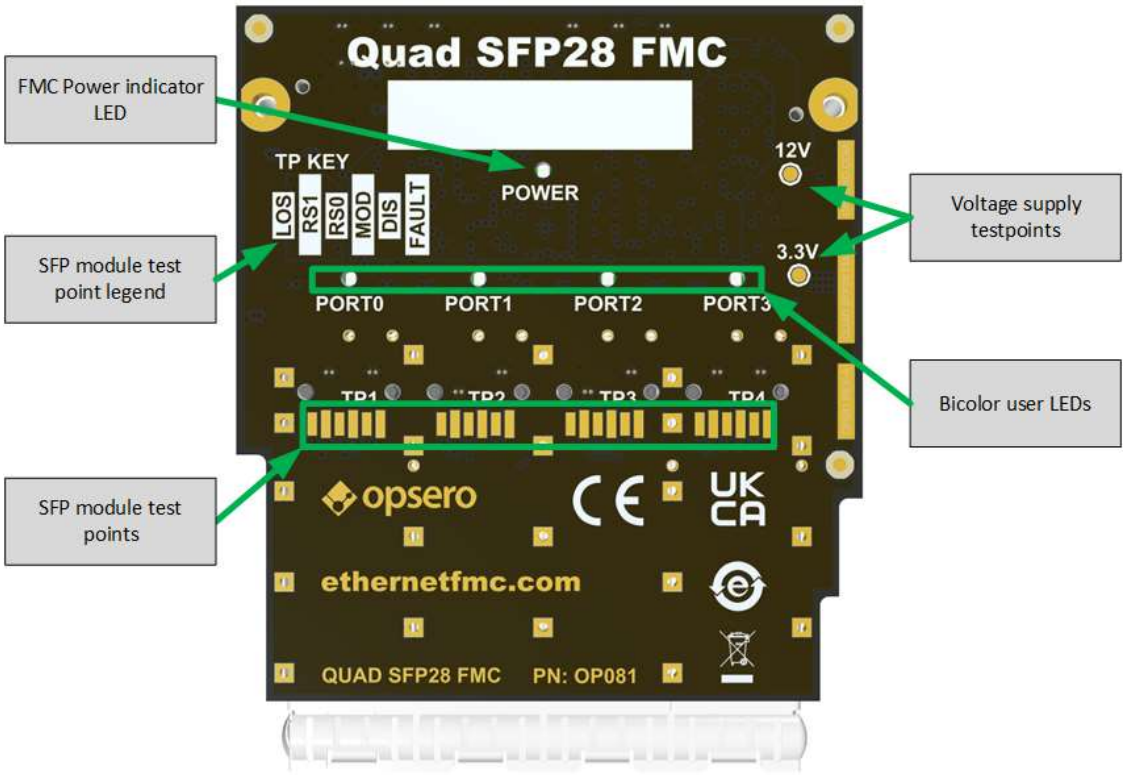
The figure below illustrates the various hardware components that are located on the top-side (component side) of the Quad SFP28 FMC.



The main components on the top-side of the mezzanine card are:

- Quad SFP28 cage
- High Pin Count FMC Connector
- 2K EEPROM
- Jitter-attenuating clock multiplier (Si5328)
- 114.285MHz crystal
- I2C switch
- Level translators
- 3.3VDC switching buck regulator

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



The main components on the bottom-side of the mezzanine card are:

- Bicolor user LEDs
- FMC Power indicator LED
- Test points for 12VDC and 3.3VDC power supplies
- Test points for SFP module I/Os
- Key/legend for SFP I/O test points

Quad SFP28 Cage

The SFP28 cage (Link-PP, SFP28 Quad Cage, LP14CC01000S) can accommodate 4x SFP, SFP+ or SFP28 modules.

Jitter-attenuating Clock Multiplier

The Quad SFP28 FMC features a jitter-attenuating clock multiplier (Skyworks, Si5328), which generates two precision clocks with selectable frequencies ranging from 8kHz to 808MHz. Its wide frequency range and exceptional jitter performance support a variety of applications, including Synchronous Ethernet.

The Si5328 utilizes a 114.285MHz crystal and oscillator circuit to generate frequencies between 8kHz and 808MHz. The clock multiplication ratio can be programmed through an I2C interface. The device also has a clock input, connected to FPGA I/O pins (LA00_CC_P/N), which can receive a recovered clock from the FPGA gigabit transceivers. In Synchronous Ethernet applications, jitter attenuation can be applied to the recovered clock, which can then be directed to the clock outputs to drive the gigabit transceivers.

See the Clocks section for more information on the clock system.

EEPROM

The 2K EEPROM stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

High Pin Count FMC Connector

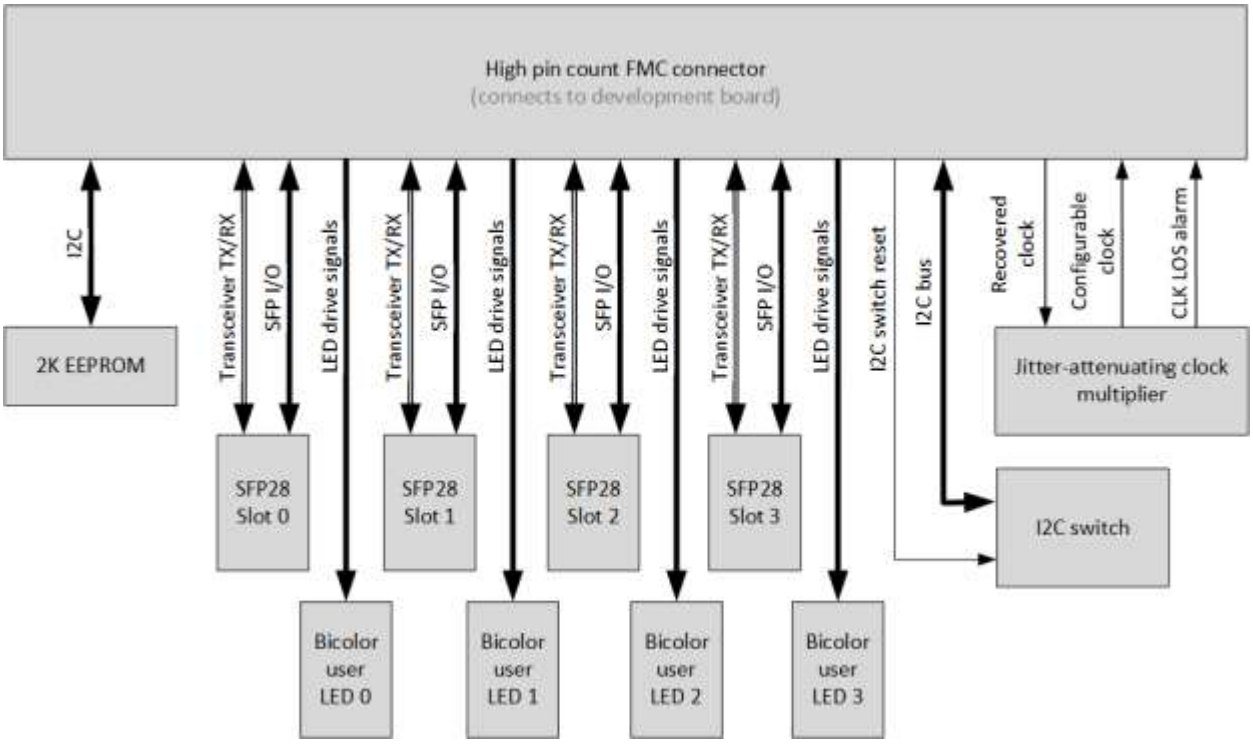
The Quad SFP28 FMC has a low pin count FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, Mezzanine-side High pin count FMC Connector, ASP-134488-01 . The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard. For the pinout details, see the Pin configuration section. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

I/O Interfaces

The FMC connector provides power to the Quad SFP28 FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- Gigabit serial links for the 4x SFP28 slots
- SFP I/O signals (FAULT, TX_DISABLE, MOD, RS0/1, LOS) for the 4x SFP28 slots
- I2C for IPMI EEPROM
- I2C (PL) for SFP28 slots and clock multiplier via an I2C switch
- LVDS recovered clock from the FPGA to drive the clock multiplier
- LVDS configurable clock from the clock multiplier
- Clock loss alarm from the clock multiplier
- Drive signals for the 4x bicolor user LEDs
- Reset signal for the I2C switch

The figure below illustrates the connections to the FMC connector.



The I2C connections from the I2C switch to the slave devices has been left out of the above diagram for clarity. Details on the I2C connections can be found in the I2C Buses section.

The level translators have been left out of the above diagram for clarity. Details can be found in the Level translation section.

Level translation

To support a wide range of I/O voltages (VADJ), the Quad SFP28 FMC uses level translators for the SFP I/O signals, the PL I2C bus signals, the I2C switch reset signal, the LED drive signals and the clock loss alarm signal. The table below lists the devices used:

Device	Purpose
TCA9416	Level translation of the PL I2C bus.
SN74AVC4T245RSVR	Level translation of SFP I/Os, I2C switch reset signal, LED drive signals and clock loss alarm.

The gigabit serial links of the SFP28 slots and the reference clocks connect to the gigabit transceivers, which are independent of the VADJ voltage and do not need voltage translation. The recovered clock signal (REC_CLK1_P/N) should be configured as an LVDS output in the FPGA and also does not require voltage translation.

Gigabit transceivers

The data channel between the SFP, SFP+, and SFP28 modules and the FPGA operates over serial gigabit links at speeds of up to 25 Gbps. The Quad SFP28 FMC connects these serial links to gigabit transceivers in the FPGA or SoC on the development board. Each serial link consists of two differential pairs: one for transmission and one for reception. These serial links connect to the first four gigabit transceivers on the FMC connector (DP0-3).

SFP28 Slot	Signal direction	FMC gigabit transceiver
0	FPGA to link partner	DP0_C2M_P/N
	Link partner to FPGA	DP0_M2C_P/N
1	FPGA to link partner	DP1_C2M_P/N
	Link partner to FPGA	DP1_M2C_P/N
2	FPGA to link partner	DP2_C2M_P/N
	Link partner to FPGA	DP2_M2C_P/N
3	FPGA to link partner	DP3_C2M_P/N
	Link partner to FPGA	DP3_M2C_P/N

As the serial links connect to gigabit transceivers, they are independent of the VADJ voltage being used and do not need voltage translation.

SFP I/O Signals

In addition to the high-speed serial link, SFP modules have several I/O signals used for configuration and fault indication. On the Quad SFP28 FMC, these I/O signals are connected through level translators to the FPGA I/O, allowing the FPGA to control and read them. The I/O signals and their functionality are listed in the table below:

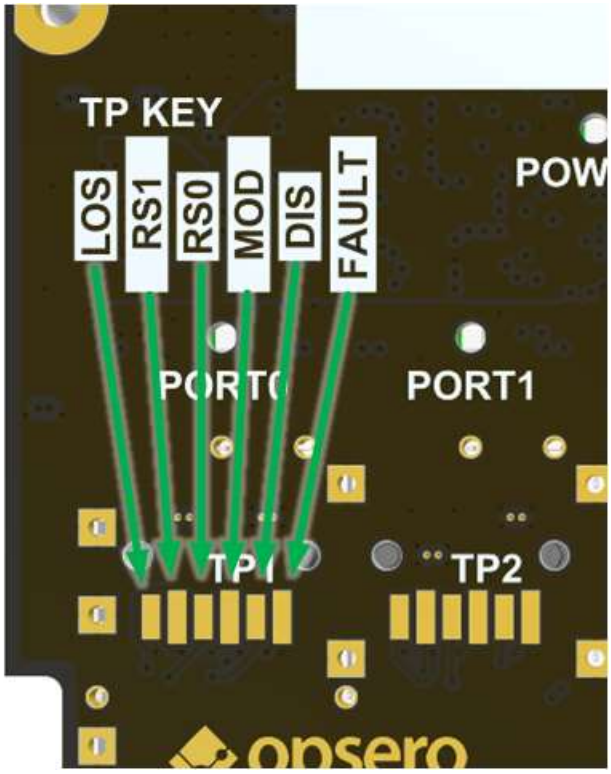
SFP pin	Name	Direction	Function
2	TX_FAULT	SFP to FPGA	Indicates transmitter fault
3	TX_DISABLE	FPGA to SFP	Disables optical output
6	MOD_ABS	SFP to FPGA	Indicates module absence
7	RS0	FPGA to SFP	Rate select 0
8	RX_LOS	SFP to FPGA	Indicates receiver loss of signal
9	RS1	FPGA to SFP	Rate select 1

The SFP I/O signals connect to the FMC pins listed in the table below:

Slot	Net Name	FMC pin
0	SFP0_TX_DISABLE_T	LA03_P
	SFP0_TX_FAULT_T	LA03_N
	SFP0_LOS_T	LA04_P
	SFP0_MOD_ABS_T	LA04_N
	SFP0_RS1_T	LA02_P
	SFP0_RS0_T	LA02_N
1	SFP1_TX_DISABLE_T	LA12_P
	SFP1_TX_FAULT_T	LA12_N
	SFP1_LOS_T	LA07_P
	SFP1_MOD_ABS_T	LA07_N

	SFP1_RS1_T	LA08_P
	SFP1_RS0_T	LA08_N
2	SFP2_TX_FAULT_T	LA15_P
	SFP2_TX_DISABLE_T	LA15_N
	SFP2_LOS_T	LA09_P
	SFP2_MOD_ABS_T	LA09_N
	SFP2_RS1_T	LA10_P
	SFP2_RS0_T	LA10_N
3	SFP3_TX_FAULT_T	LA17_CC_P
	SFP3_TX_DISABLE_T	LA17_CC_N
	SFP3_LOS_T	LA18_CC_P
	SFP3_MOD_ABS_T	LA18_CC_N
	SFP3_RS1_T	LA14_P
	SFP3_RS0_T	LA14_N

All of the SFP I/O signals are brought out to rectangular test points as a debugging aid. These test points are accessible on the bottom side of the mezzanine card and are illustrated in the bottom labelled image above. For identifying the SFP I/O signals, a key/legend is displayed on the bottom side of the mezzanine card. The signal names in the legend correspond to the test points below them, arranged in the same order and orientation as the legend. Each SFP28 slot has its own set of test points corresponding to these signals. The image below illustrates the matching between the signal names in the key and the test points for slot 0.



I2C Buses

The Quad SFP28 FMC has two independent I2C buses: the FMC's dedicated I2C bus for the IPMI EEPROM and the PL (programmable logic) I2C bus that connects to all other I2C devices.

EEPROM I2C

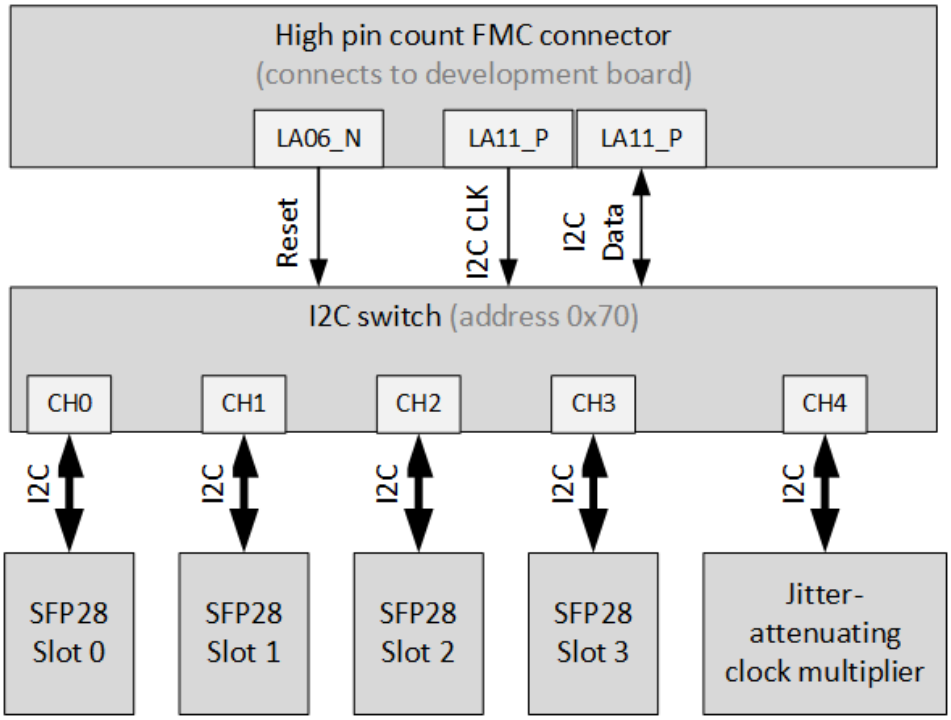
A 2K EEPROM is located on the FMC card's dedicated I2C bus. The FMC pins of the I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM or I/O expander, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

PL I2C

The main I2C bus of the Quad SFP28 FMC is implemented using two FPGA I/O pins (LA11_P/N) and enables communication between the FPGA, the four SFP28 modules, and the clock multiplier. To avoid I2C address conflicts, an I2C switch (TI, 8-channel I2C Switch with Reset, PCA9548ARGER) is used to connect these devices, as identical SFP28 modules may share the same address. The diagram below illustrates the I2C bus connections through the I2C switch:



I2C bus connections

The I2C switch is wired to have I2C address 0x70, and it can be configured to target one of the lower slave devices by specifying the appropriate channel (0-4). The connected slave devices and their channels are listed in the table below:

I2C Device	Switch channel	Device I2C address
SFP28 Slot 0	0	Module dependent
SFP28 Slot 1	1	Module dependent
SFP28 Slot 2	2	Module dependent
SFP28 Slot 3	3	Module dependent

Clock multiplier	4	0x68

Note that the I2C address of the SFP28 slots will depend on the SFP/SFP+/SFP28 module that is connected to the slot. Refer to the module datasheet for the I2C address and register details.

The I2C bus signals are connected to the FMC pins listed in the table below:

Net Name	Description	FMC pin
PL_I2C_SCL_T	I2C clock (SCL)	LA11_P
PL_I2C_SDA_T	I2C data (SDA)	LA11_N

The PL I2C bus signals pass through a level translator to convert the FPGA I/O levels (VADJ) to 3.3VDC levels.

Clock signals

Refer to the Clocks section for more information about the clock related signals and how they connect to the jitter-attenuating clock multiplier.

Bicolor User LEDs

The Quad SFP28 FMC features four bicolor (green/red) LEDs, one for each SFP28 slot, which can be driven by the FPGA and are visible on the bottom side of the mezzanine card. These LEDs provide the user or developer with programmable visible outputs that can be linked to specific signals for monitoring. Examples of such signals for monitoring include the SFP I/Os (FAULT, TX_DISABLE, MOD, RS0/1, LOS) or other SFP module-specific indicators.

The drive pins for the user LEDs are routed through level translators to convert the FPGA I/O signal levels (VADJ) to 3.3VDC levels for driving the LEDs. The level translators have sufficient output current capacity to drive the LEDs directly.

The bicolor user LEDs connect to the FMC pins listed in the table below:

Aligned with slot	Net Name	FMC pin
0	SFP0_GRN_LED_T	LA01_CC_P
	SFP0_RED_LED_T	LA01_CC_N
1	SFP1_GRN_LED_T	LA05_P
	SFP1_RED_LED_T	LA05_N

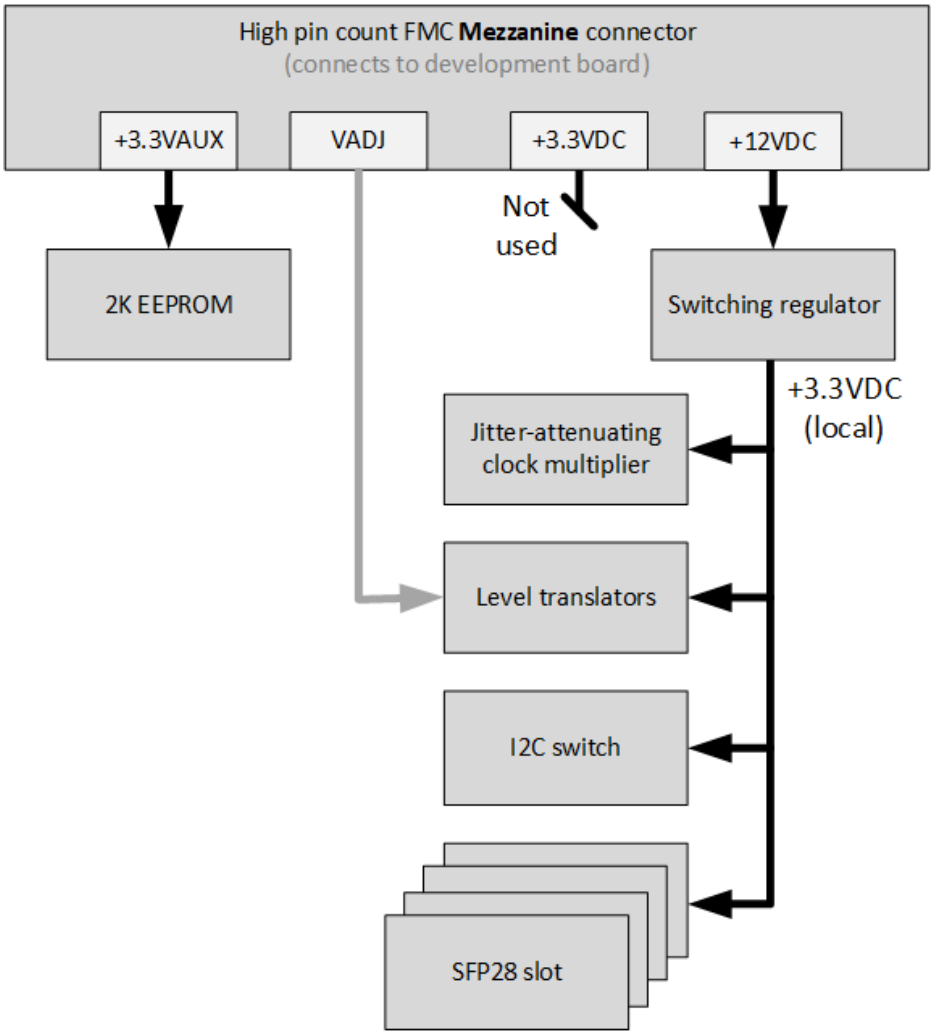
2	SFP2_GRN_LED_T	LA16_P
	SFP2_RED_LED_T	LA16_N
3	SFP3_GRN_LED_T	LA13_P
	SFP3_RED_LED_T	LA13_N

Note that when the green and red signals for a single LED are asserted at the same time, the resulting color is amber.

Power Supplies

All power required by the Quad SFP28 FMC is supplied by the development board through the FMC connector:

- +12VDC
- VADJ: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC or +3.3VDC
- +3.3VAUX



Power supplies

The FPGA/MPSoC carrier board also supplies a 3.3VDC power supply, however this supply is not used by the Quad SFP28 FMC.

12VDC Supply

The 12VDC supply is the main power source for the mezzanine card. It feeds a buck switching regulator (TI, 5A Synchronous Buck Converter, TPS565247DRLR) that generates 3.3VDC to power to all four SFP28 slots, the clock multiplier, the I2C switch and the level translators.

VADJ Supply

The VADJ supply is the FPGA I/O power supply and it determines the voltage levels of the FMC I/Os. On the Quad SFP28 FMC, the VADJ supply powers the level translators that allow the board to be used at any I/O voltage in the range of 1.2VDC to 3.3VDC.

3.3VAUX Supply

The 3.3VAUX supply is used to power the IPMI EEPROM and is independent of the main 3.3VDC supply so that the carrier board can read from the EEPROM without having to power up the entire board.

Power LED and testpoints

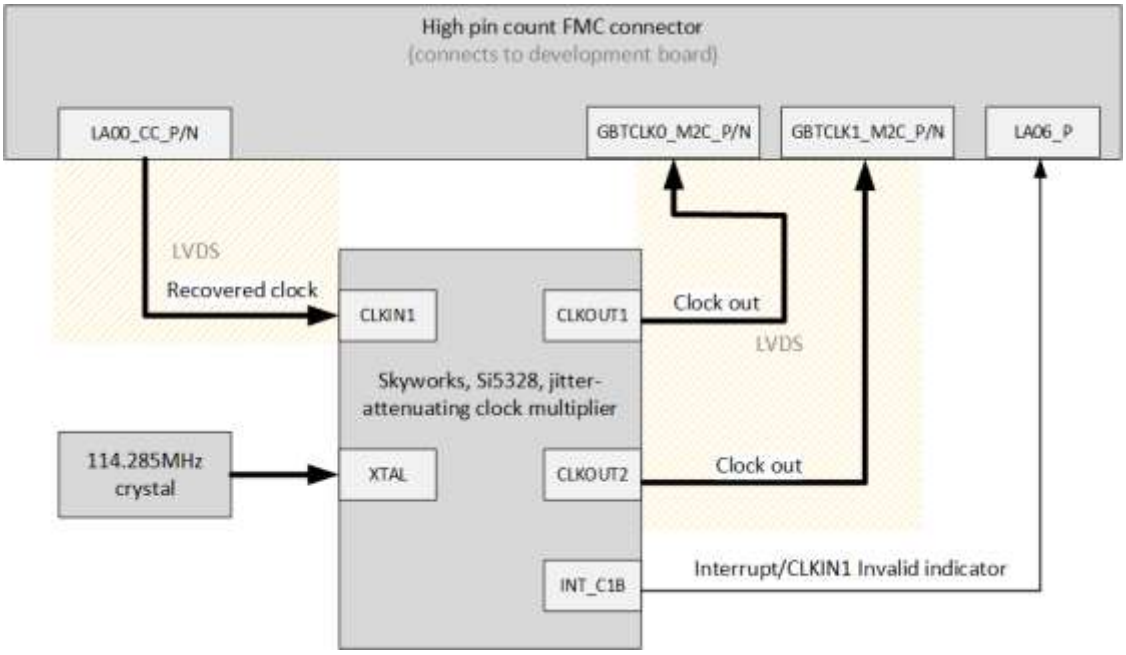
An LED indicates when both the power from the carrier board and the switching regulator are active, and it can be seen in the labelled bottom view of the board above. This LED is connected through a logic buffer to the POWER GOOD signal that is driven by the carrier board and is part of the Vita 57.1 FMC standard. The logic buffer is powered by the 3.3VDC that is generated by the switching regulator.

To aid hardware debug, there is a test point for the 12VDC and 3.3VDC (buck regulator) power supplies on the back side of the Quad SFP28 FMC. When probing these test points, the SFP28 cage can be used as the ground reference as it connects to the system ground.

Clocks

The clock architecture of the Quad SFP28 FMC is based on the jitter-attenuating clock multiplier (Skyworks, Si5328). This clock multiplier operate in a free-running mode, generating a user-specified frequency ranging from 8kHz to 808MHz, synthesized by a crystal oscillator. In Synchronous Ethernet applications, it can also generate a jitter attenuated clock that is synchronous with link partner's clock.

The figure below illustrates the clock connections on the Quad SFP28 FMC.



Clocks

Clock outputs

The Si5328 has two output clocks, both connected to the FMC connector's GT reference clock inputs. These clocks are divided down separately from a common source, allowing them to be programmed to different frequencies while remaining synchronous.

The clock outputs are connected to the FMC pins listed in the table below:

Si5328 pin	I/O standard	FMC pin
CLKOUT1	LVDS	GBTCLK0_M2C_P/N
CLKOUT2	LVDS	GBTCLK1_M2C_P/N

Clock input

The Si5328 has two input clocks, but only one is connected on the Quad SFP28 FMC. This clock input is connected to the FMC pins LA00_CC_P/N, enabling the FPGA to forward a recovered clock from the gigabit transceivers. The Si5328 can perform jitter attenuation on the recovered clock and forward the resulting clock to its outputs. This feature allows the Quad SFP28 FMC to be used in Synchronous Ethernet applications.

The clock inputs are connected to the FMC pins listed in the table below:

Si5328 pin	I/O standard	FMC pin

CLKIN1	LVDS	LA00_CC_P/N

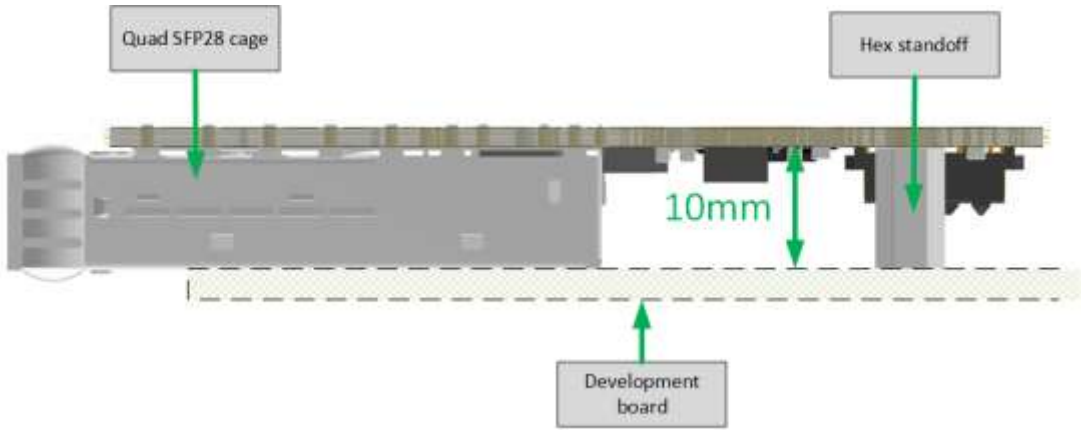
Clock loss alarm

The Si5328 has a logic output INT_C1B that indicates loss-of-signal on the input clock CLKIN1 (the recovered clock). The signal goes HIGH when the device detects missing pulses on the input clock. The clock loss alarm passes through level translation and connects to FMC pin LA06_P.

Mechanical Information

Height Profile

The figure below illustrates the height profile of the Quad SFP28 FMC. All of the components on the Quad SFP28 FMC Max fit within the 10mm gap between the FMC card and the development board. The quad SFP28 cage (Link-PP, SFP28 Quad Cage, LP14CC01000S) has a height of less than 10mm.

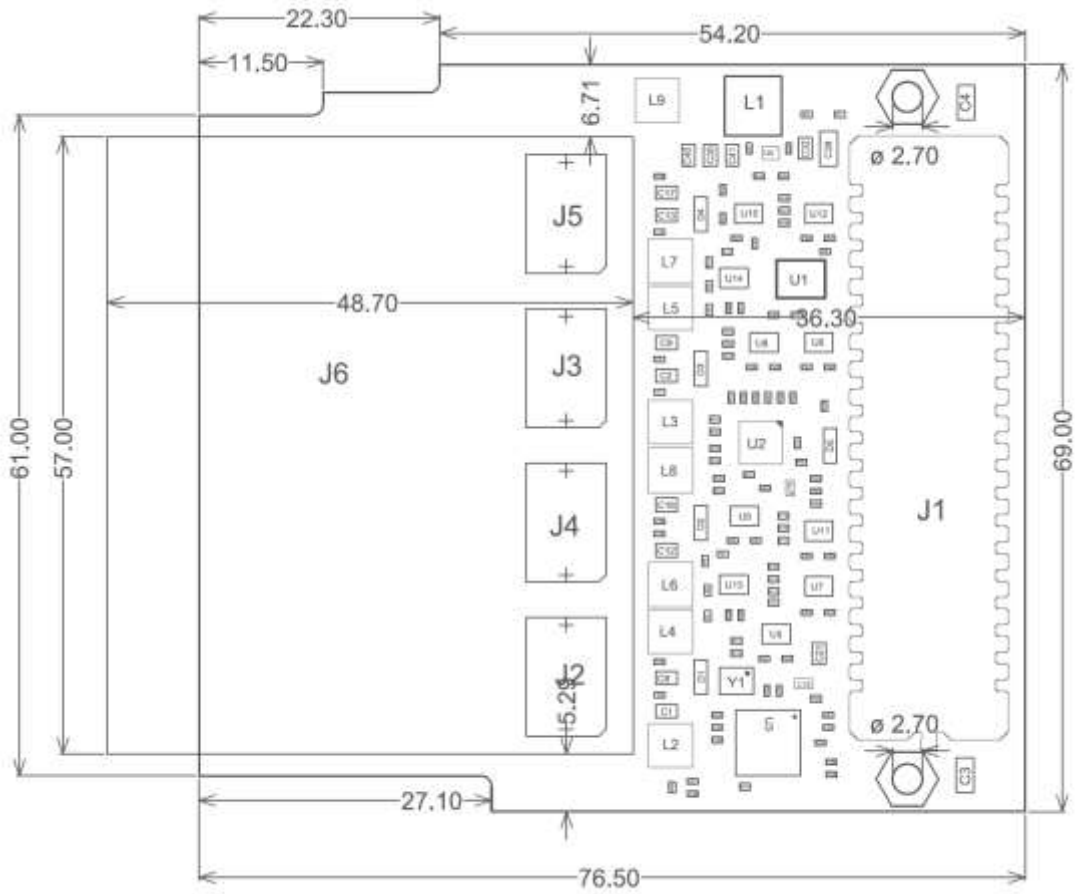


Quad SFP28 FMC height profile (view from side)

Dimensions

The mechanical dimensions of the Quad SFP28 FMC are illustrated in the figure below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



Quad SFP28 FMC mechanical drawing

- Quad SFP28 FMC Rev-A Assembly Drawing PDF

3D Model

The 3D model of the board is available as a STEP file at the links below:

- Quad SFP28 FMC Rev-A 3D STEP model

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the Ethernet FMC comes with 2x hex standoffs. We **highly recommend** using the machine screws on each of these standoffs to fix the mezzanine card to the carrier board. If the fastening screws are misplaced, they can be replaced by the ones listed below, or equivalents.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6516C
  Manufacturer: Assmann

- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head
  Part number: 90116A105
  Supplier: McMaster-Carr

Getting Started

Minimum setup

To develop with the Quad SFP28 FMC, we recommend you start by getting your hands on the minimum hardware and software requirements:

1. An FPGA or MPSoC development board - make sure that it is on our list of compatible boards.
2. A Quad SFP28 FMC to match the dev board.
3. A license for the Xilinx TEMAC IP (unless you want to use something else, see below section on getting a license).
4. Build and run one of our example designs.

Support for other devices: Note that all of our example designs were developed using Xilinx software tools and the Xilinx AXI Ethernet Subsystem IP. Although it is possible to use the Quad SFP28 FMC with FPGA devices from other chip makers such as Intel/Altera, our example designs will not work on these devices and our ability to provide technical support for these other devices is limited at the current time.

Getting a license for the Xilinx Tri-mode Ethernet MAC

When do I need a license?

- You want to use the example designs provided on this website that are based on the Xilinx soft TEMAC. (which is all of them at this point in time)
- You want to create your own designs that are based on the Xilinx soft TEMAC. Using the Xilinx soft TEMAC can save you a considerable amount of time because you benefit from all the Xilinx support including example designs, documentation and drivers.

When do I NOT need a license?

- You want to create your own designs that are **not** based on the Xilinx soft TEMAC.

Your options: Design your own TEMAC, purchase a 3rd party TEMAC, or use the open source TEMAC on opencores.org.

- You are using the Virtex®-4 FX or Virtex-5 LXT/SXT, which contain hard TEMACs.
  AND your device contains a sufficient number of them to support your application. If you need 4 ports, you must have 4 hard TEMACs in your device.

License types

Evaluation license

An evaluation license allows you to do everything you can do with the fully licensed IP core, including configuration, simulation and bitstream generation. You can also test the IP core on hardware, however it will cease to function after a certain period of time (typically 8 hours).

To obtain an evaluation license, visit Xilinx TEMAC Evaluation and click on the link Generate Soft TEMAC License Key. You will have to log into the Xilinx website, select the TEMAC evaluation license and click “Generate license”. Xilinx will then send you the license by email with instructions for how to install it.

Full license

The full license can be purchased as a “site” or “project” license. The project license limits use of the IP core to one project, generally meaning one bitstream, or one printed circuit board. The site license can be used on an unlimited number of projects however is limited to a single company site.

- **Project license part number:** *EF-DI-TEMAC-PROJ*
- **Site license part number:** *EF-DI-TEMAC-SITE*

Both licenses can be purchased from Xilinx here. Alternatively you can search the part numbers on Avnet and Digikey websites.

Compatible Boards

This section of the documentation aims to list all of the development boards for which compatibility with the Quad SFP28 FMC has been checked, and to list constraints and any notes concerning special requirements or limitations with the board.

List of boards

The following development boards have been verified compatible with the Quad SFP28 FMC. For more detailed information regarding compatibility with a particular

development board, including the availability of an example design, click on the name of the board in the table below.

Note that we are still working on the reference designs for these boards and we expect them to be available by September 2024.

Series-7 boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx KC705 Kintex-7 Development board	HPC	✔	Coming soon	4
AMD Xilinx KC705 Kintex-7 Development board	LPC	✔	No	1 [1]
AMD Xilinx VC707 Virtex-7 Development board	HPC1	✔	Coming soon	4
AMD Xilinx VC707 Virtex-7 Development board	HPC2	✔	Coming soon	4
AMD Xilinx VC709 Virtex-7 Development board	HPC	✔	Coming soon	4
AMD Xilinx ZC706 Zynq-7000 Development board	HPC	✔	Coming soon	4
AMD Xilinx ZC706 Zynq-7000 Development board	LPC	✔	No	1 [2]
Avnet PicoZed FMC Carrier Card V2 Zynq-7000 Development Board	LPC	✔	No	1 [3]

UltraScale boards

Carrier	FMC	Compatible	Ref design	Supported Ports

[1] LPC connectors can only support 1-lane PCIe

[2] LPC connectors can only support 1-lane PCIe

[3] LPC connectors can only support 1-lane PCIe

AMD Xilinx KCU105 Kintex UltraScale Development board	HPC	✔	Coming soon	4
AMD Xilinx KCU105 Kintex UltraScale Development board	LPC	✔	No	1 [4]
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC0	✔	Coming soon	4
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC1	✔	Coming soon	4

Zynq Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx ZCU104 Zynq UltraScale+ Development board	LPC	✔	No	1 [5]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC0	✔	Coming soon	4
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	✔	Coming soon	4
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	✔	Coming soon	4
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC1	✔	No	1
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	✔	Coming soon	4
AMD Xilinx ZCU208 Zynq UltraScale+ Development board	FMC+	✔	Coming soon	4
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	✔	Coming soon	4

[4] LPC connectors can only support 1-lane PCIe

[5] LPC connectors can only support 1-lane PCIe

Trenz UltraITX+ Baseboard Zynq UltraScale+ Development board	HPC	✔	Coming soon	4

Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx VCU118 Virtex UltraScale+ Development board	HPC	✘ Use FMC+ instead	No	Not supported
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	✔	Coming soon	4

Versal boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	✔	Coming soon	4
AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	✔	Coming soon	4
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+1	✔	Coming soon	4
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+2	✔	Coming soon	4
AMD Xilinx VPK120 Versal Premium Series Development board	FMC+	✔	Coming soon	4

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the Quad SFP28 FMC, please check your board against the list of requirements below.

VADJ

The development board must have the ability to supply a VADJ voltage between 1.2VDC and 3.3VDC. The Quad SFP28 FMC has an EEPROM containing IPMI data to be used by a power management device. If the development board has such a power management device, an appropriate VADJ voltage will be applied automatically on power-up. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. The SFP28 slots 0-3 are routed to transceivers DP0-DP3 respectively and these transceivers must be connected to the FPGA for the SFP28 slots to work.

Slot	Signal direction	FMC Pin	FMC pin name
0	Link partner to FPGA	C6/C7	DP0_M2C_P/N
	FPGA to Link partner	C2/C3	DP0_C2M_P/N
1	Link partner to FPGA	A2/A3	DP1_M2C_P/N
	FPGA to Link partner	A22/A23	DP1_C2M_P/N
2	Link partner to FPGA	A6/A7	DP2_M2C_P/N
	FPGA to Link partner	A26/A27	DP2_C2M_P/N
3	Link partner to FPGA	A10/A11	DP3_M2C_P/N
	FPGA to Link partner	A30/A31	DP3_C2M_P/N

Note that low pin count (LPC) FMC connectors only have one possible GT connection (DP0). For this reason, carrier boards with LPC FMC connectors can only support a single SFP28 slot (slot 0).

At least one of the GT clock references (FMC pins GBTCLK0_M2C_P/N and GBTCLK1_M2C_P/N) should be connected to one of the GT reference clock inputs of the quad to which DP0-3 connect, or an adjacent quad.

Required I/O

The following FMC pins **must** be connected to the FPGA as they provide critical I/O to the mezzanine card.

FMC Pin	FMC name	Net	Description
H16	LA11_P	PL_I2C_SCL_T	PL I2C bus clock (SCL)
H17	LA11_N	PL_I2C_SDA_T	PL I2C bus data (SDA)
G9	LA03_P	SFP0_TX_DISABLE_T	Slot 0: Disables optical output
G15	LA12_P	SFP1_TX_DISABLE_T	Slot 1: Disables optical output
H20	LA15_N	SFP2_TX_DISABLE_T	Slot 2: Disables optical output
D21	LA17_CC_N	SFP3_TX_DISABLE_T	Slot 3: Disables optical output
H7	LA02_P	SFP0_RS1_T	Slot 0: Rate select 1
H8	LA02_N	SFP0_RS0_T	Slot 0: Rate select 0
G12	LA08_P	SFP1_RS1_T	Slot 1: Rate select 1
G13	LA08_N	SFP1_RS0_T	Slot 1: Rate select 0
C14	LA10_P	SFP2_RS1_T	Slot 2: Rate select 1
C15	LA10_N	SFP2_RS0_T	Slot 2: Rate select 0
C18	LA14_P	SFP3_RS1_T	Slot 3: Rate select 1
C19	LA14_N	SFP3_RS0_T	Slot 3: Rate select 0

Featured I/O

The following FMC pins should ideally be connected to the FPGA as they provide extra functionality to the mezzanine card. These pins are not critical to the operation of the mezzanine card; it can operate without them if they are not connected on the carrier board.

FMC Pin	FMC name	Net	Description
G10	LA03_N	SFP0_TX_FAULT_T	Slot 0: Indicates transmitter fault
H10	LA04_P	SFP0_LOS_T	Slot 0: Indicates receiver loss of signal
H11	LA04_N	SFP0_MOD_ABS_T	Slot 0: Indicates module absence (Slot 0)

G16	LA12_N	SFP1_TX_FAULT_T	Slot 1: Indicates transmitter fault
H13	LA07_P	SFP1_LOS_T	Slot 1: Indicates receiver loss of signal
H14	LA07_N	SFP1_MOD_ABS_T	Slot 1: Indicates module absence (Slot 0)
H19	LA15_P	SFP2_TX_FAULT_T	Slot 2: Indicates transmitter fault
D14	LA09_P	SFP2_LOS_T	Slot 2: Indicates receiver loss of signal
D15	LA09_N	SFP2_MOD_ABS_T	Slot 2: Indicates module absence (Slot 0)
D20	LA17_CC_P	SFP3_TX_FAULT_T	Slot 3: Indicates transmitter fault
C22	LA18_CC_P	SFP3_LOS_T	Slot 3: Indicates receiver loss of signal
C23	LA18_CC_N	SFP3_MOD_ABS_T	Slot 3: Indicates module absence (Slot 0)
D8	LA01_CC_P	SFP0_GRN_LED_T	Slot 0: Green LED enable
D9	LA01_CC_N	SFP0_RED_LED_T	Slot 0: Red LED enable
D11	LA05_P	SFP1_GRN_LED_T	Slot 1: Green LED enable
D12	LA05_N	SFP1_RED_LED_T	Slot 1: Red LED enable
G18	LA16_P	SFP2_GRN_LED_T	Slot 2: Green LED enable
G19	LA16_N	SFP2_RED_LED_T	Slot 2: Red LED enable
D17	LA13_P	SFP3_GRN_LED_T	Slot 3: Green LED enable
D18	LA13_N	SFP3_RED_LED_T	Slot 3: Red LED enable
C10	LA06_P	CLK_LOS_ALARM	Clock loss alarm (recovered clock)
C11	LA06_N	I2C_SW_RST_N_T	I2C switch reset (active low)

Example Designs

We are currently working on the example designs for Quad SFP28 FMC and we expect them to be released by September 2024.

Programming Guide

This section provides the details of the programming requirements to operate the Ethernet FMC hardware and customise functionality.

SFP I/Os

Some of the SFP I/Os must be driven by the FPGA to fixed levels in order to configure the SFP/SPF+/SFP28 modules for normal operation.

Optical output

SFP module input TX_DISABLE allows the FPGA to disable the optical output if so desired. In normal operation however, this input should be driven LOW to **enable** optical output.

Net	Description	FMC pin	Value for normal operation
SFP0_TX_DISABLE_T	Slot 0: Disables optical output	LA03_P	LOW (0)
SFP1_TX_DISABLE_T	Slot 1: Disables optical output	LA12_P	LOW (0)
SFP2_TX_DISABLE_T	Slot 2: Disables optical output	LA15_N	LOW (0)
SFP3_TX_DISABLE_T	Slot 3: Disables optical output	LA17_CC_N	LOW (0)

Note that the pins in the above table must not be left floating. If your SFP modules do not require these signals to be driven, we recommend that you drive them LOW to ensure that the inputs to the level translators are not left floating.

Rate select

The SFP module inputs, RS0 and RS1, generally allow the FPGA to configure the module for different link speeds or performance levels. However, their specific function may vary by vendor. Please refer to the datasheet of your SFP/SFP+/SFP28 module for detailed information on configuring these pins. Note that some modules do not use these pins at all.

If you are unsure what levels to apply to RS0 and RS1, or if your modules do not require them, we recommend driving the signals to the constant values shown in the table below.

Net	Description	FMC pin	Value
SFP0_RS1_T	Slot 0: Rate select 1	LA02_P	LOW (0)
SFP0_RS0_T	Slot 0: Rate select 0	LA02_N	LOW (0)
SFP1_RS1_T	Slot 1: Rate select 1	LA08_P	LOW (0)
SFP1_RS0_T	Slot 1: Rate select 0	LA08_N	LOW (0)
SFP2_RS1_T	Slot 2: Rate select 1	LA10_P	LOW (0)
SFP2_RS0_T	Slot 2: Rate select 0	LA10_N	LOW (0)
SFP3_RS1_T	Slot 3: Rate select 1	LA14_P	LOW (0)
SFP3_RS0_T	Slot 3: Rate select 0	LA14_N	LOW (0)

Note that the pins in the above table must not be left floating. If your SFP modules do not require these signals to be driven, we recommend that you drive them LOW to ensure that the inputs to the level translators are not left floating.

I2C Switch

The I2C switch (PCA9548) is connected to the PS I2C bus and allows the FPGA to communicate with the SFP/SFP+/SFP28 modules and the jitter-attenuating clock multiplier. The I2C switch has address 0x70.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	1	1	0	0	0	0	0x70

The PS I2C bus signals are connected to the FMC pins listed in the table below:

Net Name	Description	FMC pin
PL_I2C_SCL_T	I2C clock (SCL)	LA11_P
PL_I2C_SDA_T	I2C data (SDA)	LA11_N

The channels of the I2C switch are connected as shown in the table below:

I2C Device	Switch channel	Device I2C address
SFP28 Slot 0	0	Module dependent
SFP28 Slot 1	1	Module dependent
SFP28 Slot 2	2	Module dependent
SFP28 Slot 3	3	Module dependent
Clock multiplier	4	0x68

Note that the I2C addresses of the SFP/SFP+/SFP28 modules are dependent on the specific module used. Refer to the module datasheet for this information.

Clock multiplier

The jitter-attenuating clock multiplier (Skyworks, Si5328) must be configured via the PS I2C bus to enable appropriate clocks for the SFP/SFP+/SFP28 modules used. The Si5328 has the I2C address 0x68.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	1	0	1	0	0	0	0x68

Refer to the Si5328 datasheet for detailed information on the device registers and how to configure the clock outputs.

EEPROM

The 2K EEPROM is intended to store information that identifies the mezzanine card and also specifies the power supplies required by the card. This information is typically read by the system power management on the carrier board when it is powered up. In typical user applications, it should not be necessary to read the data on the EEPROM, and we highly recommend against writing to the EEPROM. Nevertheless, if you wish to access the EEPROM, it can be read and written to at the I2C address 0x50.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	1	0	0	0	0	0x50

The EEPROM sits on the FMC card's dedicated I2C bus. The FMC pins of the EEPROM's I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

FMC EEPROM Tool

The Opsero FMC EEPROM Tool can be used to verify, reprogram or update the EEPROM contents of Opsero FMC products using an FPGA or MPSoC board such as the ZCU102 or VCU118 board.

Only use this tool with Opsero FMC products. The use of this tool with FMCs from other manufacturers is strictly prohibited and may result in damage to the FMC or to the carrier board.

Supported boards

The tool currently supports the following FPGA/MPSoC boards. You must have at least one of these boards in order to use the tool.

- KC705
- KCU105
- VCU118
- VCK190
- VMK180
- ZedBoard
- ZCU102 Rev1.0 and Rev1.1
- ZCU104
- ZCU106

Download

The tool can be downloaded at the link below:

Opsero FMC EEPROM Tool v1.5

The zip file contains a boot file (bitstream or BOOT.bin) for each of the supported boards.

Usage instructions

To run the tool, follow these steps:

1. Plug the FMC card you wish to reprogram into one of the FMC connectors of your FPGA/MPSoC board. The tool is designed to probe all of the FMC connectors on the FPGA/MPSoC board.
2. If you are using the ZedBoard, be sure to set the VADJ jumper setting to 1.8V. If you are using the KC705, be sure that your FMC card can support a VADJ of 2.5V, which is the default setting of that board.
3. Connect the UART of your FPGA/MPSoC board to a PC.
4. For Zynq and Zynq MP boards, a BOOT.bin file is provided. Copy this file to your board's SD card and configure it to boot from SD card. Then plug the SD card back into the board and power it up.
5. For FPGA boards, a bitstream is provided with an embedded ELF file. Power up your FPGA/MPSoC board and then download the bitstream to the FPGA board using the Vivado Hardware Manager tool.
6. Open a terminal program such as Putty and connect to the serial port of your FPGA/MPSoC board. If you see nothing in the terminal window, press ENTER to redisplay the menu.
7. Use the menu options to do the following:
   - **Program the EEPROM (p)**
     You will be asked to select the FMC product from a list, and also to enter the product's serial number. Note that entering incorrect information here can lead to your FMC card being damaged by a VADJ voltage that is greater than it's true rating. If you are not sure about the product to select here, please contact Opsero first.

Board Revision History

Rev A

- First board release

References

Board Files

Rev-A

- Quad SFP28 FMC Rev-A Schematics PDF
- Quad SFP28 FMC Rev-A Assembly Drawing PDF
- Quad SFP28 FMC Rev-A 3D STEP model

Part Datasheets

Use the links below to access the datasheets of the significant parts on the mezzanine card.

- Samtec, Mezzanine-side High pin count FMC Connector, ASP-134488-01
- Link-PP, SFP28 20-pin Connector, LP11C000003
- Link-PP, SFP28 Quad Cage, LP14CC01000S
- Skyworks, SyncE Jitter-Attenuating Clock Multiplier, SI5328B-C-GM
- TI, 5A Synchronous Buck Converter, TPS565247DRLR
- TI, 8-channel I2C Switch with Reset, PCA9548ARGER
- TI, Voltage Translator, SN74AVC4T245RSVR
- TI, I2C Level translator, TCA9416DTMR
- Abracon, 114.285MHz Crystal, ABM8-166-114.285MHZ-T2

Revision History

Date	Version	Description
2024-07-29	1.0	Initial PDF release.

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