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Stratix® 10 GX/SX SoC FPGA SOM
Hardware Datasheet

Embedding Intelligence

Document Revision History

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Stratix® 10 GX/SX SoC FPGA System on Module based on the Stratix® 10 GX/SX SoC FPGA CPU. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Stratix® 10 GX/SX SoC FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Stratix® 10 GX/SX SoC FPGA SOM is an extension of Stratix® 10 GX/SX SoC FPGA. Stratix® 10 GX/SX SoC FPGA SOM has a form factor of 110mm x 75mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors and Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Stratix® 10 GX/SX SoC FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
HPS	Hard Processor System
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte

Acronyms	Abbreviations
Mbps	Megabits per sec
MHz	Mega Hertz
NPTH	Non-Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On the Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Intel Stratix® 10 Device Datasheet
- Intel Stratix® 10 GX/SX Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Stratix® 10 GX/SX SoC FPGA SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Stratix® 10 GX/SX SoC FPGA SOM Block Diagram

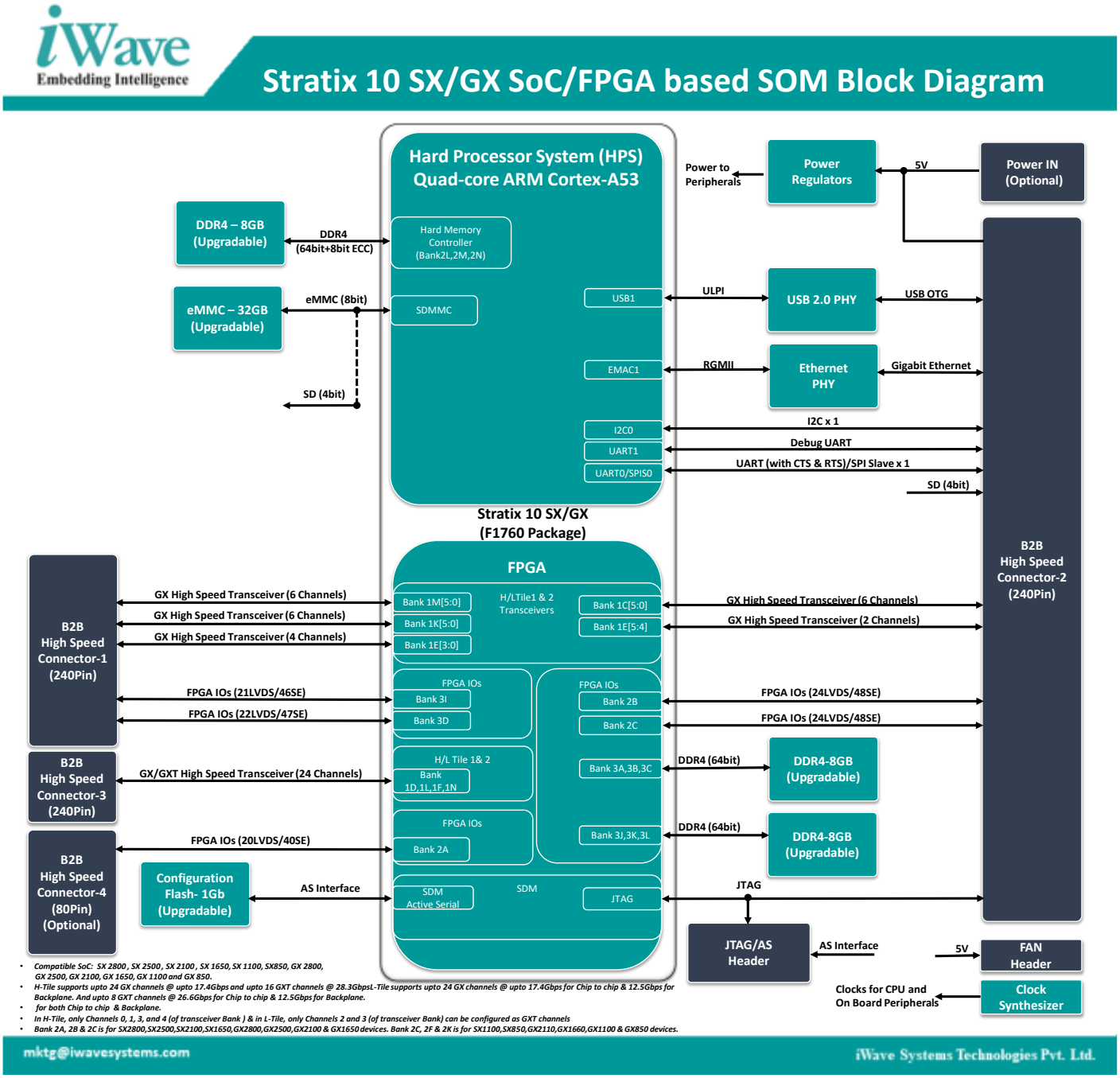


Figure 1: Stratix® 10 GX/SX SoC FPGA SOM Block Diagram

2.2 Stratix® 10 GX/SX SoC FPGA SOM Features

The Stratix® 10 GX/SX SoC FPGA SOM supports the following features.

SoC

Intel's Stratix® 10 SoC & FPGA compatibility with F1760 Package

- Compatible Stratix® 10 SX SoC FPGA Family-SX850, SX1100, SX1650, SX2100, SX2500, SX2800 variants support.
  - Quad-Core 64bit ARM Cortex -A53 with MPU up to 1200MHz
  - Up to 2753K Logic Elements & 9,33,120 ALMs
  - High Speed Transceivers x48 up to 28.3Gbps
- Compatible Stratix® 10 GX FPGA Family - GX850, GX1100, GX1650, GX2100, GX2500, GX2800 variants support.
  - Up to 2753K Logic Elements & 9,33,120 ALMs
  - High Speed Transceivers x48 up to 28.3Gbps

PMIC

- Dialog's DA9062 PMIC with RTC

Memory

- 8GB DDR4 SDRAM (64bit) with 8bit ECC for HPS
- 2 x 8GB DDR4 SDRAM (64bit + 64bit) for FPGA
- 32GB eMMC Flash (Upgradable)
- 1Gb QSPI Flash (Upgradable).

Other On-SOM Features

- Gigabit Ethernet PHY Transceiver for HPS
- USB2.0 Transceiver for HPS
- JTAG/Active Serial Header for SDM
- Fan Header -5V

Board to Board Connector1 Interfaces (240pin)

From FPGA Block

- 16 GX/GXT Transceiver Channels up to 21Gbps[1, 5]
- FPGA IOs & General-Purpose Clocks – Bank3I
  - Upto 21 LVDS/46SE IOs
  - One General Purpose Clock Input LVDS Pair/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended

- FPGA IOs & General-Purpose Clocks – Bank3D
  - Upto 22 LVDS/47SE IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended

Board to Board Connector2 Interfaces (240pin)

From HPS Block: [2]

- Gigabit Ethernet x 1 Port
- USB2.0 OTG x 1 Port
- UART x 1 Port
- I2C x 1 Port
- Debug UART x 1 Port
- JTAG x 1 Port from SDM
- SPI x 1 Port from SDM (Optional)
- SPI Slave x 1 Port (Optional)
- SDMMC x 1 Port (Optional)

From FPGA Block:

- 8 GX/GXT Transceiver Channels up to 21Gbps[1, 5]
- FPGA IOs & General-Purpose Clocks – Bank2B[3]
  - Upto 24 LVDS/48 SE IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended
- FPGA IOs & General-Purpose Clocks – Bank2C[3]
  - Upto 24 LVDS/48 SE IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended

Board to Board Connector3 Interfaces (240pin)

From FPGA Block

- 24 GX/GXT Transceiver Channels up to 28.3Gbps[4, 5]

Board to Board Connector4 Interfaces (80pin)

From FPGA Block

- FPGA IOs – Bank2A[3]
  - Upto 20 LVDS IOs/42 SE IOs
  - Upto 20 LVDS/48 SE IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended

General Specification

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor : 110mm x 75mm

[1] In Stratix® 10 GX/SX SoC FPGA Highest Transceiver Grade supports GXT Transceivers upto 28.3Gbps, but speed capped to 21Gbps due to connector limitation.

[2]In Stratix® 10 SoC/FPGA SOM, these interfaces can be supported only if Stratix® 10 "SoC" family devices (SX family devices) are used which supports Hard Processor System (HPS).

[3]In Stratix® 10 SoC/FPGA SOM Bank 2A, 2B & 2C is renamed as 2C, 2F & 2K respectively for SX1100, SX850, GX2110, GX1660, GX1100 & GX850 devices. Only Bank naming is different and all other functionalities remain same.

[4]H-Tile supports upto 24 GX channels @ upto 17.4Gbps and upto 16 GXT channels @ 28.3GbpsL-Tile supports upto 24 GX channels @ upto 17.4Gbps for Chip to chip & 12.5Gbps for Backplane. And upto 8 GXT channels @ 26.6Gbps for Chip to chip & 12.5Gbps for Backplane.

[5]In H-Tile, only Channels 0, 1, 3, and 4 (of transceiver Bank) & in L-Tile, only Channels 2 and 3 (of transceiver Bank) can be configured as GXT channels.

2.3 Stratix® 10 GX/SX SoC FPGA

The Stratix® 10 GX/SX SoC FPGA SOM is based on Intel's Stratix® 10 GX/SX family devices with NF43 package (1,760 pins, 42.5 mm x 42.5 mm). Intel's Stratix® 10 GX/SX family devices come with FPGA alone devices -GX Family and FPGA + HPS supported devices (which is called as SoC) -SX Family. The Stratix® 10 GX/SX SoC/FPGA comes with three different FPGA fabric speed grade supported devices and different power options. Also, its high-speed transceivers come with three different speed grade supported devices.

The Stratix® 10 SX SoC devices supports Quad Core ARM Cortex-A53 core up to 1.5 GHz speed/core. The Quad ARM Cortex-A53 core with FPGA fabric allows greater flexibility for the system designers and helps lower the system cost and power consumption. This improved logic integration with a rich feature set of embedded peripherals, hardened floating point variable precision DSP blocks, embedded high speed transceivers, hard memory controllers and protocol intellectual property controllers which is ideal for cost-sensitive high-end applications. The Block Diagram of Stratix® 10 GX/SX SoC FPGA device from the datasheet is shown below for reference.

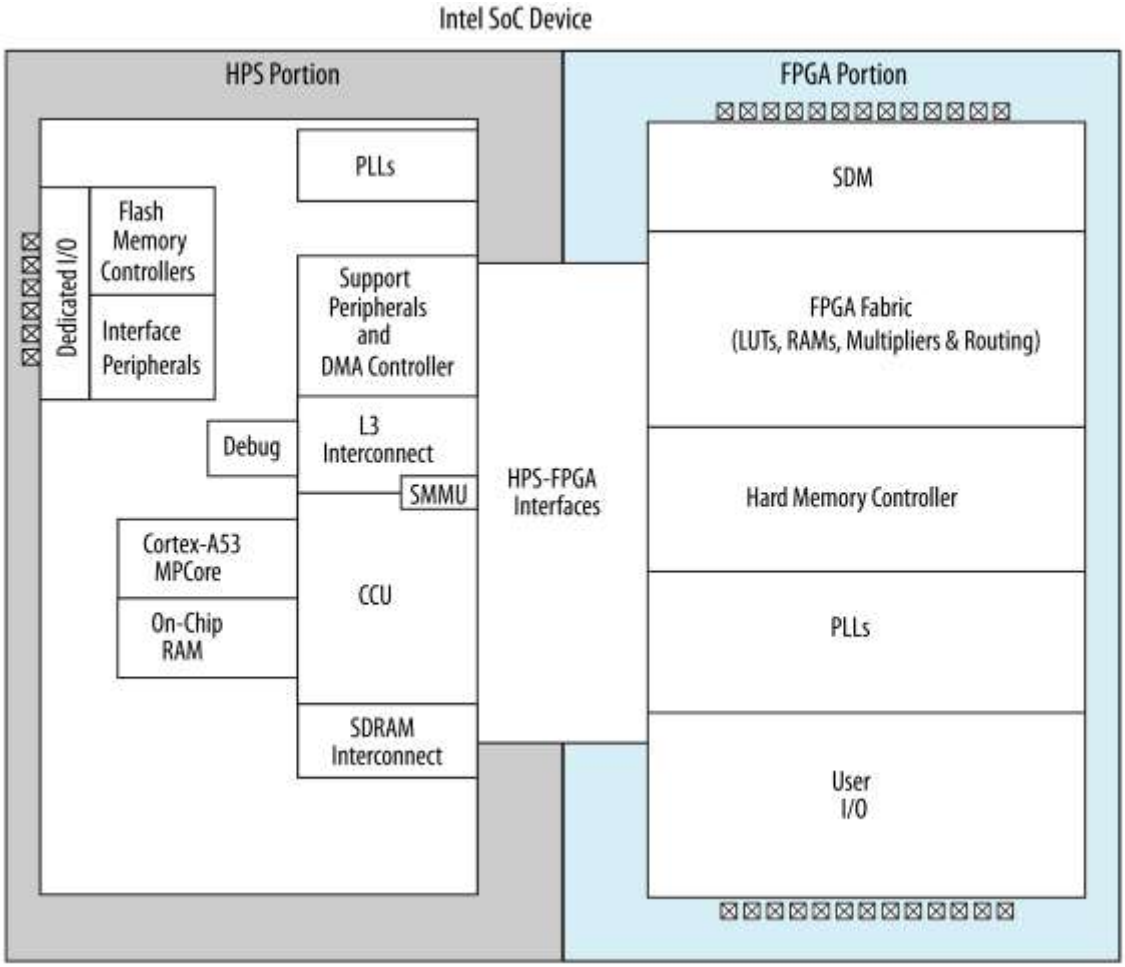
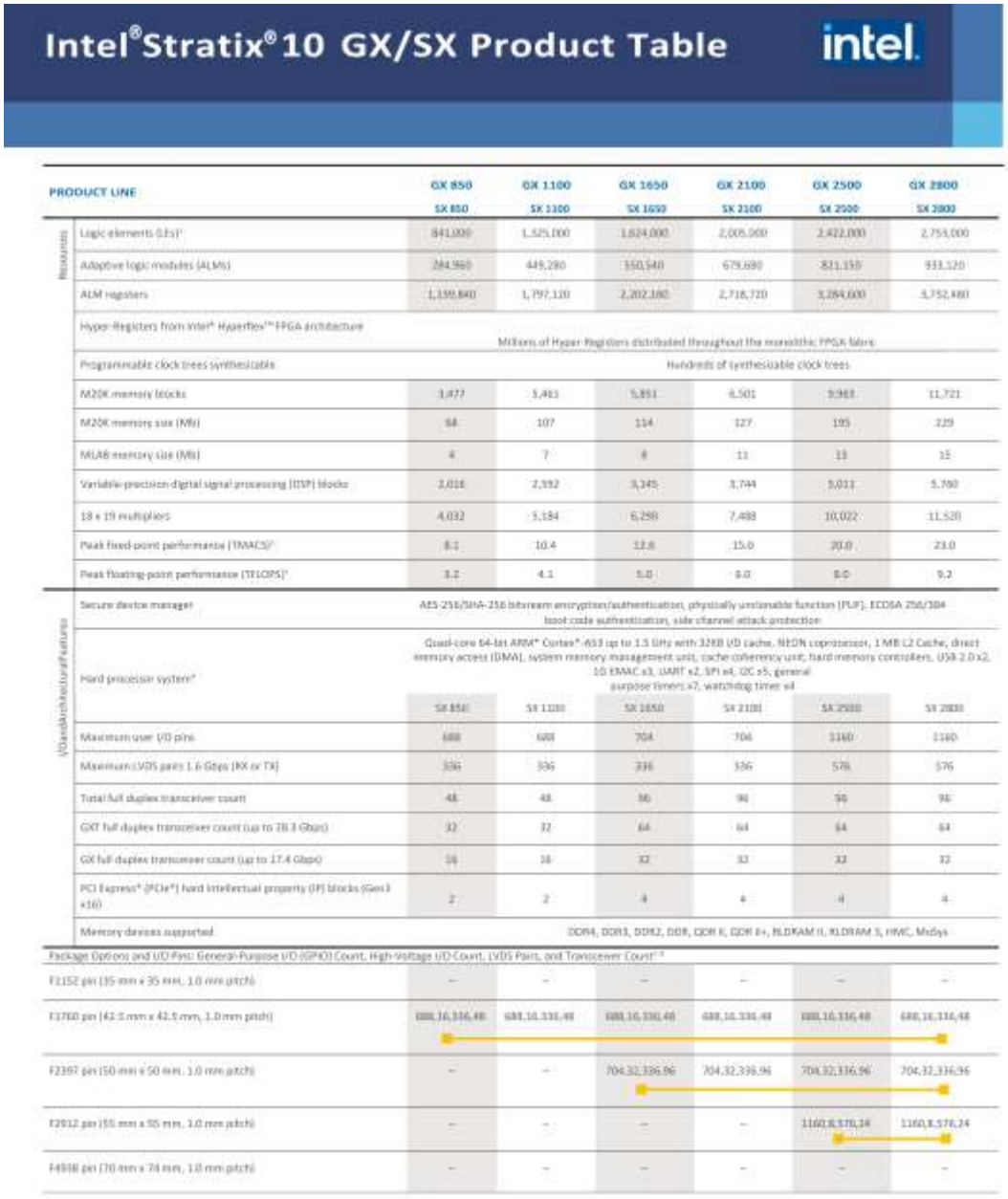


Figure 2: Stratix® 10 SoC Device Simplified Block Diagram

Note: Please refer the latest Stratix® 10 GX/SX Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Stratix® 10 GX/SX SoC FPGA SOM is compatible with SX Family devices (with SoC)- SX850, SX1100, SX1650, SX2100, SX2500, SX2800 variants and GX Family devices (Only FPGA)- GX850, GX1100, GX1650, GX2100, GX2500, GX2800 variants. Feature comparison between these devices is shown below.



PRODUCT LINE	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800
Resources: Logic elements (LEs)[1]	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000
Resources: Adaptive logic modules (ALMs)	284,960	449,280	550,540	679,680	821,150	933,120
Resources: ALM registers	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480
Resources: Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric					
Resources: Programmable clock trees synthesizable	Hundreds of synthesizable clock trees					
Resources: M20K memory blocks	3,477	5,461	5,851	6,501	9,963	11,721
Resources: M20K memory size (Mb)	68	107	114	127	195	229
Resources: MLAB memory size (Mb)	4	7	8	11	13	15
Resources: Variable-precision digital signal processing (DSP) blocks	2,016	2,592	3,145	3,744	5,011	5,760
Resources: 18 x 19 multipliers	4,032	5,184	6,290	7,488	10,022	11,520
Resources: Peak fixed-point performance (TMACS)[2]	8.1	10.4	12.6	15.0	20.0	23.0
Resources: Peak floating-point performance (TFLOPS)[2]	3.2	4.1	5.0	6.0	8.0	9.2
I/O and Architecture Features: Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection					
I/O and Architecture Features: Hard processor system[3]	Quad-core 64-bit ARM* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 10 EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4					
I/O and Architecture Features:	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800
I/O and Architecture Features: Maximum user I/O pins	688	688	704	704	1160	1160
I/O and Architecture Features: Maximum LVDS pairs 1.6 Gbps (RX or TX)	336	336	336	336	576	576
I/O and Architecture Features: Total full duplex transceiver count	48	48	96	96	96	96
I/O and Architecture Features: GXT full duplex transceiver count (up to 28.3 Gbps)	32	32	64	64	64	64
I/O and Architecture Features: GX full duplex transceiver count (up to 17.4 Gbps)	16	16	32	32	32	32
I/O and Architecture Features: PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	2	2	4	4	4	4
I/O and Architecture Features: Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys					
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[4] [5]						
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	–	–	–	–	1160,8,576,24	1160,8,576,24
F4936 pin (70 mm x 74 mm, 1.0 mm pitch)	–	–	–	–	–	–

Figure 3: Stratix® 10 GX/SX SoC FPGA Devices Comparison

2.3.1 Stratix® 10 Power

The Stratix® 10 GX/SX SoC FPGA SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for power management. In Stratix® 10 GX/SX SoC FPGA SOM, Core power, Periphery circuitry power & Digital power of HPS PLL (VCC, VCCP, VCCL_HPS & VCCPLLDIG_HPS) is connected to a SmartVID regulator, where the voltage can be varied between 0.8V to 0.94V based on Temperature. The HPS I/O voltage (VCCIO_HPS) is fixed to 1.8V. The I/O voltage details of each FPGA Bank & High-speed transceiver is mentioned in the corresponding section.

2.3.2 Stratix® 10 Reset

In Stratix® 10 GX/SX SoC FPGA SOM, the POR is taken care internally by the device. It supports warm reset input from Board-to-Board Connector2 pin35 and connected to pin BA9 of the SDM bank of the SoC FPGA having SDM_HPS_COLD_nRESET function.

2.3.3 Stratix® 10 Reference Clock

The Stratix® 10 GX/SX SoC FPGA SOM supports on board clock synthesizer for reference clock to different blocks of Stratix® 10 GX/SX SoC FPGA and On SOM Interfaces. These reference clock details are mentioned in the below table:

Table 3: Stratix® 10 GX/SX SoC FPGA SOM Reference Clocks.

Sl. No	On-SOM Clock Synthesizer Frequency	Stratix® 10 Ball Name/Pin Name	Stratix® 10 Bank	Signal Type/ Termination	Description
1	OUT0 -125MHz	OSC_CLK_1/AY9	SDM	1.8V, LVCMOS	125MHz single ended reference clock for SDM.
2	OUT1 -100MHz	CLK_3I_1P/W5	Bank 3I	1.8V, LVCMOS	100MHz single ended reference clock for FPGA. This is connected to Bank 3I Global clock pin.
3	OUT4 -25MHz	HPS_IOB_24/B20	HPS	1.8V, LVCMOS	25MHz single ended reference clock for HPS.
4	OUT6 -267MHz	CLK_2M_1P/D27 CLK_2M_1N/E27	Bank 2M	1.8V LVDS	LVDS reference clock for HPS DDR4. This is connected to FPGA Bank 2M Global clock pins.
5	OUT2- 300MHz/ 200MHz	CLK_3B_1P/AL5 CLK_3B_1N/AL6	Bank 3B	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM1. This is connected to FPGA Bank 3B Global clock pins.
6	OUT3- 300MHz/ 200MHz	CLK_3K_1P/K8 CLK_3K_1N/K7	Bank 3K	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM2. This is connected to FPGA Bank 3K Global clock pins.
7	OUT5 -25MHz	-	-	1.8V, LVCMOS	25MHz reference clock for Ethernet PHY
8	OUT7 -24MHz	-	-	1.8V, LVCMOS	24MHz reference clock for USB2.0 Transceiver

2.3.4 Stratix® 10 GX/SX SOC FPGA Configuration & Status

The Stratix® 10 GX/SX SoC FPGA uses multi-stage boot process that supports both a non-secure and a secure boot. It supports different configuration schemes -JTAG-based configuration, AS Fast or Standard POR configuration. These configuration schemes are selected using the MSEL pin setting.

The SDM is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the First stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the HPS first and then configure the FPGA or it can be set to configure the FPGA first, then boot the HPS.

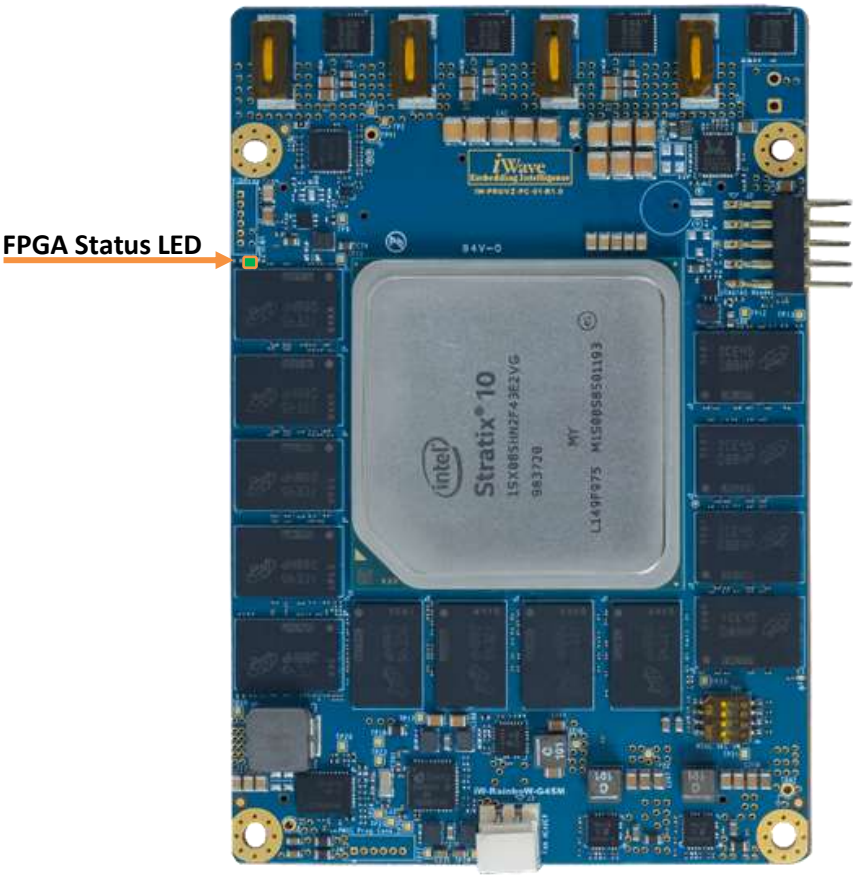


Figure 4: FPGA Configuration Done Indication LED

The Stratix® 10 GX/SX SoC FPGA SOM supports LED for the FPGA Configuration status indication namely CONFIG_DONE. LED D2 is for CONFIG_DONE and it is asserted when the FPGA configuration is complete. It can be used to indicate if the FPGA is configured or not.

2.3.5 Stratix® 10 On SOM Switch

The Stratix® 10 GX/SX SoC FPGA always boots from SDM first and then boots the HPS or FPGA. Stratix® 10 GX/SX SoC FPGA supports the SDM QSPI or JTAG as the First Stage Bootloader in Standard or Fast Mode. Upon device reset, Stratix® 10 GX/SX MSEL pins are read to determine the primary boot device. The ON SOM Switch also supports to switch between Active serial or JTAG connectivity on the On SOM Header. Optional feature of Direct to Factory Image option is also made available on the switch.

The Stratix® 10 GX/SX SoC FPGA SOM supports Switching between Active Serial & JTAG Connectivity on the On SOM Header using the POS1 of the switch (SW1). Refer the below table to select between JTAG & Active Serial.

Table 4: JTAG & Active Serial Switch Truth Table

Stratix® 10 GX/SX - AS/JTAG Header selection	SW1 (4 Position Switch-POS1)	
	POS 1	Switch Position Image
SDM JTAG on AS/JTAG Header	OFF	
SDM Active Serial on AS/JTAG Header	ON	

The Stratix® 10 GX/SX SoC FPGA SOM supports selection between the different configuration schemes making use of POS 2 and POS 3 the switch (SW1). Refer the below table to select between the different configuration schemes.

Table 5: Configuration Selection Truth Table

Stratix® 10 GX/SX Configuration Scheme Selection	SW1 (4 Position Switch-POS2 &POS3)		
	POS 2	POS 3	Switch Position Image
	MSEL1	MSEL2	
Active Serial - Fast Mode	OFF	OFF	
Active Serial - Normal Mode	ON	OFF	

JTAG Only	ON	ON	

The Stratix® 10 GX/SX SoC FPGA SOM also supports option for switching to Factory image and Application Image using the Direct to Factory Image function of the SDM using POS 4 the switch (SW1). Refer the below table to select between Application Image and Factory Image.

Table 6: Application and Factory Image Selection Truth Table

Stratix® 10 GX/SX Application and Factory Image selection	**SW1 (4 Position Switch-POS1)**	
	POS 4	**Switch Position Image**
Application Image	OFF	
Factory Image	ON	

2.4 PMIC with RTC

The Stratix® 10 GX/SX SoC FPGA SOM supports Dialog semiconductor DA9062 PMIC. The I2C0 module of Stratix® 10 GX/SX SoC FPGA HPS is used for PMIC interface through I2C address 0x58.

PMIC's LDO2, LDO3, LDO4 and Buck4 output regulators are connected to I/O voltage of concern Banks (Bank 2A for LDO2, Bank2B for LDO3, Bank2C for LDO4 and Bank 3D & 3I for Buck4) and by default set to 1.8V. The I/O voltages are configurable through software after bootup.

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector2 pin68 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

Important Note: Every Power Off and On, The DA9062 PMIC work as per the initial OTP Settings

2.5 Memory

2.5.1 DDR4 SDRAM with ECC for HPS

The Stratix® 10 GX/SX SoC FPGA SOM supports 72bit, 4GB DDR4 RAM memory for Stratix® 10's HPS. Four 16 bit, 2GB DDR4 SDRAM ICs are RAM memory of 8GB. Also, Stratix® 10 GX/SX SoC FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1067MHz. DDR4 memory is connected to the hard memory controller supported Banks- 2L, 2M and 2N. In Stratix® 10 FPGA only SOM (where HPS is not available), DDR4 can still be used from FPGA fabric. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The HPS DDR4 reference clock is connected to Bank 2M -D27 & E27 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.2 DDR4 SDRAM1 for FPGA

The Stratix® 10 GX/SX SoC FPGA SOM supports 64bit, 8GB DDR4 RAM memory through FPGA Fabric. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for FPGA. These DDR4 devices operates at 1200MHz speed. In Stratix® 10 GX/SX SoC FPGA SOM, Bank 3A, 3B and 3C is used for FPGA DDR4 interface. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The FPGA SDRAM1 DDR4 reference clock is connected to Bank 3B AL5 & AL6 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.3 DDR4 SDRAM2 for FPGA

The Stratix® 10 GX/SX SoC FPGA SOM supports 64bit, 8GB DDR4 RAM memory through FPGA Fabric. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for FPGA. These DDR4 devices operates at 1200MHz speed. In Stratix® 10 GX/SX SoC FPGA SOM, Bank 3J, 3K and 3L is used for FPGA DDR4 interface. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.4 eMMC Flash

The Stratix® 10 GX/SX SoC FPGA SOM supports 32GB eMMC Flash memory for Second Stage Boot & Storage of Stratix® 10 GX/SX SoC FPGA HPS. This eMMC Flash memory is directly connected to the SDMMC controller of the Stratix® 10 SX HPS and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC5.0 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SOM based on the Product Part Number.*

2.6 On SOM Features

2.6.1 JTAG/ Active Serial Header

The Stratix® 10 GX/SX SoC FPGA SOM supports 10Pin JTAG/Active Serial Header (J2) for JTAG or Active Serial interface. JTAG Interface Signals and Active Serial Signals from the SDM of Stratix® 10 GX/SX SoC FPGA is connected to the 10pin Header through a MUX switch. JTAG and Active Serial can be selected by toggling the POS 4 of SW1 DIP Switch. The Stratix® 10 GX/SX SoC FPGA 's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Stratix® 10 GX/SX SoC FPGA. These JTAG interface signals are at 1.8V Voltage level.

The JTAG/Active Serial Header (J2) is physically located on topside of the SOM as shown below. USB Blaster Programming Cable can be directly connected to this JTAG Header. JTAG interface signals are also connected to Board-to-Board Connector2 for access from carrier board.

Number of Pins	- 10
Connector Part	- 610110249121 from Wurth
Mating Connector	- 10pin cable of USB Blaster can be connected to the board directly

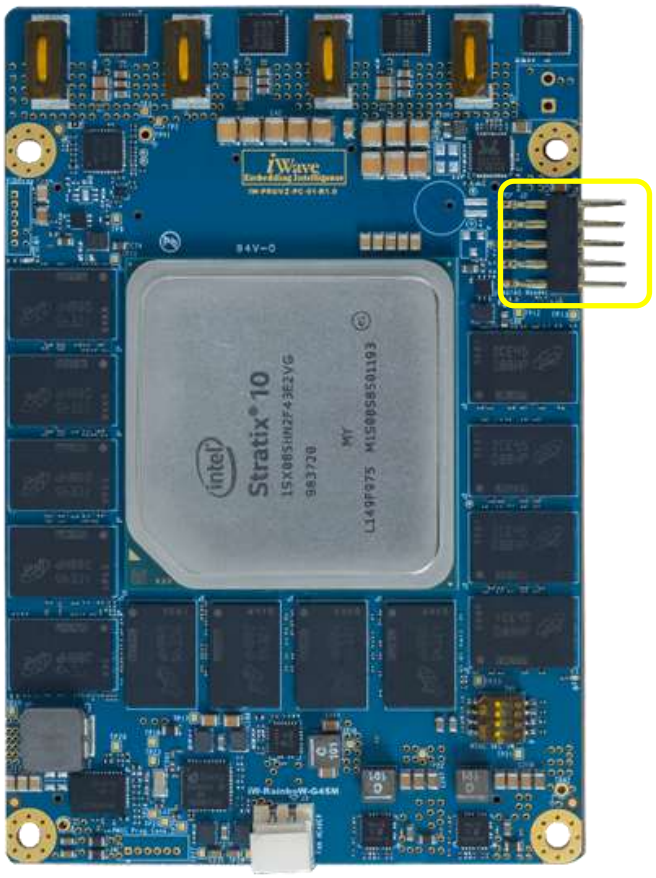


Figure 5: JTAG/Active Serial Header

Table 7: JTAG/Active Serial Header Pinout- JTAG is selected

Pin No	Signal Name	Signal Type/ Termination	Description
1	JTAG_TCK	I, 1.8V CMOS	JTAG test Clock.
2	GND	Power	Ground.
3	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
4	VCC(TRGT)	Power	Target Power Supply
5	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
6	JTAG_RESET	10K PU	JTAG RESET. Not connected to SoC or FPGA
7	NC	-	NC.
8	NC	-	NC.
9	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
10	GND	Power	Ground.

Table 8: JTAG/Active Serial Header Pinout- Active Serial is selected

Pin No	Signal Name	Signal Type/ Termination	Description
1	AS_CLK	I, 1.8V CMOS/10K PD	Dedicated Serial clock to configure flash.
2	GND	Power	Ground.
3	AS_CNFG_DONE	IO, 1.8V OD/10K PU	Configuration status IO to Stratix® 10 GX/SX SoC/FPGA.
4	VCC(TRGT)	Power	Target Power Supply
5	AS_nCONFIG	I, 1.8V CMOS/10K PU	Configuration input to Stratix® 10 GX/SX SoC/FPGA
6	AS_nCE	I, 1.8V CMOS/10K PD	Chip Enable input to Stratix® 10 GX/SX SoC/FPGA.
7	AS_DO	I, 1.8V CMOS	Serial Data input to Configuration flash
8	AS_CS0	I, 1.8V CMOS/10K PU	Chip select input to configuration flash.
9	AS_DI	O, 1.8V CMOS	Serial Data output from configuration flash.
10	GND	Power	Ground.

2.6.2 Fan Header

The Stratix® 10 GX/SX SoC FPGA SOM supports a Fan Header (J3) to connect cooling Fan if required. The Fan Header (J1) is physically located on topside of the SOM as shown below.

Number of Pins - 2

Connector Part - 52125-02-0200-01 from CNC

Mating Connector - 52225-02 from CNC

Compatible Fan (Example) - AFB0505MB from Delta Electronics

Table 9: Fan Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, 5V Power	Supply Voltage.
2	GND	Power	Ground.

2.7 Board to Board Connector1

The Stratix® 10 GX/SX SoC FPGA SOM supports two 240 pin high speed ruggedized terminal strip connectors, One 240pin High-Speed High-Density connector and One 80pin High-Speed High-Density connector for interfaces expansion. All the effort is made in Stratix® 10 GX/SX SoC FPGA SOM design to provide the maximum interfaces of Stratix® 10 GX/SX SoC FPGA to the carrier board through these four Board to Board Connectors.

The Stratix® 10 GX/SX SoC FPGA SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J8) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - QTH-120-01-L-D-A from Samtech
Mating Connector - QSH-120-01-L-D-A from Samtech
Staking Height - 5mm

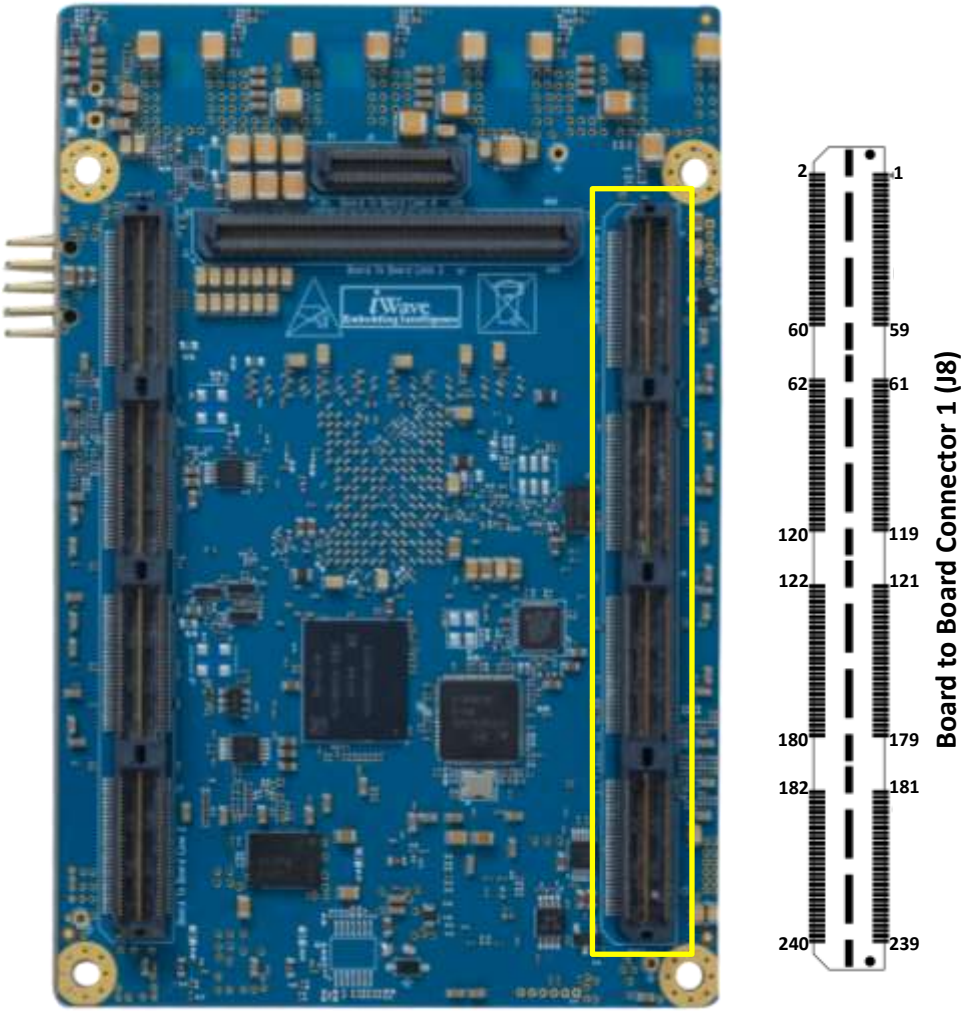


Figure 6: Board to Board Connector1

Table 10: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
GXBL1M_TX_CH0P	3	4	REFCLK_GXBL1M_CHTP
GXBL1M_TX_CH0N	5	6	REFCLK_GXBL1M_CHTN
GND	7	8	GND
GXBL1M_TX_CH1P	9	10	FPGA_LVDS3D_24N_IO1
GXBL1M_TX_CH1N	11	12	FPGA_LVDS3D_16P_IO16
GND	13	14	FPGA_LVDS3D_16N_IO17
GXBL1M_RX_CH1N	15	16	FPGA_LVDS3D_18P_IO12
GXBL1M_RX_CH1P	17	18	FPGA_LVDS3D_18N_IO13
GND	19	20	GND
GXBL1M_RX_CH0N	21	22	FPGA_LVDS3D_15N/CLKOUT_0N
GXBL1M_RX_CH0P	23	24	FPGA_LVDS3D_15P/CLKOUT_0P
GND	25	26	GND
FPGA_LVDS3D_17P_IO14	27	28	FPGA_LVDS3D_20N_IO9
FPGA_LVDS3D_17N_IO15	29	30	FPGA_LVDS3D_20P_IO8
FPGA_LVDS3D_19P_IO10	31	32	FPGA_LVDS3D_14P_IO20
FPGA_LVDS3D_19N_IO11	33	34	FPGA_LVDS3D_14N_IO21
GND	35	36	GND
GXBL1M_TX_CH2P	37	38	FPGA_LVDS3D_9P_IO30
GXBL1M_TX_CH2N	39	40	FPGA_LVDS3D_9N_IO31
GND	41	42	FPGA_LVDS3D_11N_IO27
GXBL1M_TX_CH3P	43	44	FPGA_LVDS3D_11P_IO26
GXBL1M_TX_CH3N	45	46	FPGA_LVDS3D_8P_IO32
GND	47	48	FPGA_LVDS3D_8N_IO33
GXBL1M_RX_CH3N	49	50	FPGA_LVDS3D_7P_IO34
GXBL1M_RX_CH3P	51	52	FPGA_LVDS3D_7N_IO35
GND	53	54	GND
GXBL1M_RX_CH2N	55	56	FPGA_LVDS3D_13N/CLKIN_0N
GXBL1M_RX_CH2P	57	58	FPGA_LVDS3D_13P/CLKIN_0P
GND	59	60	GND
GND	61	62	GND
GXBL1M_TX_CH4P	63	64	REFCLK_GXBL1M_CHBP
GXBL1M_TX_CH4N	65	66	REFCLK_GXBL1M_CHBN
GND	67	68	GND
GXBL1M_TX_CH5P	69	70	FPGA_LVDS3D_4P_IO40
GXBL1M_TX_CH5N	71	72	FPGA_LVDS3D_4N_IO41
GND	73	74	FPGA_LVDS3D_21P_IO6
GXBL1M_RX_CH5N	75	76	FPGA_LVDS3D_21N_IO7
GXBL1M_RX_CH5P	77	78	FPGA_LVDS3D_23P_IO2
GND	79	80	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GXBL1M_RX_CH4N	81	82	FPGA_LVDS3D_12N/CLKIN_1N
GXBL1M_RX_CH4P	83	84	FPGA_LVDS3D_12P/CLKIN_1P
GND	85	86	GND
FPGA_LVDS3D_1P_IO46	87	88	FPGA_LVDS3D_22N_IO5
FPGA_LVDS3D_1N_IO47	89	90	FPGA_LVDS3D_22p_IO4
FPGA_LVDS3D_2P_IO44	91	92	FPGA_LVDS3D_3P_IO42
FPGA_LVDS3D_2N_IO45	93	94	FPGA_LVDS3D_3N_IO43
GND	95	96	GND
GXBL1K_TX_CH0P	97	98	REFCLK_GXBL1K_CHTP
GXBL1K_TX_CH0N	99	100	REFCLK_GXBL1K_CHTN
GND	101	102	GND
GXBL1K_TX_CH1P	103	104	FPGA_LVDS3D_23N_IO3
GXBL1K_TX_CH1N	105	106	FPGA_LVDS3D_5N_IO39
GND	107	108	FPGA_LVDS3D_5P_IO38
GXBL1K_RX_CH1N	109	110	FPGA_LVDS3D_6N_IO37
GXBL1K_RX_CH1P	111	112	FPGA_LVDS3D_6P_IO36
GND	113	114	GND
GXBL1K_RX_CH0N	115	116	FPGA_LVDS3D_10N/CLKOUT_1N
GXBL1K_RX_CH0P	117	118	FPGA_LVDS3D_10P/CLKOUT_1P
GND	119	120	GND
GND	121	122	GND
GXBL1K_TX_CH2P	123	124	FPGA_LVDS3I_15P/CLKOUT_0P
GXBL1K_TX_CH2N	125	126	FPGA_LVDS3I_15N/CLKOUT_0N
GND	127	128	FPGA_LVDS3I_19P_IO10
GXBL1K_TX_CH3P	129	130	FPGA_LVDS3I_13P/CLKIN_0P
GXBL1K_TX_CH3N	131	132	FPGA_LVDS3I_13N/CLKIN_0N
GND	133	134	FPGA_LVDS3I_19N_IO11
GXBL1K_RX_CH3N	135	136	FPGA_LVDS3I_6P_IO36
GXBL1K_RX_CH3P	137	138	FPGA_LVDS3I_6N_IO37
GND	139	140	GND
GXBL1K_RX_CH2N	141	142	FPGA_LVDS3I_10N/CLKOUT_1N
GXBL1K_RX_CH2P	143	144	FPGA_LVDS3I_10P/CLKOUT_1P
GND	145	146	GND
FPGA_LVDS3I_22P_IO4	147	148	FPGA_LVDS3I_5N_IO39
FPGA_LVDS3I_22N_IO5	149	150	FPGA_LVDS3I_5P_IO38
FPGA_LVDS3I_23N_IO3	151	152	FPGA_LVDS3I_4N_IO41
FPGA_LVDS3I_23P_IO2	153	154	FPGA_LVDS3I_4P_IO40
GND	155	156	GND
GXBL1K_TX_CH4P	157	158	REFCLK_GXBL1K_CHBP
GXBL1K_TX_CH4N	159	160	REFCLK_GXBL1K_CHBN
GND	161	162	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GXBL1K_TX_CH5P	163	164	FPGA_LVDS3I_20p_IO8
GXBL1K_TX_CH5N	165	166	FPGA_LVDS3I_20n_IO9
GND	167	168	FPGA_LVDS3I_1n_IO47
GXBL1K_RX_CH5N	169	170	FPGA_LVDS3I_1p_IO46
GXBL1K_RX_CH5P	171	172	FPGA_LVDS3I_24P_IO0
GND	173	174	GND
GXBL1K_RX_CH4N	175	176	FPGA_LVDS3I_2N_IO45
GXBL1K_RX_CH4P	177	178	FPGA_LVDS3I_2P_IO44
GND	179	180	GND
GND	181	182	GND
GXBL1E_TX_CH0P	183	184	REFCLK_GXBL1E_CHTP
GXBL1E_TX_CH0N	185	186	REFCLK_GXBL1E_CHTN
GND	187	188	GND
GXBL1E_TX_CH1P	189	190	FPGA_LVDS3I_24N_IO1
GXBL1E_TX_CH1N	191	192	FPGA_LVDS3I_14N_IO21
GND	193	194	FPGA_LVDS3I_14P_IO20
GXBL1E_RX_CH1N	195	196	FPGA_LVDS3I_16P_IO16
GXBL1E_RX_CH1P	197	198	FPGA_LVDS3I_16N_IO17
GND	199	200	GND
GXBL1E_RX_CH0N	201	202	FPGA_LVDS3I_8N_IO33
GXBL1E_RX_CH0P	203	204	FPGA_LVDS3I_8P_IO32
GND	205	206	GND
FPGA_LVDS3I_3N_IO43	207	208	FPGA_LVDS3I_11N_IO27
FPGA_LVDS3I_3P_IO42	209	210	FPGA_LVDS3I_11P_IO26
FPGA_LVDS3I_7P_IO34	211	212	FPGA_LVDS3I_9P_IO30
FPGA_LVDS3I_7N_IO35	213	214	FPGA_LVDS3I_9N_IO31
GND	215	216	GND
GXBL1E_TX_CH2P	217	218	REFCLK_GXBL1E_CHBP
GXBL1E_TX_CH2N	219	220	REFCLK_GXBL1E_CHBN
GND	221	222	GND
GXBL1E_TX_CH3P	223	224	FPGA_LVDS3I_12N/CLKIN_1N
GXBL1E_TX_CH3N	225	226	FPGA_LVDS3I_17N_IO15
GND	227	228	FPGA_LVDS3I_17P_IO14
GXBL1E_RX_CH3N	229	230	FPGA_LVDS3I_18P_IO12
GXBL1E_RX_CH3P	231	232	SOMPWR_EN
GND	233	234	GND
GXBL1E_RX_CH2N	235	236	FPGA_LVDS3I_21N_IO7
GXBL1E_RX_CH2P	237	238	FPGA_LVDS3I_21P_IO6
GND	239	240	GND

2.7.1 FPGA High Speed Transceivers

The Stratix® 10 GX/SX SoC FPGA SOM supports 16 high speed transceiver channels (6 from 1M bank, 6 from 1K bank & 4 from 1E bank) on Board-to-Board connector1. In Stratix® 10 GX/SX SoC FPGA SOM, Transceiver power to the SoC FPGA is fixed to 1.12V. The Transceivers connected to Board-to-Board Connector1 is capable of running up to a maximum speed of 21Gbps (speed is capped to 21Gbps as the maximum speed supported by the connector is 21Gbps).

For more details on High-Speed Transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-1K Channels				
99	GXBL1K_TX_CH0N	GXBL1K_TX_CH0N/ AA39	O, DIFF	Bank1K channel0 High speed differential transmitter negative.
97	GXBL1K_TX_CH0P	GXBL1K_TX_CH0P/ AA40	O, DIFF	Bank1K channel0 High speed differential transmitter positive.
115	GXBL1K_RX_CH0N	GXBL1K_RX_CH0N/ W35	I, DIFF	Bank1K channel0 High speed differential receiver negative.
117	GXBL1K_RX_CH0P	GXBL1K_RX_CH0P/ W36	I, DIFF	Bank1K channel0 High speed differential receiver positive.
105	GXBL1K_TX_CH1N	GXBL1K_TX_CH1N/ Y41	O, DIFF	Bank1K channel1 High speed differential transmitter negative.
103	GXBL1K_TX_CH1P	GXBL1K_TX_CH1P/ Y42	O, DIFF	Bank1K channel1 High speed differential transmitter positive.
109	GXBL1K_RX_CH1N	GXBL1K_RX_CH1N/ Y37	I, DIFF	Bank1K channel1 High speed differential receiver negative.
111	GXBL1K_RX_CH1P	GXBL1K_RX_CH1P/ Y38	I, DIFF	Bank1K channel1 High speed differential receiver positive.
125	GXBL1K_TX_CH2N	GXBL1K_TX_CH2N/ W39	O, DIFF	Bank1K channel2 High speed differential transmitter negative.
123	GXBL1K_TX_CH2P	GXBL1K_TX_CH2P/ W40	O, DIFF	Bank1K channel2 High speed differential transmitter positive.
141	GXBL1K_RX_CH2N	GXBL1K_RX_CH2N/ U35	I, DIFF	Bank1K channel2 High speed differential receiver negative.
143	GXBL1K_RX_CH2P	GXBL1K_RX_CH2P/ U36	I, DIFF	Bank1K channel2 High speed differential receiver positive.
131	GXBL1K_TX_CH3N	GXBL1K_TX_CH3N/ V41	O, DIFF	Bank1K channel3 High speed differential transmitter negative.
129	GXBL1K_TX_CH3P	GXBL1K_TX_CH3P/ V42	O, DIFF	Bank1K channel3 High speed differential transmitter positive.
135	GXBL1K_RX_CH3N	GXBL1K_RX_CH3N/ V37	I, DIFF	Bank1K channel3 High speed differential receiver negative.
137	GXBL1K_RX_CH3P	GXBL1K_RX_CH3P/ V38	I, DIFF	Bank1K channel3 High speed differential receiver positive.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
159	GXBL1K_TX_CH4N	GXBL1K_TX_CH4N/ U39	O, DIFF	Bank1K channel4 High speed differential transmitter negative.
157	GXBL1K_TX_CH4P	GXBL1K_TX_CH4P/ U40	O, DIFF	Bank1K channel4 High speed differential transmitter positive.
175	GXBL1K_RX_CH4N	GXBL1K_RX_CH4N/ T37	I, DIFF	Bank1K channel4 High speed differential receiver negative.
177	GXBL1K_RX_CH4P	GXBL1K_RX_CH4P/ T38	I, DIFF	Bank1K channel4 High speed differential receiver positive.
165	GXBL1K_TX_CH5N	GXBL1K_TX_CH5N/ T41	O, DIFF	Bank1K channel5 High speed differential transmitter negative.
163	GXBL1K_TX_CH5P	GXBL1K_TX_CH5P/ T42	O, DIFF	Bank1K channel5 High speed differential transmitter positive.
169	GXBL1K_RX_CH5N	GXBL1K_RX_CH5N/ R35	I, DIFF	Bank1K channel5 High speed differential receiver negative.
171	GXBL1K_RX_CH5P	GXBL1K_RX_CH5P/ R36	I, DIFF	Bank1K channel5 High speed differential receiver positive.
160	REFCLK_GXBL1K_CHBN	REFCLK_GXBL1K_CHBN/ AB33	I, DIFF	Bank1K differential Bottom reference clock negative.
158	REFCLK_GXBL1K_CHBP	REFCLK_GXBL1K_CHBP/ AB34	I, DIFF	Bank1K differential Bottom reference clock positive.
100	REFCLK_GXBL1K_CHTN	REFCLK_GXBL1K_CHTN/ Y33	I, DIFF	Bank1K differential Top reference clock negative.
98	REFCLK_GXBL1K_CHTP	REFCLK_GXBL1K_CHTP/ Y34	I, DIFF	Bank1K differential Top reference clock positive.
BANK-1M Channels				
5	GXBL1M_TX_CH0N	GXBL1M_TX_CH0N/ J39	O, DIFF	Bank1M channel0 High speed differential transmitter Negative.
3	GXBL1M_TX_CH0P	GXBL1M_TX_CH0P/ J40	O, DIFF	Bank1M channel0 High speed differential transmitter Positive.
21	GXBL1M_RX_CH0N	GXBL1M_RX_CH0N/ J35	I, DIFF	Bank1M channel0 High speed differential receiver Negative.
23	GXBL1M_RX_CH0P	GXBL1M_RX_CH0P/ J36	I, DIFF	Bank1M channel0 High speed differential receiver Positive.
15	GXBL1M_RX_CH1N	GXBL1M_RX_CH1N/ G35	I, DIFF	Bank1M channel1 High speed differential receiver Negative.
17	GXBL1M_RX_CH1P	GXBL1M_RX_CH1P/ G36	I, DIFF	Bank1M channel1 High speed differential receiver Positive.
11	GXBL1M_TX_CH1N	GXBL1M_TX_CH1N/ H41	O, DIFF	Bank1M channel1 High speed differential transmitter Negative.
9	GXBL1M_TX_CH1P	GXBL1M_TX_CH1P/ H42	I, DIFF	Bank1M channel1 High speed differential receiver Positive.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
55	GXBL1M_RX_CH2N	GXBL1M_RX_CH2N/ C35	I, DIFF	Bank1M channel2 High speed differential receiver Negative.
57	GXBL1M_RX_CH2P	GXBL1M_RX_CH2P/ C36	I, DIFF	Bank1M channel2 High speed differential receiver Positive.
39	GXBL1M_TX_CH2N	GXBL1M_TX_CH2N/ G39	O, DIFF	Bank1M channel2 High speed differential transmitter Negative.
37	GXBL1M_TX_CH2P	GXBL1M_TX_CH2P/ G40	O, DIFF	Bank1M channel2 High speed differential transmitter Positive.
45	GXBL1M_TX_CH3N	GXBL1M_TX_CH3N/ F41	O, DIFF	Bank1M channel3 High speed differential transmitter Negative.
43	GXBL1M_TX_CH3P	GXBL1M_TX_CH3P/ F42	O, DIFF	Bank1M channel3 High speed differential transmitter Positive.
49	GXBL1M_RX_CH3N	GXBL1M_RX_CH3N/ E35	I, DIFF	Bank1M channel3 High speed differential receiver Negative.
51	GXBL1M_RX_CH3P	GXBL1M_RX_CH3P/ E36	I, DIFF	Bank1M channel3 High speed differential receiver Positive.
65	GXBL1M_TX_CH4N	GXBL1M_TX_CH4N/ D41	O, DIFF	Bank1M channel4 High speed differential transmitter Negative.
63	GXBL1M_TX_CH4P	GXBL1M_TX_CH4P/ D42	O, DIFF	Bank1M channel4 High speed differential transmitter Positive.
81	GXBL1M_RX_CH4N	GXBL1M_RX_CH4N/ A31	I, DIFF	Bank1M channel4 High speed differential receiver Negative.
83	GXBL1M_RX_CH4P	GXBL1M_RX_CH4P/ A32	I, DIFF	Bank1M channel4 High speed differential receiver Positive.
71	GXBL1M_TX_CH5N	GXBL1M_TX_CH5N/ E39	O, DIFF	Bank1M channel5 High speed differential transmitter Negative.
69	GXBL1M_TX_CH5P	GXBL1M_TX_CH5P/ E40	O, DIFF	Bank1M channel5 High speed differential transmitter Positive.
75	GXBL1M_RX_CH5N	GXBL1M_RX_CH5N/ D33	I, DIFF	Bank1M channel5 High speed differential receiver Negative.
77	GXBL1M_RX_CH5P	GXBL1M_RX_CH5P/ D34	I, DIFF	Bank1M channel5 High speed differential receiver Positive.
66	REFCLK_GXBL1M_CHBN	REFCLK_GXBL1M_CHBN/ P33	I, DIFF	Bank1M differential Bottom reference clock Negative.
64	REFCLK_GXBL1M_CHBP	REFCLK_GXBL1M_CHBP/ P34	I, DIFF	Bank1M differential Bottom reference clock Positive.
6	REFCLK_GXBL1M_CHTN	REFCLK_GXBL1M_CHTN/ M33	I, DIFF	Bank1M differential Top reference clock Negative.
4	REFCLK_GXBL1M_CHTP	REFCLK_GXBL1M_CHTP/ M34	I, DIFF	Bank1M differential Top reference clock Positive.
BANK-1E Channels				
185	GXBL1E_TX_CH0N	GXBL1E_TX_CH0N/ AN39	O, DIFF	Bank1E channel0 High speed differential transmitter Negative.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
183	GXBL1E_TX_CH0P	GXBL1E_TX_CH0P/ AN40	O, DIFF	Bank1E channel0 High speed differential transmitter Positive.
201	GXBL1E_RX_CH0N	GXBL1E_RX_CH0N/ AL35	I, DIFF	Bank1E channel0 High speed differential receiver Negative.
203	GXBL1E_RX_CH0P	GXBL1E_RX_CH0P/ AL36	I, DIFF	Bank1E channel0 High speed differential receiver Positive.
191	GXBL1E_TX_CH1N	GXBL1E_TX_CH1N/ AM41	O, DIFF	Bank1E channel1 High speed differential transmitter Negative.
189	GXBL1E_TX_CH1P	GXBL1E_TX_CH1P/ AM42	O, DIFF	Bank1E channel1 High speed differential transmitter Positive.
195	GXBL1E_RX_CH1N	GXBL1E_RX_CH1N/ AM37	I, DIFF	Bank1E channel1 High speed differential receiver Negative.
197	GXBL1E_RX_CH1P	GXBL1E_RX_CH1P/ AM38	I, DIFF	Bank1E channel1 High speed differential receiver Positive.
219	GXBL1E_TX_CH2N	GXBL1E_TX_CH2N/ AL39	O, DIFF	Bank1E channel2 High speed differential transmitter Negative.
217	GXBL1E_TX_CH2P	GXBL1E_TX_CH2P/ AL40	O, DIFF	Bank1E channel2 High speed differential transmitter Positive.
235	GXBL1E_RX_CH2N	GXBL1E_RX_CH2N/ AK37	I, DIFF	Bank1E channel2 High speed differential receiver Negative.
237	GXBL1E_RX_CH2P	GXBL1E_RX_CH2P/ AK38	I, DIFF	Bank1E channel2 High speed differential receiver Positive.
225	GXBL1E_TX_CH3N	GXBL1E_TX_CH3N/ AK41	O, DIFF	Bank1E channel3 High speed differential transmitter Negative.
223	GXBL1E_TX_CH3P	GXBL1E_TX_CH3P/ AK42	O, DIFF	Bank1E channel3 High speed differential transmitter Positive.
229	GXBL1E_RX_CH3N	GXBL1E_RX_CH3N/ AJ35	I, DIFF	Bank1E channel3 High speed differential receiver Negative.
231	GXBL1E_RX_CH3P	GXBL1E_RX_CH3P/ AJ36	I, DIFF	Bank1E channel3 High speed differential receiver Positive.
220	REFCLK_GXBL1E_CHBN	REFCLK_GXBL1E_CHBN/ AK33	I, DIFF	Bank1E differential Top reference clock Negative.
218	REFCLK_GXBL1E_CHBP	REFCLK_GXBL1E_CHBP/ AK34	I, DIFF	Bank1E differential Top reference clock Positive.
186	REFCLK_GXBL1E_CHTN	REFCLK_GXBL1E_CHTN/ AH33	I, DIFF	Bank1E differential Bottom reference clock Negative.
184	REFCLK_GXBL1E_CHTP	REFCLK_GXBL1E_CHTP/ AH34	I, DIFF	Bank1E differential Bottom reference clock Positive.

2.7.2 FPGA IOs & General-Purpose Clocks – Bank3I

The Stratix® 10 GX/SX SoC FPGA SOM supports up to 24 LVDS IOs/48 Single Ended IOs and from Stratix® 10 GX/SX FPGA Bank3I on Board-to-Board connector1. In Stratix® 10 SoC/FPGA SOM, Bank3I signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3I signals are routed as LVDS IOs, these pins can be used as SE IOs if required. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Stratix® 10 GX/SX SoC FPGA SOM, upon these 21 LVDS IOs/46 Single Ended IOs from Stratix® 10 GX/SX SoC FPGA Bank3I, one General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Stratix® 10 GX/SX SoC FPGA SOM, Bank3I I/O voltage is by default set to 1.8V. It can be configured to other supported voltages by controlling the Buck 4 of the PMIC after Boot.

For more details on FPGA Bank3I pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
170	FPGA_LVDS3I_1P_IO46	LVDS3I_1P/ V7	IO, 1.8V LVCMOS	Bank3I IO1p Single Ended I/O.
176	FPGA_LVDS3I_2N_IO45	LVDS3I_2N/ U7	IO, 1.8V LVDS	Bank3I 2n differential Negative. Same pin can be configured as Single ended I/O.
178	FPGA_LVDS3I_2P_IO44	LVDS3I_2P/ U8	IO, 1.8V LVDS	Bank3I 2p differential Positive. Same pin can be configured as Single ended I/O.
207	FPGA_LVDS3I_3N_IO43	LVDS3I_3N/ V8	IO, 1.8V LVDS	Bank3I 3n differential Negative. Same pin can be configured as Single ended I/O.
209	FPGA_LVDS3I_3P_IO42	LVDS3I_3P/ W8	IO, 1.8V LVDS	Bank3I 3p differential Positive. Same pin can be configured as Single ended I/O.
152	FPGA_LVDS3I_4N_IO41	LVDS3I_4N/ U9	IO, 1.8V LVDS	Bank3I 4n differential Negative. Same pin can be configured as Single ended I/O.
154	FPGA_LVDS3I_4P_IO40	LVDS3I_4P/ U10	IO, 1.8V LVDS	Bank3I 4p differential Positive. Same pin can be configured as Single ended I/O.
148	FPGA_LVDS3I_5N_IO39	LVDS3I_5N/ V11	IO, 1.8V LVDS	Bank3I 5n differential Negative. Same pin can be configured as Single ended I/O.
150	FPGA_LVDS3I_5P_IO38	LVDS3I_5P/ V10	IO, 1.8V LVDS	Bank3I 5p differential Positive. Same pin can be configured as Single ended I/O.
138	FPGA_LVDS3I_6N_IO37	LVDS3I_6N/ U12	IO, 1.8V LVDS	Bank3I 6n differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
136	FPGA_LVDS3I_6P_IO36	LVDS3I_6P/ V12	IO, 1.8V LVDS	Bank3I 6p differential Positive. Same pin can be configured as Single ended I/O.
213	FPGA_LVDS3I_7N_IO35	LVDS3I_7N/ V1	IO, 1.8V LVDS	Bank3I 7n differential Negative. Same pin can be configured as Single ended I/O.
211	FPGA_LVDS3I_7P_IO34	LVDS3I_7P/ W1	IO, 1.8V LVDS	Bank3I 7p differential Positive. Same pin can be configured as Single ended I/O.
202	FPGA_LVDS3I_8N_IO33	LVDS3I_8N/ V2	IO, 1.8V LVDS	Bank3I 8n differential Negative. Same pin can be configured as Single ended I/O.
204	FPGA_LVDS3I_8P_IO32	LVDS3I_8P/ V3	IO, 1.8V LVDS	Bank3I 8p differential Positive. Same pin can be configured as Single ended I/O.
214	FPGA_LVDS3I_9N_IO31	LVDS3I_9N/ Y1	IO, 1.8V LVDS	Bank3I 9n differential Negative. Same pin can be configured as Single ended I/O.
212	FPGA_LVDS3I_9P_IO30	LVDS3I_9P/ AA1	IO, 1.8V LVDS	Bank3I 9p differential Positive. Same pin can be configured as Single ended I/O.
142	FPGA_LVDS3I_10N/CLKOUT_1N	LVDS3I_10N/ W3	IO, 1.8V LVDS	Bank3I 10n differential Negative. Same pin can be configured as Clock1 Output differential Negative or Single ended I/O.
144	FPGA_LVDS3I_10P/CLKOUT_1P	LVDS3I_10P/ W4	IO, 1.8V LVDS	Bank3I 10p differential Positive. Same pin can be configured as Clock1 Output differential Positive or Single ended I/O.
208	FPGA_LVDS3I_11N_IO27	LVDS3I_11N/ Y2	IO, 1.8V LVDS	Bank3I 11n differential Negative. Same pin can be configured as Single ended I/O.
210	FPGA_LVDS3I_11P_IO26	LVDS3I_11P/ Y3	IO, 1.8V LVDS	Bank3I 11p differential Positive. Same pin can be configured as Single ended I/O.
224	FPGA_LVDS3I_12N/CLKIN_1N	LVDS3I_12N/ V5	IO, 1.8V LVCMOS	Bank3I IO12n Single Ended I/O.
132	FPGA_LVDS3I_13N/CLKIN_0N	LVDS3I_13N/ Y4	IO, 1.8V LVDS	Bank3I 13n differential Negative. Same pin can be configured as Clock0 Input differential Negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
130	FPGA_LVDS3I_13P/CLKIN_0P	LVDS3I_13P/ AA4	IO, 1.8V LVDS	Bank3I 13p differential Positive. Same pin can be configured as Clock0 Input differential Positive or Single ended I/O.
192	FPGA_LVDS3I_14N_IO21	LVDS3I_14N/ Y6	IO, 1.8V LVDS	Bank3I 14n differential Negative. Same pin can be configured as Single ended I/O.
194	FPGA_LVDS3I_14P_IO20	LVDS3I_14P/ W6	IO, 1.8V LVDS	Bank3I 14p differential Positive. Same pin can be configured as Single ended I/O.
126	FPGA_LVDS3I_15N/CLKOUT_0N	LVDS3I_15N/ AA2	IO, 1.8V LVDS	Bank3I 15n differential Negative. Same pin can be configured Clock0 Output differential Negative or as Single ended I/O.
124	FPGA_LVDS3I_15P/CLKOUT_0P	LVDS3I_15P/ AB2	IO, 1.8V LVDS	Bank3I 15p differential Positive. Same pin can be configured as Clock0 Output differential Positive or Single ended I/O.
198	FPGA_LVDS3I_16N_IO17	LVDS3I_16N/ AA6	IO, 1.8V LVDS	Bank3I 16n differential Negative. Same pin can be configured as Single ended I/O.
196	FPGA_LVDS3I_16P_IO16	LVDS3I_16P/ AA5	IO, 1.8V LVDS	Bank3I 16p differential Positive. Same pin can be configured as Single ended I/O.
226	FPGA_LVDS3I_17N_IO15	LVDS3I_17N/ AB3	IO, 1.8V LVDS	Bank3I 17n differential Negative. Same pin can be configured as Single ended I/O.
228	FPGA_LVDS3I_17P_IO14	LVDS3I_17P/ AB4	IO, 1.8V LVDS	Bank3I 17p differential Positive. Same pin can be configured as Single ended I/O.
230	FPGA_LVDS3I_18P_IO12	LVDS3I_18P/ Y7	IO, 1.8V LVCMOS	Bank3I IO18p Single Ended I/O.
134	FPGA_LVDS3I_19N_IO11	LVDS3I_19N/ Y12	IO, 1.8V LVDS	Bank3I 19n differential Negative. Same pin can be configured as Single ended I/O.
128	FPGA_LVDS3I_19P_IO10	LVDS3I_19P/ Y13	IO, 1.8V LVDS	Bank3I 19p differential Positive. Same pin can be configured as Single ended I/O.
166	FPGA_LVDS3I_20n_IO9	LVDS3I_20n/ W10	IO, 1.8V LVDS	Bank3I 20n differential Negative. Same pin can be configured as Single ended I/O.
164	FPGA_LVDS3I_20p_IO8	LVDS3I_20p/ W9	IO, 1.8V LVDS	Bank3I 20p differential Positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
236	FPGA_LVDS3I_21N_IO7	LVDS3I_21N/ AA9	IO, 1.8V LVDS	Bank3I 21n differential Negative. Same pin can be configured as Single ended I/O.
238	FPGA_LVDS3I_21P_IO6	LVDS3I_21P/ AA10	IO, 1.8V LVDS	Bank3I 21p differential Positive. Same pin can be configured as Single ended I/O.
149	FPGA_LVDS3I_22N_IO5	LVDS3I_22N/ W11	IO, 1.8V LVDS	Bank3I 22n differential Negative. Same pin can be configured as Single ended I/O.
147	FPGA_LVDS3I_22P_IO4	LVDS3I_22P/ Y11	IO, 1.8V LVDS	Bank3I 22p differential Positive. Same pin can be configured as Single ended I/O.
151	FPGA_LVDS3I_23N_IO3	LVDS3I_23N/ AA11	IO, 1.8V LVDS	Bank3I 23n differential Negative. Same pin can be configured as Single ended I/O.
153	FPGA_LVDS3I_23P_IO2	LVDS3I_23P/ AA12	IO, 1.8V LVDS	Bank3I 23p differential Positive. Same pin can be configured as Single ended I/O.
190	FPGA_LVDS3I_24N_IO1	LVDS3I_24N/ Y9	IO, 1.8V LVCMOS	Bank3I IO24n Single Ended I/O.
172	FPGA_LVDS3I_24P_IO0	LVDS3I_24P/ Y8	IO, 1.8V LVCMOS	Bank3I IO24p Single Ended I/O.

2.7.3 FPGA IOs & General-Purpose Clocks – Bank3D

The Stratix® 10 GX/SX SoC FPGA SOM supports upto 22 LVDS IOs/47 Single Ended IOs from Stratix® 10 FPGA Bank3D on Board-to-Board connector1. In Stratix® 10 SoC/FPGA SOM, Bank3D signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3A signals are routed as LVDS IOs, these pins can be used as SE IOs if required. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Stratix® 10 GX/SX SoC FPGA SOM, upon these 22 LVDS IOs/47 Single Ended IOs from Stratix® 10 FPGA Bank3D, two General Purpose Clock input LVDS pairs and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Stratix® 10 GX/SX SoC FPGA SOM, Bank3D I/O voltage is by default set to 1.8V. It can be configured to other supported voltages by controlling the Buck 4 of the PMIC after Boot.

For more details on FPGA Bank3D pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
89	FPGA_LVDS3D_1N_IO47	LVDS3D_1N/ AB10	IO, 1.8V LVDS	Bank3D 1n differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
87	FPGA_LVDS3D_1P_IO46	LVDS3D_1P/ AB9	IO, 1.8V LVDS	Bank3D 1p differential Positive. Same pin can be configured as Single ended I/O.
93	FPGA_LVDS3D_2N_IO45	LVDS3D_2N/ AB12	IO, 1.8V LVDS	Bank3D 2n differential Negative. Same pin can be configured as Single ended I/O.
91	FPGA_LVDS3D_2P_IO44	LVDS3D_2P/ AB13	IO, 1.8V LVDS	Bank3D 2p differential Positive. Same pin can be configured as Single ended I/O.
94	FPGA_LVDS3D_3N_IO43	LVDS3D_3N/ AB8	IO, 1.8V LVDS	Bank3D 3n differential Negative. Same pin can be configured as Single ended I/O.
92	FPGA_LVDS3D_3P_IO42	LVDS3D_3P/ AB7	IO, 1.8V LVDS	Bank3D 3p differential Positive. Same pin can be configured as Single ended I/O.
72	FPGA_LVDS3D_4N_IO41	LVDS3D_4N/ AC13	IO, 1.8V LVDS	Bank3D 4n differential Negative. Same pin can be configured as Single ended I/O.
70	FPGA_LVDS3D_4P_IO40	LVDS3D_4P/ AC12	IO, 1.8V LVDS	Bank3D 4p differential Positive. Same pin can be configured as Single ended I/O.
106	FPGA_LVDS3D_5N_IO39	LVDS3D_5N/ AC11	IO, 1.8V LVDS	Bank3D 5n differential Negative. Same pin can be configured as Single ended I/O.
108	FPGA_LVDS3D_5P_IO38	LVDS3D_5P/ AC10	IO, 1.8V LVDS	Bank3D 5p differential Positive. Same pin can be configured as Single ended I/O.
110	FPGA_LVDS3D_6N_IO37	LVDS3D_6N/ AD10	IO, 1.8V LVDS	Bank3D 6n differential Negative. Same pin can be configured as Single ended I/O.
112	FPGA_LVDS3D_6P_IO36	LVDS3D_6P/ AD11	IO, 1.8V LVDS	Bank3D 6p differential Positive. Same pin can be configured as Single ended I/O.
52	FPGA_LVDS3D_7N_IO35	LVDS3D_7N/ AC2	IO, 1.8V LVDS	Bank3D 7n differential Negative. Same pin can be configured as Single ended I/O.
50	FPGA_LVDS3D_7P_IO34	LVDS3D_7P/ AC3	IO, 1.8V LVDS	Bank3D 7p differential Positive. Same pin can be configured as Single ended I/O.
48	FPGA_LVDS3D_8N_IO33	LVDS3D_8N/ AB5	IO, 1.8V LVDS	Bank3D 8n differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
46	FPGA_LVDS3D_8P_IO32	LVDS3D_8P/ AC6	IO, 1.8V LVDS	Bank3D 8p differential Positive. Same pin can be configured as Single ended I/O.
40	FPGA_LVDS3D_9N_IO31	LVDS3D_9N/ AC5	IO, 1.8V LVDS	Bank3D 9n differential Negative. Same pin can be configured as Single ended I/O.
38	FPGA_LVDS3D_9P_IO30	LVDS3D_9P/ AD5	IO, 1.8V LVDS	Bank3D 9p differential Positive. Same pin can be configured as Single ended I/O.
116	FPGA_LVDS3D_10N/CLKOUT_1N	LVDS3D_10N/ AC8	IO, 1.8V LVDS	Bank3D 10n differential Negative. Same pin can be configured as Clock1 Output differential Negative or Single ended I/O.
118	FPGA_LVDS3D_10P/CLKOUT_1P	LVDS3D_10P/ AC7	IO, 1.8V LVDS	Bank3D 10p differential Positive. Same pin can be configured as Clock1 Output differential Positive or Single ended I/O.
42	FPGA_LVDS3D_11N_IO27	LVDS3D_11N/ AD4	IO, 1.8V LVDS	Bank3D 11n differential Negative. Same pin can be configured as Single ended I/O.
44	FPGA_LVDS3D_11P_IO26	LVDS3D_11P/ AD3	IO, 1.8V LVDS	Bank3D 11p differential Positive. Same pin can be configured as Single ended I/O.
82	FPGA_LVDS3D_12N/CLKIN_1N	LVDS3D_12N/ AD9	IO, 1.8V LVDS	Bank3D 12n differential Negative. Same pin can be configured as Clock1 Input differential Negative or Single ended I/O.
84	FPGA_LVDS3D_12P/CLKIN_1P	LVDS3D_12P/ AD8	IO, 1.8V LVDS	Bank3D 12p differential Positive. Same pin can be configured as Clock1 Input differential Positive or Single ended I/O.
56	FPGA_LVDS3D_13N/CLKIN_0N	LVDS3D_13N/ AD6	IO, 1.8V LVDS	Bank3D 13n differential Negative. Same pin can be configured as Clock0 Input differential Negative or Single ended I/O.
58	FPGA_LVDS3D_13P/CLKIN_0P	LVDS3D_13P/ AE6	IO, 1.8V LVDS	Bank3D 13p differential Positive. Same pin can be configured as Clock0 Input differential Positive or Single ended I/O.
34	FPGA_LVDS3D_14N_IO21	LVDS3D_14N/ AE4	IO, 1.8V LVDS	Bank3D 14n differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
32	FPGA_LVDS3D_14P_IO20	LVDS3D_14P/ AE3	IO, 1.8V LVDS	Bank3D 14p differential Positive. Same pin can be configured as Single ended I/O.
22	FPGA_LVDS3D_15N/CLKOUT_0N	LVDS3D_15N/ AC1	IO, 1.8V LVDS	Bank3D 15n differential Negative. Same pin can be configured as Clock0 Output differential Negative or Single ended I/O.
24	FPGA_LVDS3D_15P/CLKOUT_0P	LVDS3D_15P/ AD1	IO, 1.8V LVDS	Bank3D 15p differential Positive. Same pin can be configured as Clock0 Output differential Positive or Single ended I/O.
14	FPGA_LVDS3D_16N_IO17	LVDS3D_16N/ AF7	IO, 1.8V LVDS	Bank3D 16n differential Negative. Same pin can be configured as Single ended I/O.
12	FPGA_LVDS3D_16P_IO16	LVDS3D_16P/ AE7	IO, 1.8V LVDS	Bank3D 16p differential Positive. Same pin can be configured as Single ended I/O.
29	FPGA_LVDS3D_17N_IO15	LVDS3D_17N/ AE1	IO, 1.8V LVDS	Bank3D 17n differential Negative. Same pin can be configured as Single ended I/O.
27	FPGA_LVDS3D_17P_IO14	LVDS3D_17P/ AE2	IO, 1.8V LVDS	Bank3D 17p differential Positive. Same pin can be configured as Single ended I/O.
18	FPGA_LVDS3D_18N_IO13	LVDS3D_18N/ AF6	IO, 1.8V LVDS	Bank3D 18n differential Negative. Same pin can be configured as Single ended I/O.
16	FPGA_LVDS3D_18P_IO12	LVDS3D_18P/ AF5	IO, 1.8V LVDS	Bank3D 18p differential Positive. Same pin can be configured as Single ended I/O.
33	FPGA_LVDS3D_19N_IO11	LVDS3D_19N/ AE9	IO, 1.8V LVDS	Bank3D 19n differential Negative. Same pin can be configured as Single ended I/O.
31	FPGA_LVDS3D_19P_IO10	LVDS3D_19P/ AE8	IO, 1.8V LVDS	Bank3D 19p differential Positive. Same pin can be configured as Single ended I/O.
28	FPGA_LVDS3D_20N_IO9	LVDS3D_20N/ AF11	IO, 1.8V LVDS	Bank3D 20n differential Negative. Same pin can be configured as Single ended I/O.
30	FPGA_LVDS3D_20P_IO8	LVDS3D_20P/ AF12	IO, 1.8V LVDS	Bank3D 20p differential Positive. Same pin can be configured as Single ended I/O.
76	FPGA_LVDS3D_21N_IO7	LVDS3D_21N/ AF10	IO, 1.8V LVDS	Bank3D 21n differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
74	FPGA_LVDS3D_21P_IO6	LVDS3D_21P/ AG10	IO, 1.8V LVDS	Bank3D 21p differential Positive. Same pin can be configured as Single ended I/O.
88	FPGA_LVDS3D_22N_IO5	LVDS3D_22N/ AE11	IO, 1.8V LVDS	Bank3D 22n differential Negative. Same pin can be configured as Single ended I/O.
90	FPGA_LVDS3D_22p_IO4	LVDS3D_22p/ AE12	IO, 1.8V LVDS	Bank3D 22p differential Positive. Same pin can be configured as Single ended I/O.
104	FPGA_LVDS3D_23N_IO3	LVDS3D_23N/ AF9	IO, 1.8V LVDS	Bank3D IO23n Single Ended I/O.
78	FPGA_LVDS3D_23P_IO2	LVDS3D_23P/ AG9	IO, 1.8V LVDS	Bank3D IO23p Single Ended I/O.
10	FPGA_LVDS3D_24N_IO1	LVDS3D_24N/ AG12	IO, 1.8V LVDS	Bank3D IO24n Single Ended I/O.

2.7.4 Power Control Input

The Stratix® 10 GX/SX SoC FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin in Board-to-Board Connector1. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	Pin Name	Signal Type/ Termination	Description
232	SOMPWR_EN	NA	I, 5V	Active High SOM power enable. *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	Power	Ground.

2.8 Board to Board Connector2

The Stratix® 10 GX/SX SoC FPGA SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtech

Mating Connector - QSH-120-01-L-D-A from Samtech

Staking Height - 5mm

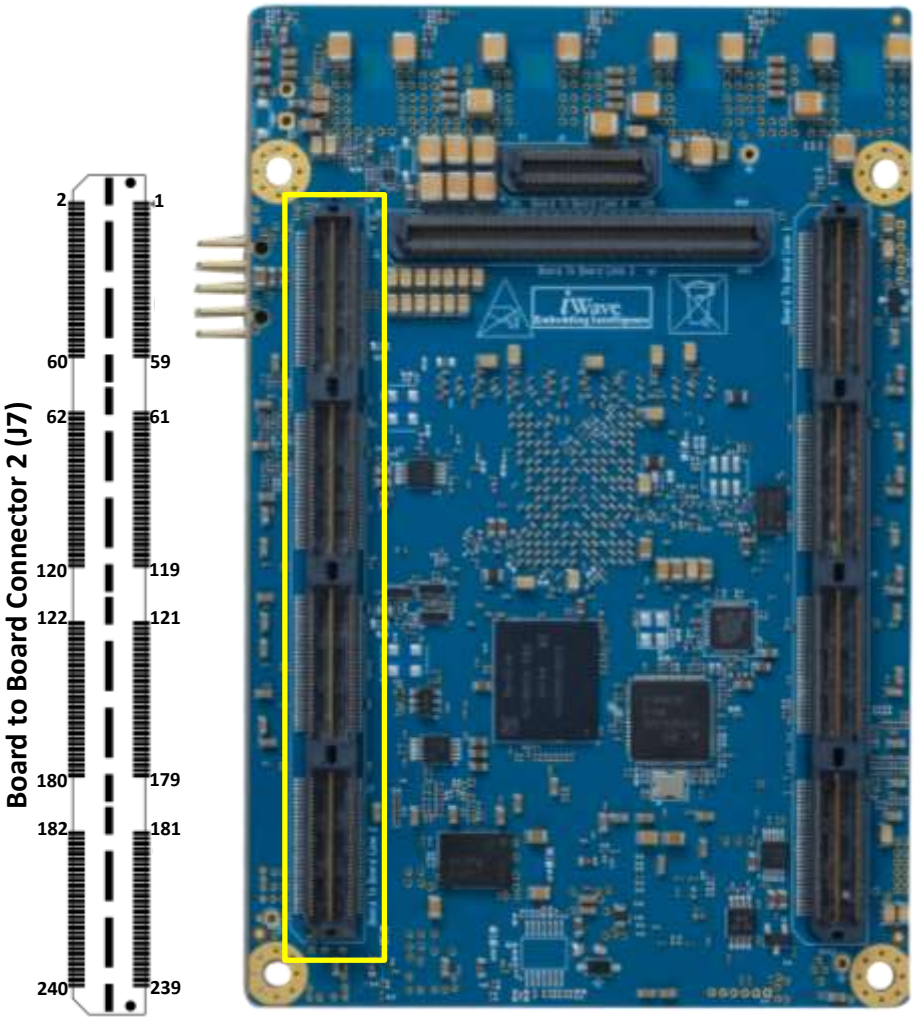


Figure 7: Board to Board Connector2

Table 11: Board to Board Connector2 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
NC	25	26	USB_OTG_DM
SDM_TDI_B2B	27	28	USB_OTG_DP
SDM_TMS_B2B	29	30	GND
SDM_TCK_B2B	31	32	USB_PWR_EN
SDM_TDO_B2B	33	34	USB_OTG_ID
RESET_SW_IN	35	36	VBUS_USB
GND	37	38	IO3V3_10
GPHY_DTXRXM	39	40	NC (Optionally HPS_SD_WP_B2B)
GPHY_DTXRXP	41	42	NC (Optionally HPS_SD_CD_B2B)
GND	43	44	NC (Optionally HPS_SD_PWR_EN_B2B)
GPHY_CTXRXM	45	46	HPS_I2C0_SDA
GPHY_CTXRXP	47	48	HPS_I2C0_SCL
GND	49	50	IO3V4_10
GPHY_BTXRXM	51	52	IO3V5_10
GPHY_BTXRXP	53	54	HPS_UART1_TX
GND	55	56	HPS_UART1_RX
GPHY_ATXRXM	57	58	B_GPHY_LINK_LED
GPHY_ATXRXP	59	60	B_GPHY_ACTIVITY_LED
HPS_SPIS0_CLK/UART0_CTS_N	61	62	NC (Optionally HPS_SD_DATA3_B2B or SDM_AS_CLK_B2B)
HPS_SPIS0_SS0_N/UART0_TX	63	64	NC (Optionally HPS_SD_DATA2_B2B or SDM_AS_CONFIG_DONE_B2B)
HPS_SPIS0_MOSI/UART0_RTS_N	65	66	NC

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
			(Optionally HPS_SD_DATA1_B2B SDM_AS_NCONFIG_B2B)
HPS_SPIS0_MISO/UART0_RX	67	68	VRTC_3V0 (Optionally SDM_AS_STATUS_B2B)
NC (Optionally HPS_SD_DATA0_B2B or SDM_AS_NCSO0_B2B)	69	70	IO3V6_10
NC (Optionally HPS_SD_CMD_B2B or SDM_AS_DATA0_B2B)	71	72	NC (Optionally HPS_SD_CLK_B2B or SDM_AS_DATA1_B2B)
GND	73	74	GND
FPGA_LVDS2B_1N_IO47	75	76	FPGA_LVDS2B_2P_IO44
FPGA_LVDS2B_1P_IO46	77	78	FPGA_LVDS2B_2N_IO45
FPGA_LVDS2B_3N_IO43	79	80	FPGA_LVDS2B_4N_IO41
FPGA_LVDS2B_3P_IO42	81	82	FPGA_LVDS2B_4P_IO40
FPGA_LVDS2B_5N_IO39	83	84	FPGA_LVDS2B_6N_IO37
FPGA_LVDS2B_5P_IO38	85	86	FPGA_LVDS2B_6P_IO36
FPGA_LVDS2B_7P_IO34	87	88	FPGA_LVDS2B_9p_IO30
FPGA_LVDS2B_7N_IO35	89	90	FPGA_LVDS2B_9n_IO31
FPGA_LVDS2B_8p_IO32	91	92	FPGA_LVDS2B_14P_IO20
FPGA_LVDS2B_8n_IO33	93	94	FPGA_LVDS2B_14N_IO21
FPGA_LVDS2B_11P_IO26	95	96	FPGA_LVDS2B_16N_IO17
FPGA_LVDS2B_11N_IO27	97	98	FPGA_LVDS2B_16P_IO16
FPGA_LVDS2B_17P_IO14	99	100	FPGA_LVDS2B_18P_IO12
FPGA_LVDS2B_17N_IO15	101	102	FPGA_LVDS2B_18N_IO13
FPGA_LVDS2B_19P_IO10	103	104	FPGA_LVDS2B_20P_IO8
FPGA_LVDS2B_19N_IO11	105	106	FPGA_LVDS2B_20N_IO9
GND	107	108	GND
FPGA_LVDS2B_12P/CLKIN_1P	109	110	FPGA_LVDS2B_10P/CLKOUT_1P
FPGA_LVDS2B_12N/CLKIN_1N	111	112	FPGA_LVDS2B_10N/CLKOUT_1N
GND	113	114	GND
FPGA_LVDS2B_15P/CLKOUT_0P	115	116	FPGA_LVDS2B_13P/CLKIN_0P
FPGA_LVDS2B_15N/CLKOUT_0N	117	118	FPGA_LVDS2B_13N/CLKIN_0N
GND	119	120	GND
FPGA_LVDS2B_21N_IO7	121	122	FPGA_LVDS2B_22P_IO4
FPGA_LVDS2B_21P_IO6	123	124	FPGA_LVDS2B_22N_IO5
FPGA_LVDS2B_23N_IO3	125	126	FPGA_LVDS2B_24P_IO0
FPGA_LVDS2B_23P_IO2	127	128	FPGA_LVDS2B_24N_IO1
GND	129	130	GND
FPGA_LVDS2C_1P_IO46	131	132	FPGA_LVDS2C_2P_IO44
FPGA_LVDS2C_1N_IO47	133	134	FPGA_LVDS2C_2N_IO45

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
FPGA_LVDS2C_3P_IO42	135	136	FPGA_LVDS2C_4P_IO40
FPGA_LVDS2C_3N_IO43	137	138	FPGA_LVDS2C_4N_IO41
FPGA_LVDS2C_5P_IO38	139	140	FPGA_LVDS2C_6P_IO36
FPGA_LVDS2C_5N_IO39	141	142	FPGA_LVDS2C_6N_IO37
FPGA_LVDS2C_7N_IO35	143	144	FPGA_LVDS2C_8P_IO32
FPGA_LVDS2C_7P_IO34	145	146	FPGA_LVDS2C_8N_IO33
FPGA_LVDS2C_9P_IO30	147	148	FPGA_LVDS2C_14P_IO20
FPGA_LVDS2C_9N_IO31	149	150	FPGA_LVDS2C_14N_IO21
FPGA_LVDS2C_11P_IO26	151	152	FPGA_LVDS2C_16P_IO16
FPGA_LVDS2C_11N_IO27	153	154	FPGA_LVDS2C_16N_IO17
FPGA_LVDS2C_17P_IO14	155	156	FPGA_LVDS2C_18P_IO12
FPGA_LVDS2C_17N_IO15	157	158	FPGA_LVDS2C_18N_IO13
FPGA_LVDS2C_19P_IO10	159	160	FPGA_LVDS2C_20N_IO9
FPGA_LVDS2C_19N_IO11	161	162	FPGA_LVDS2C_20P_IO8
FPGA_LVDS2C_21P_IO6	163	164	FPGA_LVDS2C_22P_IO4
FPGA_LVDS2C_21N_IO7	165	166	FPGA_LVDS2C_22N_IO5
GND	167	168	GND
FPGA_LVDS2C_15P/CLKOUT_0P	169	170	FPGA_LVDS2C_10P/CLKOUT_1P
FPGA_LVDS2C_15N/CLKOUT_0N	171	172	FPGA_LVDS2C_10N/CLKOUT_1N
GND	173	174	GND
FPGA_LVDS2C_12P/CLKIN_1P	175	176	FPGA_LVDS2C_13P/CLKIN_0P
FPGA_LVDS2C_12N/CLKIN_1N	177	178	FPGA_LVDS2C_13N/CLKIN_0N
GND	179	180	GND
FPGA_LVDS2C_23N_IO3	181	182	FPGA_LVDS2C_24P_IO0
FPGA_LVDS2C_23P_IO2	183	184	FPGA_LVDS2C_24N_IO1
GND	185	186	GND
GXBL1C_RX_CH0P	187	188	REFCLK_GXBL1C_CHTP
GXBL1C_RX_CH0N	189	190	REFCLK_GXBL1C_CHTN
GND	191	192	GND
GXBL1C_TX_CH0P	193	194	GXBL1C_RX_CH3P
GXBL1C_TX_CH0N	195	196	GXBL1C_RX_CH3N
GND	197	198	GND
GXBL1C_RX_CH1P	199	200	GXBL1C_TX_CH3P
GXBL1C_RX_CH1N	201	202	GXBL1C_TX_CH3N
GND	203	204	GND
GXBL1C_TX_CH1P	205	206	GXBL1C_RX_CH4P
GXBL1C_TX_CH1N	207	208	GXBL1C_RX_CH4N
GND	209	210	GND
GXBL1C_RX_CH2P	211	212	GXBL1C_TX_CH4P
GXBL1C_RX_CH2N	213	214	GXBL1C_TX_CH4N
GND	215	216	GND

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
GXBL1C_TX_CH2P	217	218	GXBL1C_RX_CH5P
GXBL1C_TX_CH2N	219	220	GXBL1C_RX_CH5N
GND	221	222	GND
REFCLK_GXBL1C_CHBP	223	224	GXBL1C_TX_CH5P
REFCLK_GXBL1C_CHBN	225	226	GXBL1C_TX_CH5N
GND	227	228	GND
GXBL1E_RX_CH4P	229	230	GXBL1E_RX_CH5P
GXBL1E_RX_CH4N	231	232	GXBL1E_RX_CH5N
GND	233	234	GND
GXBL1E_TX_CH4P	235	236	GXBL1E_TX_CH5P
GXBL1E_TX_CH4N	237	238	GXBL1E_TX_CH5N
GND	239	240	GND

2.8.1 HPS & SDM Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Stratix® 10 GX/SX SoC FPGA 's HPS & SDM is explained in the following section.

2.8.1.1 Gigabit Ethernet Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2. The MAC is integrated in the Stratix® 10 GX/SX SoC FPGA HPS and connected to the external Gigabit Ethernet PHY "RTL8211FI-VD-CG" on SOM. This Gigabit Ethernet PHY is interfaced with EMAC1 interface of Stratix® 10 HPS and works at 1.8V IO voltage level.

In Stratix® 10 GX/SX SoC FPGA SOM, PS GPIO "HPS_GPIO0_IO10" is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through FPGA IO "IO3V2_10". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the Carrier board.

In Stratix® 10 GX/SX SoC FPGA SOM, EMAC1 Ethernet PHY Address is set to 100 using on SOM Strapping option.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
39	GPHY_DTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
41	GPHY_DTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
45	GPHY_CTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
47	GPHY_CTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
51	GPHY_BTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
53	GPHY_BTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
57	GPHY_ATXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
59	GPHY_ATXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
58	B_GPHY_LINK_LED	NA	O, 1.8V CMOS	Gigabit Ethernet 1000Mbps Link status LED (Active High).
60	B_GPHY_ACTIVITY_LED	NA	O, 1.8V CMOS	Gigabit Ethernet Activity LED (Active High).

2.8.1.2 USB2.0 OTG Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB1 OTG controller of Stratix® 10 GX/SX SoC FPGA HPS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Stratix® 10 GX/SX SoC FPGA SOM supports "USB3320" ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Stratix® 10 GX/SX SoC FPGA SOM, HPS GPIO "HPS_GPIO0_IO11" is used for USB ULPI PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Stratix® 10 GX/SX SoC FPGA SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
26	USB_OTG_DM	NA	IO, USB	USB OTG data negative.
28	USB_OTG_DP	NA	IO, USB	USB OTG data positive.
32	USB_PWR_EN	NA	O, 3.3V CMOS	USB active high power enable output to control external USB VBUS.
34	USB_OTG_ID	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
36	VBUS_USB	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.8.1.3 SD/SDIO Interface (Optional)

The Stratix® 10 GX/SX SoC FPGA SOM optionally supports SD/SDIO interface on Board-to-Board Connector2. The SDMMC controller of Stratix® 10 HPS can be used for SD/SDIO interface on the Board-to-Board Connector. By default, these lines are connected to the On SOM eMMC. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (19Mhz), High Speed mode (50Mhz), SDR12 (25Mhz), SDR25 (25Mhz), SDR50 (100Mhz), SDR104 (200Mhz) & DDR50 mode (50Mhz). Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Stratix® 10 GX/SX SoC FPGA SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through HPS pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
40	HPS_SD_WP_B2B	HPS_IOB_20/ D20	O, 1.8V LVCMOS	SD Write Protect.
42	HPS_SD_CD_B2B	HPS_IOB_19/ D18	I, 1.8V LVCMOS	SD Card Detect.
44	HPS_SD_PWR_EN_B2B	HPS_IOB_23/ R19	O, 1.8V LVCMOS	SD Power Enable/Voltage select through PS GPIO.
62	HPS_SD_DATA3_B2B	HPS_IOB_18/ P19	IO, 1.8V LVCMOS	SD DATA3.
64	HPS_SD_DATA2_B2B	HPS_IOB_17/ H18	IO, 1.8V LVCMOS	SD DATA2.
66	HPS_SD_DATA1_B2B	HPS_IOB_16/ K21	IO, 1.8V LVCMOS	SD DATA1.
69	HPS_SD_DATA0_B2B	HPS_IOB_13/ J18	IO, 1.8V LVCMOS	SD DATA0.
71	HPS_SD_CMD_B2B	HPS_IOB_14/ L21	IO, 1.8V LVCMOS	SD Command.
72	HPS_SD_CLK_B2B	HPS_IOB_15/ C20	O, 1.8V LVCMOS	SD Clock.

2.8.1.4 SPI Interface (Optional)

The Stratix® 10 GX/SX SoC FPGA SOM supports one SPI slave interface with one chip select on Board-to-Board Connector2 from the HPS Bank. The SPIS0 controller of Stratix® 10 SX HPS is used for SPI interface through HPS pins. The same pins are used for UART support by default. It can function in slave mode and supports full-duplex operation.

For more details on SPI Slave Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
61	HPS_SPIS0_CLK/UART0_CTS_N	HPS_IOA_1/ A15	O, 1.8V LVCMOS	SPI clock.
65	HPS_SPIS0_MOSI/UART0_RTS_N	HPS_IOA_2/ B15	O, 1.8V LVCMOS	SPI chip select0.
63	HPS_SPIS0_SS0_N/UART0_TX	HPS_IOA_3/ C18	IO, 1.8V LVCMOS	SPI Master output Slave input.
67	HPS_SPIS0_MISO/UART0_RX	HPS_IOA_4/ A11	IO, 1.8V LVCMOS	SPI Master input Slave output.

2.8.1.5 Debug UART Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports one Debug UART interface on Board-to-Board Connector2. The UART1 controller of Stratix® 10 SX HPS is used for Debug UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
54	HPS_UART1_TX	HPS_IOA_7/ B14	O, 1.8V LVCMOS	UART1 Transmit data line for Debug.
56	HPS_UART1_RX	HPS_IOA_8/ B17	I, 1.8V LVCMOS	UART1 Receive data line for Debug.

2.8.1.6 Data UART Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports one DATA UART interface on Board-to-Board Connector2. The UART0 controller of Stratix® 10 SX's HPS is used for Data UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
61	HPS_SPIS0_CLK/UART0_CTS_N	HPS_IOA_1/ A15	O, 1.8V LVCMOS	UART0 Clear to Send data line.
65	HPS_SPIS0_MOSI/UART0_RTS_N	HPS_IOA_2/ B15	I, 1.8V LVCMOS	UART0 Request to Send data line.
63	HPS_SPIS0_SS0_N/UART0_TX	HPS_IOA_3/ C18	O, 1.8V LVCMOS	UART0 Transmit data line.
67	HPS_SPIS0_MISO/UART0_RX	HPS_IOA_4/ A11	I, 1.8V LVCMOS	UART0 Receive data line.

2.8.1.7 I2C Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports one I2C interface on Board-to-Board Connector2. The I2C0 module of Stratix® 10 SX's HPS is used for I2C interface through HPS pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM PMIC with I2C address 0x58 in the Stratix® 10 GX/SX SoC FPGA SOM.

When using Stratix® 10 GX devices where HPS is not available, optionally LVDS signals are connected for configuring and using and I2C.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
46	HPS_I2C0_SDA	HPS_IOA_5/ B13	IO, 1.8V OD/ 4.7K PU	I2C0 data.
48	HPS_I2C0_SCL	HPS_IOA_6/ A14	O, 1.8V OD/ 4.7K PU	I2C0 clock.

2.8.1.8 JTAG Interface

The Stratix® 10 GX/SX SoC FPGA SOM supports JTAG interface on Board-to-Board Connector2. The Stratix® 10 GX/SX SoC FPGA 's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Intel Stratix® 10 SoC FPGA. These JTAG interface signals are also connected to on-board JTAG connector. The JTAG connection can be selected to either Board-to-Board Connector2 or On Board JTAG Header using bit-1 of SW1.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
27	SDM_TDI_B2B	TDI_SDM/ BA10	I, 1.8V LVCMOS/ 10K	JTAG Test Data Input.
29	SDM_TMS_B2B	TMS_SDM/ AY12	I, 1.8V LVCMOS/ 10K	JTAG Test Mode Select.
31	SDM_TCK_B2B	TCK_SDM/ AY11	I, 1.8V LVCMOS/ 10K	JTAG Test Clock.
33	SDM_TDO_B2B	TDO_SDM/ AW13	O, 1.8V LVCMOS	JTAG Test Data Output.

2.8.2 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Stratix® 10 GX/SX SoC FPGA 's FPGA is explained in the following section.

2.8.2.1 FPGA High Speed Transceivers

The Stratix® 10 GX/SX SoC FPGA SOM supports 8 high speed transceiver channels (6 from 1C bank & 2 from 1E bank) on Board-to-Board connector2. In Stratix® 10 GX/SX SoC FPGA SOM, Transceiver power to the SoC FPGA is fixed to 1.12V. The Transceivers connected to Board-to-Board Connector2 is capable of running up to a maximum speed of 21Gbps (speed is capped to 21Gbps as the maximum speed supported by the connector is 21Gbps).

For more details on Transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-1C Channels				
187	GXBL1C_RX_CH0P	GXBL1C_RX_CH0P/ AV30	I, DIFF	Bank1C channel0 High speed differential receiver positive.
189	GXBL1C_RX_CH0N	GXBL1C_RX_CH0N/ AV29	I, DIFF	Bank1C channel0 High speed differential receiver Negative.
193	GXBL1C_TX_CH0P	GXBL1C_TX_CH0P/ BB34	O, DIFF	Bank1C channel0 High speed differential transmitter positive.
195	GXBL1C_TX_CH0N	GXBL1C_TX_CH0N/ BB33	O, DIFF	Bank1C channel0 High speed differential transmitter Negative.
199	GXBL1C_RX_CH1P	GXBL1C_RX_CH1P/ AY30	I, DIFF	Bank1C channel1 High speed differential receiver positive.
201	GXBL1C_RX_CH1N	GXBL1C_RX_CH1N/ AY29	I, DIFF	Bank1C channel1 High speed differential receiver Negative.
205	GXBL1C_TX_CH1P	GXBL1C_TX_CH1P/ BA36	O, DIFF	Bank1C channel1 High speed differential transmitter positive.
207	GXBL1C_TX_CH1N	GXBL1C_TX_CH1N/ BA35	O, DIFF	Bank1C channel1 High speed differential transmitter Negative.
211	GXBL1C_RX_CH2P	GXBL1C_RX_CH2P/ BB30	I, DIFF	Bank1C channel2 High speed differential receiver positive.
213	GXBL1C_RX_CH2N	GXBL1C_RX_CH2N/ BB29	I, DIFF	Bank1C channel2 High speed differential receiver Negative.
217	GXBL1C_TX_CH2P	GXBL1C_TX_CH2P/ BB38	O, DIFF	Bank1C channel2 High speed differential transmitter positive.
219	GXBL1C_TX_CH2N	GXBL1C_TX_CH2N/ BB37	O, DIFF	Bank1C channel2 High speed differential transmitter Negative.
194	GXBL1C_RX_CH3P	GXBL1C_RX_CH3P/ AW32	I, DIFF	Bank1C channel3 High speed differential receiver positive.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
196	GXBL1C_RX_CH3N	GXBL1C_RX_CH3N/ AW31	I, DIFF	Bank1C channel3 High speed differential receiver Negative.
200	GXBL1C_TX_CH3P	GXBL1C_TX_CH3P/ AY38	O, DIFF	Bank1C channel3 High speed differential transmitter positive.
202	GXBL1C_TX_CH3N	GXBL1C_TX_CH3N/ AY37	O, DIFF	Bank1C channel3 High speed differential transmitter Negative.
206	GXBL1C_RX_CH4P	GXBL1C_RX_CH4P/ BA32	I, DIFF	Bank1C channel4 High speed differential receiver positive.
208	GXBL1C_RX_CH4N	GXBL1C_RX_CH4N/ BA31	I, DIFF	Bank1C channel4 High speed differential receiver Negative.
212	GXBL1C_TX_CH4P	GXBL1C_TX_CH4P/ BA40	O, DIFF	Bank1C channel4 High speed differential transmitter positive.
214	GXBL1C_TX_CH4N	GXBL1C_TX_CH4N/ BA39	O, DIFF	Bank1C channel4 High speed differential transmitter Negative.
218	GXBL1C_RX_CH5P	GXBL1C_RX_CH5P/ AY34	I, DIFF	Bank1C channel5 High speed differential receiver positive.
220	GXBL1C_RX_CH5N	GXBL1C_RX_CH5N/ AY33	I, DIFF	Bank1C channel5 High speed differential receiver Negative.
224	GXBL1C_TX_CH5P	GXBL1C_TX_CH5P/ AV38	O, DIFF	Bank1C channel5 High speed differential transmitter positive.
226	GXBL1C_TX_CH5N	GXBL1C_TX_CH5N/ AV37	O, DIFF	Bank1C channel5 High speed differential transmitter Negative.
223	REFCLK_GXBL1C_CHBP	REFCLK_GXBL1C_CHBP/ AV34	I, DIFF	Bank1C differential Bottom reference clock positive.
225	REFCLK_GXBL1C_CHBN	REFCLK_GXBL1C_CHBN/ AV33	I, DIFF	Bank1C differential Bottom reference clock Negative.
188	REFCLK_GXBL1C_CHTP	REFCLK_GXBL1C_CHTP/ AT34	I, DIFF	Bank1C differential Top reference clock positive.
190	REFCLK_GXBL1C_CHTN	REFCLK_GXBL1C_CHTN/ AT33	I, DIFF	Bank1C differential Top reference clock Negative.
BANK-1E Channels				
229	GXBL1E_RX_CH4P	GXBL1E_RX_CH4P/ AH38	I, DIFF	Bank1E channel4 High speed differential receiver positive.
231	GXBL1E_RX_CH4N	GXBL1E_RX_CH4N/ AH37	I, DIFF	Bank1E channel4 High speed differential receiver Negative.
235	GXBL1E_TX_CH4P	GXBL1E_TX_CH4P/ AJ40	O, DIFF	Bank1E channel4 High speed differential transmitter positive.
237	GXBL1E_TX_CH4N	GXBL1E_TX_CH4N/ AJ39	O, DIFF	Bank1E channel4 High speed differential transmitter Negative.
230	GXBL1E_RX_CH5P	GXBL1E_RX_CH5P/ AF38	I, DIFF	Bank1E channel5 High speed differential receiver positive.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
232	GXBL1E_RX_CH5N	GXBL1E_RX_CH5N/ AF37	I, DIFF	Bank1E channel5 High speed differential receiver Negative.
236	GXBL1E_TX_CH5P	GXBL1E_TX_CH5P/ AH42	O, DIFF	Bank1E channel5 High speed differential transmitter positive.
238	GXBL1E_TX_CH5N	GXBL1E_TX_CH5N/ AH41	O, DIFF	Bank1E channel5 High speed differential transmitter Negative.

2.8.2.2 FPGA IOs & General-Purpose Clocks – Bank2B

The Stratix® 10 GX/SX SoC FPGA SOM supports up to 24 LVDS IOs/48 Single Ended IOs and from Stratix® 10 GX/SX FPGA Bank2B on Board-to-Board connector2. In Stratix® 10 SoC/FPGA SOM, Bank2B signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank2B signals are routed as LVDS IOs, these pins can be used as SE IOs if required. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Stratix® 10 GX/SX SoC FPGA SOM, upon these 24 LVDS IOs/48 Single Ended IOs from Stratix® 10 GX/SX SoC FPGA Bank2B, two General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Stratix® 10 GX/SX SoC FPGA SOM, Bank2B I/O voltage is by default set to 1.8V. It can be configured to other supported voltages by controlling the LDO 3 of the PMIC after Boot.

For more details on FPGA Bank2B pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
75	FPGA_LVDS2B_1N_IO47	LVDS2B_1N/ AR21	IO, 1.8V LVDS	Bank2B 1n differential Negative. Same pin can be configured as Single ended I/O.
77	FPGA_LVDS2B_1P_IO46	LVDS2B_1N/ AP21	IO, 1.8V LVDS	Bank2B 1p differential Positive. Same pin can be configured as Single ended I/O.
78	FPGA_LVDS2B_2N_IO45	LVDS2B_2N/ AT20	IO, 1.8V LVDS	Bank2B 2n differential Negative. Same pin can be configured as Single ended I/O.
76	FPGA_LVDS2B_2P_IO44	LVDS2B_2P/ AT21	IO, 1.8V LVDS	Bank2B 2p differential Positive. Same pin can be configured as Single ended I/O.
79	FPGA_LVDS2B_3N_IO43	LVDS2B_3N/ AM22	IO, 1.8V LVDS	Bank2B 3n differential Negative. Same pin can be configured as Single ended I/O.
81	FPGA_LVDS2B_3P_IO42	LVDS2B_3P/ AM23	IO, 1.8V LVDS	Bank2B 3p differential Positive. Same pin can be configured as Single ended I/O.
80	FPGA_LVDS2B_4N_IO41	LVDS2B_4N/ AU20	IO, 1.8V LVDS	Bank2B 4n differential Negative. Same pin can be configured as Single ended I/O.
82	FPGA_LVDS2B_4P_IO40	LVDS2B_4P/ AU19	IO, 1.8V LVDS	Bank2B 4p differential Positive. Same pin can be configured as Single ended I/O.
83	FPGA_LVDS2B_5N_IO39	LVDS2B_5N/ AN21	IO, 1.8V LVDS	Bank2B 5n differential Negative. Same pin can be configured as Single ended I/O.
85	FPGA_LVDS2B_5P_IO38	LVDS2B_5P/ AN22	IO, 1.8V LVDS	Bank2B 5p differential Positive. Same pin can be configured as Single ended I/O.
84	FPGA_LVDS2B_6N_IO37	LVDS2B_6N/ AP20	IO, 1.8V LVDS	Bank2B 6n differential Negative. Same pin can be configured as Single ended I/O.
86	FPGA_LVDS2B_6P_IO36	LVDS2B_6P/ AN20	IO, 1.8V LVDS	Bank2B 6p differential Positive. Same pin can be configured as Single ended I/O.
89	FPGA_LVDS2B_7N_IO35	LVDS2B_7N/ AV20	IO, 1.8V LVDS	Bank2B 7n differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
87	FPGA_LVDS2B_7P_IO34	LVDS2B_7P/ AW20	IO, 1.8V LVDS	Bank2B 7p differential Positive. Same pin can be configured as Single ended I/O.
88	FPGA_LVDS2B_9p_IO30	LVDS2B_9P/ AW21	IO, 1.8V LVDS	Bank2B 9p differential Positive. Same pin can be configured as Single ended I/O.
90	FPGA_LVDS2B_9n_IO31	LVDS2B_9N/ AV21	IO, 1.8V LVDS	Bank2B 9n differential Negative. Same pin can be configured as Single ended I/O.
91	FPGA_LVDS2B_8p_IO32	LVDS2B_8P/ BB20	IO, 1.8V LVDS	Bank2B 8p differential Positive. Same pin can be configured as Single ended I/O.
93	FPGA_LVDS2B_8n_IO33	LVDS2B_8N/ BA20	IO, 1.8V LVDS	Bank2B 8n differential Negative. Same pin can be configured as Single ended I/O.
112	FPGA_LVDS2B_10N/CLKOUT_1N	LVDS2B_10N/ BA19	IO, 1.8V LVDS	Bank2B 10n differential Negative. Same pin can be configured as Clock1 Output differential Negative or Single ended I/O.
110	FPGA_LVDS2B_10P/CLKOUT_1P	LVDS2B_10P/ BB19	IO, 1.8V LVDS	Bank2B 10p differential Positive. Same pin can be configured as Clock1 Output differential Positive or Single ended I/O.
97	FPGA_LVDS2B_11N_IO27	LVDS2B_11N/ AY21	IO, 1.8V LVDS	Bank2B 11n differential Negative. Same pin can be configured as Single ended I/O.
95	FPGA_LVDS2B_11P_IO26	LVDS2B_11P/ BA21	IO, 1.8V LVDS	Bank2B 11p differential Positive. Same pin can be configured as Single ended I/O.
111	FPGA_LVDS2B_12N/CLKIN_1N	LVDS2B_12N/ AW19	IO, 1.8V LVDS	Bank2B 12n differential Negative. Same pin can be configured as Clock1 Input differential Negative or Single ended I/O.
109	FPGA_LVDS2B_12P/CLKIN_1P	LVDS2B_12P/ AY19	IO, 1.8V LVDS	Bank2B 12p differential Positive. Same pin can be configured as Clock1 Input differential Positive or Single ended I/O.
118	FPGA_LVDS2B_13N/CLKIN_0N	LVDS2B_13N/ AR24	IO, 1.8V LVDS	Bank2B 13n differential Negative. Same pin can be configured as Clock0 Input differential Negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
116	FPGA_LVDS2B_13P/CLKIN_0P	LVDS2B_13P/ AR23	IO, 1.8V LVDS	Bank2B 13p differential Positive. Same pin can be configured as Clock0 Input differential Positive or Single ended I/O.
94	FPGA_LVDS2B_14N_IO21	LVDS2B_14N/ AN23	IO, 1.8V LVDS	Bank2B 14n differential Negative. Same pin can be configured as Single ended I/O.
92	FPGA_LVDS2B_14P_IO20	LVDS2B_14P/ AP23	IO, 1.8V LVDS	Bank2B 14p differential Positive. Same pin can be configured as Single ended I/O.
117	FPGA_LVDS2B_15N/CLKOUT_0N	LVDS2B_15N/ AL25	IO, 1.8V LVDS	Bank2B 15n differential Negative. Same pin can be configured as Clock0 Output differential Negative or Single ended I/O.
115	FPGA_LVDS2B_15P/CLKOUT_0P	LVDS2B_15P/ AL26	IO, 1.8V LVDS	Bank2B 15p differential Positive. Same pin can be configured as Clock0 Output differential Positive or Single ended I/O.
96	FPGA_LVDS2B_16N_IO17	LVDS2B_16N/ AM24	IO, 1.8V LVDS	Bank2B 16n differential Negative. Same pin can be configured as Single ended I/O.
98	FPGA_LVDS2B_16P_IO16	LVDS2B_16P/ AL24	IO, 1.8V LVDS	Bank2B 16p differential Positive. Same pin can be configured as Single ended I/O.
101	FPGA_LVDS2B_17N_IO15	LVDS2B_17N/ AP25	IO, 1.8V LVDS	Bank2B 17n differential Negative. Same pin can be configured as Single ended I/O.
99	FPGA_LVDS2B_17P_IO14	LVDS2B_17P/ AP24	IO, 1.8V LVDS	Bank2B 17p differential Positive. Same pin can be configured as Single ended I/O.
102	FPGA_LVDS2B_18N_IO13	LVDS2B_18N/ AN25	IO, 1.8V LVDS	Bank2B 18n differential Negative. Same pin can be configured as Single ended I/O.
100	FPGA_LVDS2B_18P_IO12	LVDS2B_18P/ AM25	IO, 1.8V LVDS	Bank2B 18p differential Positive. Same pin can be configured as Single ended I/O.
105	FPGA_LVDS2B_19N_IO11	LVDS2B_19N/ AW23	IO, 1.8V LVDS	Bank2B 19n differential Negative. Same pin can be configured as Single ended I/O.
103	FPGA_LVDS2B_19P_IO10	LVDS2B_19P/ AY23	IO, 1.8V LVDS	Bank2B 19p differential Positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
106	FPGA_LVDS2B_20N_IO9	LVDS2B_20N/ AV22	IO, 1.8V LVDS	Bank2B 20n differential Negative. Same pin can be configured as Single ended I/O.
104	FPGA_LVDS2B_20P_IO8	LVDS2B_20P/ AU22	IO, 1.8V LVDS	Bank2B 20p differential Positive. Same pin can be configured as Single ended I/O.
121	FPGA_LVDS2B_21N_IO7	LVDS2B_21N/ AU23	IO, 1.8V LVDS	Bank2B 21n differential Negative. Same pin can be configured as Single ended I/O.
123	FPGA_LVDS2B_21P_IO6	LVDS2B_21P/ AV23	IO, 1.8V LVDS	Bank2B 21p differential Positive. Same pin can be configured as Single ended I/O.
124	FPGA_LVDS2B_22N_IO5	LVDS2B_22N/ BB22	IO, 1.8V LVDS	Bank2B 22n differential Negative. Same pin can be configured as Single ended I/O.
122	FPGA_LVDS2B_22P_IO4	LVDS2B_22P/ BB23	IO, 1.8V LVDS	Bank2B 22p differential Positive. Same pin can be configured as Single ended I/O.
125	FPGA_LVDS2B_23N_IO3	LVDS2B_23N/ AR22	IO, 1.8V LVDS	Bank2B 23n differential Negative. Same pin can be configured as Single ended I/O.
127	FPGA_LVDS2B_23P_IO2	LVDS2B_23P/ AT22	IO, 1.8V LVDS	Bank2B 23p differential Positive. Same pin can be configured as Single ended I/O.
128	FPGA_LVDS2B_24N_IO1	LVDS2B_24N/ AY22	IO, 1.8V LVDS	Bank2B 24n differential Negative. Same pin can be configured as Single ended I/O.
126	FPGA_LVDS2B_24P_IO0	LVDS2B_24P/ BA22	IO, 1.8V LVDS	Bank2B 24p differential Positive. Same pin can be configured as Single ended I/O.

2.8.2.3 FPGA IOs & General-Purpose Clocks – Bank2C

The Stratix® 10 GX/SX SoC FPGA SOM supports up to 24 LVDS IOs/48 Single Ended IOs and from Stratix® 10 GX/SX FPGA Bank2C on Board-to-Board connector2. In Stratix® 10 SoC/FPGA SOM, Bank2C signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank2B signals are routed as LVDS IOs, these pins can be used as SE IOs if required. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Stratix® 10 GX/SX SoC FPGA SOM, upon these 24 LVDS IOs/48 Single Ended IOs from Stratix® 10 GX/SX SoC FPGA Bank2C, two General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Stratix® 10 GX/SX SoC FPGA SOM, Bank2C I/O voltage is by default set to 1.8V. It can be configured to other supported voltages by controlling the LDO4 of the PMIC after Boot.

For more details on FPGA Bank2C pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
133	FPGA_LVDS2C_1N_IO47	LVDS2C_1N/ AN17	IO, 1.8V LVDS	Bank2C 1n differential Negative. Same pin can be configured as Single ended I/O.
131	FPGA_LVDS2C_1P_IO46	LVDS2C_1P/ AM17	IO, 1.8V LVDS	Bank2C 1p differential Positive. Same pin can be configured as Single ended I/O.
134	FPGA_LVDS2C_2N_IO45	LVDS2C_2N/ AK18	IO, 1.8V LVDS	Bank2C 2n differential Negative. Same pin can be configured as Single ended I/O.
132	FPGA_LVDS2C_2P_IO44	LVDS2C_2P/ AJ19	IO, 1.8V LVDS	Bank2C 2p differential Positive. Same pin can be configured as Single ended I/O.
137	FPGA_LVDS2C_3N_IO43	LVDS2C_3N/ AL19	IO, 1.8V LVDS	Bank2C 3n differential Negative. Same pin can be configured as Single ended I/O.
135	FPGA_LVDS2C_3P_IO42	LVDS2C_3P/ AK19	IO, 1.8V LVDS	Bank2C 3p differential Positive. Same pin can be configured as Single ended I/O.
138	FPGA_LVDS2C_4N_IO41	LVDS2C_4N/ AJ18	IO, 1.8V LVDS	Bank2C 4n differential Negative. Same pin can be configured as Single ended I/O.
136	FPGA_LVDS2C_4P_IO40	LVDS2C_4P/ AH18	IO, 1.8V LVDS	Bank2C 4p differential Positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
141	FPGA_LVDS2C_5N_IO39	LVDS2C_5N/ AM20	IO, 1.8V LVDS	Bank2C 5n differential Negative. Same pin can be configured as Single ended I/O.
139	FPGA_LVDS2C_5P_IO38	LVDS2C_5P/ AM19	IO, 1.8V LVDS	Bank2C 5p differential Positive. Same pin can be configured as Single ended I/O.
142	FPGA_LVDS2C_6N_IO37	LVDS2C_6N/ AK17	IO, 1.8V LVDS	Bank2C 6n differential Negative. Same pin can be configured as Single ended I/O.
140	FPGA_LVDS2C_6P_IO36	LVDS2C_6P/ AL17	IO, 1.8V LVDS	Bank2C 6p differential Positive. Same pin can be configured as Single ended I/O.
143	FPGA_LVDS2C_7N_IO35	LVDS2C_7N/ AH24	IO, 1.8V LVDS	Bank2C 7n differential Negative. Same pin can be configured as Single ended I/O.
145	FPGA_LVDS2C_7P_IO34	LVDS2C_7P/ AJ23	IO, 1.8V LVDS	Bank2C 7p differential Positive. Same pin can be configured as Single ended I/O.
146	FPGA_LVDS2C_8N_IO33	LVDS2C_8N/ AK24	IO, 1.8V LVDS	Bank2C 8n differential Negative. Same pin can be configured as Single ended I/O.
144	FPGA_LVDS2C_8P_IO32	LVDS2C_8P/ AJ24	IO, 1.8V LVDS	Bank2C 8p differential Positive. Same pin can be configured as Single ended I/O.
149	FPGA_LVDS2C_9N_IO31	LVDS2C_9N/ AL21	IO, 1.8V LVDS	Bank2C 9n differential Negative. Same pin can be configured as Single ended I/O.
147	FPGA_LVDS2C_9P_IO30	LVDS2C_9P/ AL20	IO, 1.8V LVDS	Bank2C 9p differential Positive. Same pin can be configured as Single ended I/O.
172	FPGA_LVDS2C_10N/CLKOUT_1N	LVDS2C_10N/ AK21	IO, 1.8V LVDS	Bank2C 10n differential Negative. Same pin can be configured as Clock1 Output differential Negative or Single ended I/O.
170	FPGA_LVDS2C_10P/CLKOUT_1P	LVDS2C_10P/ AK22	IO, 1.8V LVDS	Bank2C 10p differential Positive. Same pin can be configured as Clock1 Output differential Positive or Single ended I/O.
153	FPGA_LVDS2C_11N_IO27	LVDS2C_11N/ AL22	IO, 1.8V LVDS	Bank2C 11n differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
151	FPGA_LVDS2C_11P_IO26	LVDS2C_11P/ AK23	IO, 1.8V LVDS	Bank2C 11p differential Positive. Same pin can be configured as Single ended I/O.
177	FPGA_LVDS2C_12N/CLKIN_1N	LVDS2C_12N/ AJ25	IO, 1.8V LVDS	Bank2C 12n differential Negative. Same pin can be configured as Clock1 Input differential Negative or Single ended I/O.
175	FPGA_LVDS2C_12P/CLKIN_1P	LVDS2C_12P/ AJ26	IO, 1.8V LVDS	Bank2C 12p differential Positive. Same pin can be configured as Clock1 Input differential Positive or Single ended I/O.
178	FPGA_LVDS2C_13N/CLKIN_0N	LVDS2C_13N/ AP18	IO, 1.8V LVDS	Bank2C 13n differential Negative. Same pin can be configured as Clock0 Input differential Negative or Single ended I/O.
176	FPGA_LVDS2C_13P/CLKIN_0P	LVDS2C_13P/ AP19	IO, 1.8V LVDS	Bank2C 13p differential Positive. Same pin can be configured as Clock0 Input differential Positive or Single ended I/O.
150	FPGA_LVDS2C_14N_IO21	LVDS2C_14N/ AR17	IO, 1.8V LVDS	Bank2C 14n differential Negative. Same pin can be configured as Single ended I/O.
148	FPGA_LVDS2C_14P_IO20	LVDS2C_14P/ AR18	IO, 1.8V LVDS	Bank2C 14p differential Positive. Same pin can be configured as Single ended I/O.
171	FPGA_LVDS2C_15N/CLKOUT_0N	LVDS2C_15N/ AT19	IO, 1.8V LVDS	Bank2C 15n differential Negative. Same pin can be configured as Clock0 Output differential Negative or Single ended I/O.
169	FPGA_LVDS2C_15P/CLKOUT_0P	LVDS2C_15P/ AR19	IO, 1.8V LVDS	Bank2C 15p differential Positive. Same pin can be configured as Clock0 Output differential Positive or Single ended I/O.
154	FPGA_LVDS2C_16N_IO17	LVDS2C_16N/ AN18	IO, 1.8V LVDS	Bank2C 16n differential Negative. Same pin can be configured as Single ended I/O.
152	FPGA_LVDS2C_16P_IO16	LVDS2C_16P/ AM18	IO, 1.8V LVDS	Bank2C 16p differential Positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
157	FPGA_LVDS2C_17N_IO15	LVDS2C_17N/ AR16	IO, 1.8V LVDS	Bank2C 17n differential Negative. Same pin can be configured as Single ended I/O.
155	FPGA_LVDS2C_17P_IO14	LVDS2C_17P/ AT16	IO, 1.8V LVDS	Bank2C 17p differential Positive. Same pin can be configured as Single ended I/O.
158	FPGA_LVDS2C_18N_IO13	LVDS2C_18N/ AT17	IO, 1.8V LVDS	Bank2C 18n differential Negative. Same pin can be configured as Single ended I/O.
156	FPGA_LVDS2C_18P_IO12	LVDS2C_18P/ AU17	IO, 1.8V LVDS	Bank2C 18p differential Positive. Same pin can be configured as Single ended I/O.
161	FPGA_LVDS2C_19N_IO11	LVDS2C_19N/ AY18	IO, 1.8V LVDS	Bank2C 19n differential Negative. Same pin can be configured as Single ended I/O.
159	FPGA_LVDS2C_19P_IO10	LVDS2C_19P/ AW18	IO, 1.8V LVDS	Bank2C 19p differential Positive. Same pin can be configured as Single ended I/O.
160	FPGA_LVDS2C_20N_IO9	LVDS2C_20N/ AV17	IO, 1.8V LVDS	Bank2C 20n differential Negative. Same pin can be configured as Single ended I/O.
162	FPGA_LVDS2C_20P_IO8	LVDS2C_20P/ AV16	IO, 1.8V LVDS	Bank2C 20p differential Positive. Same pin can be configured as Single ended I/O.
165	FPGA_LVDS2C_21N_IO7	LVDS2C_21N/ AV18	IO, 1.8V LVDS	Bank2C 21n differential Negative. Same pin can be configured as Single ended I/O.
163	FPGA_LVDS2C_21P_IO6	LVDS2C_21P/ AU18	IO, 1.8V LVDS	Bank2C 21p differential Positive. Same pin can be configured as Single ended I/O.
166	FPGA_LVDS2C_22N_IO5	LVDS2C_22N/ BB17	IO, 1.8V LVDS	Bank2C 22n differential Negative. Same pin can be configured as Single ended I/O.
164	FPGA_LVDS2C_22P_IO4	LVDS2C_22P/ BB18	IO, 1.8V LVDS	Bank2C 22p differential Positive. Same pin can be configured as Single ended I/O.
181	FPGA_LVDS2C_23N_IO3	LVDS2C_23N/ AW16	IO, 1.8V LVDS	Bank2C 23n differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
183	FPGA_LVDS2C_23P_IO2	LVDS2C_23P/ AY16	IO, 1.8V LVDS	Bank2C 23p differential Positive. Same pin can be configured as Single ended I/O.
184	FPGA_LVDS2C_24N_IO1	LVDS2C_24N/ BA17	IO, 1.8V LVDS	Bank2C 24n differential Negative. Same pin can be configured as Single ended I/O.
182	FPGA_LVDS2C_24P_IO0	LVDS2C_24P/ AY17	IO, 1.8V LVDS	Bank2C 24p differential Positive. Same pin can be configured as Single ended I/O.

2.8.3 Power & Reset Input

The Stratix® 10 GX/SX SoC FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin232) in Board-to-Board Connector1. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Stratix® 10 GX/SX SoC FPGA SOM supports VCC_RTC coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage. Also, it supports warm reset input from Board-to-Board Connector2 and connected to SDM_HPS_COLD_nRESET(BA9) pin of Stratix® 10 GX/SX SDM Bank.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B-2 Signal Name	CPU Ball Name/ Pin Name	Signal Type/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	I, 5V Power	Supply Voltage.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	Power	Ground.
68	VRTC_3V0	NA	I, 3V Power	3V backup coin cell input for RTC.
35	RESET_SW_IN	SDM_HPS_COLD_nRESET / BA9	I, 1.8V LVCMOS/ 10K PU	Active low reset input.

2.9 Board to Board Connector3

The Stratix® 10 GX/SX SoC FPGA SOM Board to Board connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A from Samtech

Staking Height - 5mm

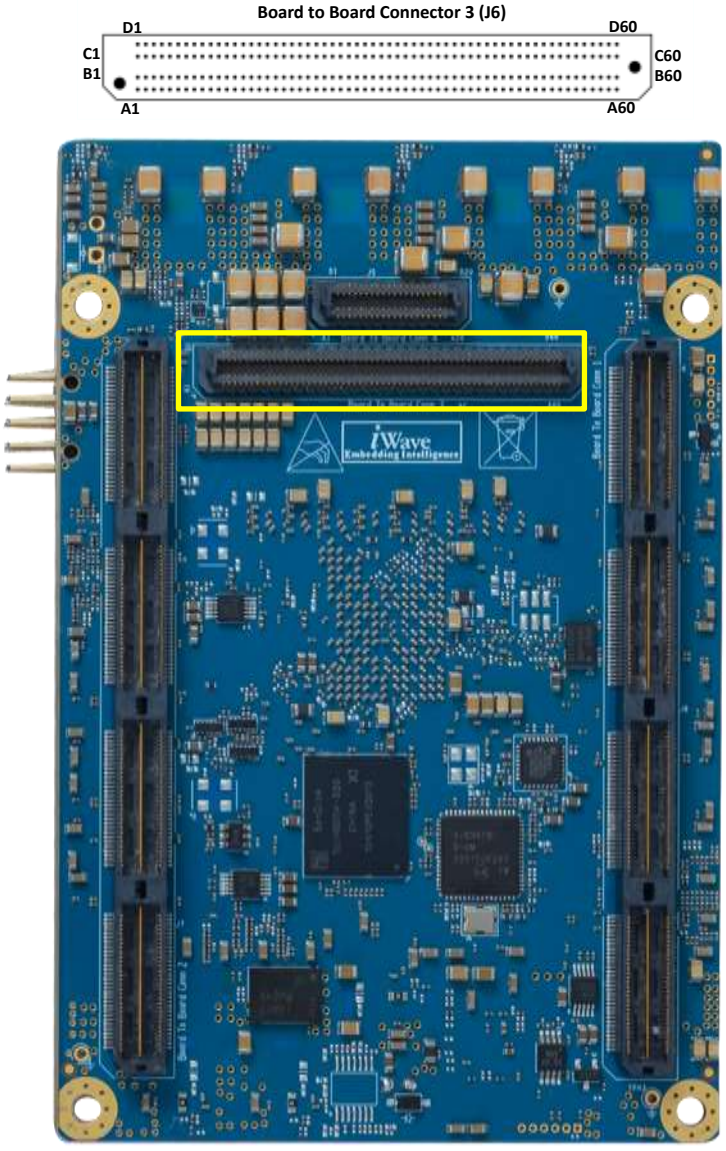


Figure 8: Board to Board Connector3

Table 12: Board to Board Connector3 Pinout

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A1	CLKGEN_REFIN_N	**B1**	GND	**C1**	NC	**D1**	GND
A2	CLKGEN_REFIN_P	**B2**	GXBL1D_RX_CH3 N	**C2**	GND	**D2**	REFCLK_GXBL1L_ CHBP
A3	GND	**B3**	GXBL1D_RX_CH3 P	**C3**	GND	**D3**	REFCLK_GXBL1L_ CHBN
A4	GXBL1D_RX_CH0 N	**B4**	GND	**C4**	GXBL1N_RX_CH3 P	**D4**	GND
A5	GXBL1D_RX_CH0 P	**B5**	GND	**C5**	GXBL1N_RX_CH3 N	**D5**	GND
A6	GND	**B6**	GXBL1D_RX_CH4 N	**C6**	GND	**D6**	GXBL1N_RX_CH2 P
A7	GND	**B7**	GXBL1D_RX_CH4 P	**C7**	GND	**D7**	GXBL1N_RX_CH2 N
A8	GXBL1D_RX_CH1 N	**B8**	GND	**C8**	GXBL1N_RX_CH0 N	**D8**	GND
A9	GXBL1D_RX_CH1 P	**B9**	GND	**C9**	GXBL1N_RX_CH0 P	**D9**	GND
A10	GND	**B10**	GXBL1D_TX_CH1 N	**C10**	GND	**D10**	GXBL1F_RX_CH2P
A11	GND	**B11**	GXBL1D_TX_CH1 P	**C11**	GND	**D11**	GXBL1F_RX_CH2 N
A12	GXBL1D_TX_CH4 N	**B12**	GND	**C12**	GXBL1N_TX_CH1 N	**D12**	GND
A13	GXBL1D_TX_CH4 P	**B13**	GND	**C13**	GXBL1N_TX_CH1 P	**D13**	GND
A14	GND	**B14**	GXBL1D_TX_CH0 N	**C14**	GND	**D14**	GXBL1L_RX_CH2P
A15	GND	**B15**	GXBL1D_TX_CH0 P	**C15**	GND	**D15**	GXBL1L_RX_CH2 N
A16	GXBL1D_TX_CH3 N	**B16**	GND	**C16**	REFCLK_GXBL1N_ CHBN	**D16**	GND
A17	GXBL1D_TX_CH3 P	**B17**	GND	**C17**	REFCLK_GXBL1N_ CHBP	**D17**	GND
A18	GND	**B18**	REFCLK_GXBL1D_ CHTN	**C18**	GND	**D18**	GXBL1D_RX_CH2 P
A19	GND	**B19**	REFCLK_GXBL1D_ CHTP	**C19**	GND	**D19**	GXBL1D_RX_CH2 N
A20	NC	**B20**	GND	**C20**	REFCLK_GXBL1N_ CHTP	**D20**	GND
A21	NC	**B21**	GND	**C21**	REFCLK_GXBL1N_ CHTN	**D21**	GND

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A22	GND	B22	GXBL1F_RX_CH4N	C22	GND	D22	GXBL1N_TX_CH2N
A23	GND	B23	GXBL1F_RX_CH4P	C23	GND	D23	GXBL1N_TX_CH2P
A24	GXBL1F_RX_CH3N	B24	GND	C24	GXBL1N_RX_CH4N	D24	GND
A25	GXBL1F_RX_CH3P	B25	GND	C25	GXBL1N_RX_CH4P	D25	GND
A26	GND	B26	GXBL1F_TX_CH4P	C26	GND	D26	GXBL1F_TX_CH2N
A27	GND	B27	GXBL1F_TX_CH4N	C27	GND	D27	GXBL1F_TX_CH2P
A28	GXBL1F_TX_CH3P	B28	GND	C28	GXBL1N_RX_CH1N	D28	GND
A29	GXBL1F_TX_CH3N	B29	GND	C29	GXBL1N_RX_CH1P	D29	GND
A30	GND	B30	GXBL1F_TX_CH1P	C30	GND	D30	GXBL1L_TX_CH2N
A31	GND	B31	GXBL1F_TX_CH1N	C31	GND	D31	GXBL1L_TX_CH2P
A32	GXBL1F_TX_CH0P	B32	GND	C32	GXBL1N_TX_CH4N	D32	GND
A33	GXBL1F_TX_CH0N	B33	GND	C33	GXBL1N_TX_CH4P	D33	GND
A34	GND	B34	REFCLK_GXBL1F_CHBP	C34	GND	D34	GXBL1D_TX_CH2N
A35	GND	B35	REFCLK_GXBL1F_CHBN	C35	GND	D35	GXBL1D_TX_CH2P
A36	GXBL1F_RX_CH1P	B36	GND	C36	GXBL1N_TX_CH3N	D36	GND
A37	GXBL1F_RX_CH1N	B37	GND	C37	GXBL1N_TX_CH3P	D37	GND
A38	GND	B38	REFCLK_GXBL1F_CHTP	C38	GND	D38	NC
A39	GND	B39	REFCLK_GXBL1F_CHTN	C39	GND	D39	NC
A40	GXBL1F_RX_CH0P	B40	GND	C40	GXBL1N_TX_CH0N	D40	GND
A41	GXBL1F_RX_CH0N	B41	GND	C41	GXBL1N_TX_CH0P	D41	GND
A42	GND	B42	REFCLK_GXBL1D_CHBP	C42	GND	D42	GXBL1L_RX_CH1N
A43	GND	B43	REFCLK_GXBL1D_CHBN	C43	GND	D43	GXBL1L_RX_CH1P
A44	GXBL1D_TX_CH5P	B44	GND	C44	GXBL1L_RX_CH3N	D44	GND

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A45	GXBL1D_TX_CH5N	**B45**	GND	**C45**	GXBL1L_RX_CH3P	**D45**	GND
A46	GND	**B46**	GXBL1L_TX_CH5P	**C46**	GND	**D46**	GXBL1L_RX_CH4N
A47	GND	**B47**	GXBL1L_TX_CH5N	**C47**	GND	**D47**	GXBL1L_RX_CH4P
A48	GXBL1N_TX_CH5P	**B48**	GND	**C48**	REFCLK_GXBL1L_CHTP	**D48**	GND
A49	GXBL1N_TX_CH5N	**B49**	GND	**C49**	REFCLK_GXBL1L_CHTN	**D49**	GND
A50	GND	**B50**	GXBL1D_RX_CH5P	**C50**	GND	**D50**	GXBL1L_RX_CH0N
A51	GND	**B51**	GXBL1D_RX_CH5N	**C51**	GND	**D51**	GXBL1L_RX_CH0P
A52	GXBL1F_TX_CH5P	**B52**	GND	**C52**	GXBL1L_TX_CH0P	**D52**	GND
A53	GXBL1F_TX_CH5N	**B53**	GND	**C53**	GXBL1L_TX_CH0N	**D53**	GND
A54	GND	**B54**	GXBL1F_RX_CH5P	**C54**	GND	**D54**	GXBL1L_TX_CH3P
A55	GND	**B55**	GXBL1F_RX_CH5N	**C55**	GND	**D55**	GXBL1L_TX_CH3N
A56	GXBL1L_RX_CH5P	**B56**	GND	**C56**	GXBL1L_TX_CH1N	**D56**	GND
A57	GXBL1L_RX_CH5N	**B57**	GND	**C57**	GXBL1L_TX_CH1P	**D57**	GND
A58	GND	**B58**	GXBL1N_RX_CH5P	**C58**	GND	**D58**	GXBL1L_TX_CH4P
A59	NC	**B59**	GXBL1N_RX_CH5N	**C59**	GND	**D59**	GXBL1L_TX_CH4N
A60	NC	**B60**	GND	**C60**	NC	**D60**	GND

2.9.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Stratix® 10 GX/SX SoC FPGA 's FPGA is explained in the following section.

2.9.1.1 Transceivers FPGA High Speed Transceivers

The Stratix® 10 GX/SX SoC FPGA SOM supports 24 high speed transceiver channels (6 from 1D bank, 6 from 1L bank, 6 from Bank 1F & 6 from 1N bank) on Board-to-Board connector1. In Stratix® 10 GX/SX SoC FPGA SOM, Transceiver power to the SoC FPGA is fixed to 1.12V. The Transceivers connected to Board-to-Board Connector3 is capable of running up to a maximum speed of 28.3Gbps (For GXT Transceivers). These transceivers can be used to interface to multiple high-speed interface protocols. Each 6 Channel Transceiver Bank supports two dedicated reference clock input pairs.

For more details on Transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-1D Channels				
A4	GXBL1D_RX_CH0N	GXBL1D_RX_CH0N/ AU35	I, DIFF	Bank1D channel0 High speed differential receiver Negative
A5	GXBL1D_RX_CH0P	GXBL1D_RX_CH0P/ AU36	I, DIFF	Bank1D channel0 High speed differential receiver Positive.
B14	GXBL1D_TX_CH0N	GXBL1D_TX_CH0N/ AW39	O, DIFF	Bank1D channel0 High speed differential transmitter Negative.
B15	GXBL1D_TX_CH0P	GXBL1D_TX_CH0P/ AW40	O, DIFF	Bank1D channel0 High speed differential transmitter Positive.
A8	GXBL1D_RX_CH1N	GXBL1D_RX_CH1N/ AW35	I, DIFF	Bank1D channel1 High speed differential receiver Negative.
A9	GXBL1D_RX_CH1P	GXBL1D_RX_CH1P/ AW36	I, DIFF	Bank1D channel1 High speed differential receiver Positive.
B10	GXBL1D_TX_CH1N	GXBL1D_TX_CH1N/ AV41	O, DIFF	Bank1D channel1 High speed differential transmitter Negative.
B11	GXBL1D_TX_CH1P	GXBL1D_TX_CH1P/ AV42	O, DIFF	Bank1D channel1 High speed differential transmitter Positive.
D19	GXBL1D_RX_CH2N	GXBL1D_RX_CH2N/ AR35	I, DIFF	Bank1D channel2 High speed differential receiver Negative.
D18	GXBL1D_RX_CH2P	GXBL1D_RX_CH2P/ AR36	I, DIFF	Bank1D channel2 High speed differential receiver Positive.
D34	GXBL1D_TX_CH2N	GXBL1D_TX_CH2N/ AU39	O, DIFF	Bank1D channel2 High speed differential transmitter Negative.
D35	GXBL1D_TX_CH2P	GXBL1D_TX_CH2P/ AU40	O, DIFF	Bank1D channel2 High speed differential transmitter Positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B2	GXBL1D_RX_CH3N	GXBL1D_RX_CH3N/ AN35	I, DIFF	Bank1D channel3 High speed differential receiver Negative.
B3	GXBL1D_RX_CH3P	GXBL1D_RX_CH3P/ AN36	I, DIFF	Bank1D channel3 High speed differential receiver Positive.
A16	GXBL1D_TX_CH3N	GXBL1D_TX_CH3N/ AT41	O, DIFF	Bank1D channel3 High speed differential transmitter Negative.
A17	GXBL1D_TX_CH3P	GXBL1D_TX_CH3P/ AT42	O, DIFF	Bank1D channel3 High speed differential transmitter Positive.
B6	GXBL1D_RX_CH4N	GXBL1D_RX_CH4N/ AT37	I, DIFF	Bank1D channel4 High speed differential receiver Negative.
B7	GXBL1D_RX_CH4P	GXBL1D_RX_CH4P/ AT38	I, DIFF	Bank1D channel4 High speed differential receiver Positive.
A12	GXBL1D_TX_CH4N	GXBL1D_TX_CH4N/ AR39	O, DIFF	Bank1D channel4 High speed differential transmitter Negative.
A13	GXBL1D_TX_CH4P	GXBL1D_TX_CH4P/ AR40	O, DIFF	Bank1D channel4 High speed differential transmitter Positive.
B51	GXBL1D_RX_CH5N	GXBL1D_RX_CH5N/ AP37	I, DIFF	Bank1D channel5 High speed differential receiver Negative.
B50	GXBL1D_RX_CH5P	GXBL1D_RX_CH5P/ AP38	I, DIFF	Bank1D channel5 High speed differential receiver Positive.
A45	GXBL1D_TX_CH5N	GXBL1D_TX_CH5N/ AP41	O, DIFF	Bank1D channel5 High speed differential transmitter Negative.
A44	GXBL1D_TX_CH5P	GXBL1D_TX_CH5P/ AP42	O, DIFF	Bank1D channel5 High speed differential transmitter Positive.
B43	REFCLK_GXBL1D_CHBN	REFCLK_GXBL1D_CHBN/ AP33	I, DIFF	Bank1D differential Bottom reference clock Negative.
B42	REFCLK_GXBL1D_CHBP	REFCLK_GXBL1D_CHBP/ AP34	I, DIFF	Bank1D differential Bottom reference clock Positive.
B18	REFCLK_GXBL1D_CHTN	REFCLK_GXBL1D_CHTN/ AM33	I, DIFF	Bank1D differential Top reference clock Negative.
B19	REFCLK_GXBL1D_CHTP	REFCLK_GXBL1D_CHTP/ AM34	I, DIFF	Bank1D differential Top reference clock Positive.
BANK-1F Channels				
A41	GXBL1F_RX_CH0N	GXBL1F_RX_CH0N/ AG35	I, DIFF	Bank1F channel0 High speed differential receiver Negative.
A40	GXBL1F_RX_CH0P	GXBL1F_RX_CH0P/ AG36	I, DIFF	Bank1F channel0 High speed differential receiver Positive.
A33	GXBL1F_TX_CH0N	GXBL1F_TX_CH0N/ AG39	O, DIFF	Bank1F channel0 High speed differential transmitter Negative.
A32	GXBL1F_TX_CH0P	GXBL1F_TX_CH0P/ AG40	O, DIFF	Bank1F channel0 High speed differential transmitter Positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A37	GXBL1F_RX_CH1N	GXBL1F_RX_CH1N/ AD37	I, DIFF	Bank1F channel1 High speed differential receiver Negative.
A36	GXBL1F_RX_CH1P	GXBL1F_RX_CH1P/ AD38	I, DIFF	Bank1F channel1 High speed differential receiver Positive.
B31	GXBL1F_TX_CH1N	GXBL1F_TX_CH1N/ AF41	O, DIFF	Bank1F channel1 High speed differential transmitter Negative.
B30	GXBL1F_TX_CH1P	GXBL1F_TX_CH1P/ AF42	O, DIFF	Bank1F channel1 High speed differential transmitter Positive.
D11	GXBL1F_RX_CH2N	GXBL1F_RX_CH2N/ AE35	I, DIFF	Bank1F channel2 High speed differential receiver Negative.
D10	GXBL1F_RX_CH2P	GXBL1F_RX_CH2P/ AE36	I, DIFF	Bank1F channel2 High speed differential receiver Positive.
D26	GXBL1F_TX_CH2N	GXBL1F_TX_CH2N/ AE39	O, DIFF	Bank1F channel2 High speed differential transmitter Negative.
D27	GXBL1F_TX_CH2P	GXBL1F_TX_CH2P/ AE40	O, DIFF	Bank1F channel2 High speed differential transmitter Positive.
A24	GXBL1F_RX_CH3N	GXBL1F_RX_CH3N/ AB37	I, DIFF	Bank1F channel3 High speed differential receiver Negative.
A25	GXBL1F_RX_CH3P	GXBL1F_RX_CH3P/ AB38	I, DIFF	Bank1F channel3 High speed differential receiver Positive.
A29	GXBL1F_TX_CH3N	GXBL1F_TX_CH3N/ AD41	O, DIFF	Bank1F channel3 High speed differential transmitter Negative.
A28	GXBL1F_TX_CH3P	GXBL1F_TX_CH3P/ AD42	O, DIFF	Bank1F channel3 High speed differential transmitter Positive.
B22	GXBL1F_RX_CH4N	GXBL1F_RX_CH4N/ AC35	I, DIFF	Bank1F channel4 High speed differential receiver Negative.
B23	GXBL1F_RX_CH4P	GXBL1F_RX_CH4P/ AC36	I, DIFF	Bank1F channel4 High speed differential receiver Positive.
B27	GXBL1F_TX_CH4N	GXBL1F_TX_CH4N/ AC39	O, DIFF	Bank1F channel4 High speed differential transmitter Negative.
B26	GXBL1F_TX_CH4P	GXBL1F_TX_CH4P/ AC40	O, DIFF	Bank1F channel4 High speed differential transmitter Positive.
B55	GXBL1F_RX_CH5N	GXBL1F_RX_CH5N/ AA35	I, DIFF	Bank1F channel5 High speed differential receiver Negative.
B54	GXBL1F_RX_CH5P	GXBL1F_RX_CH5P/ AA36	I, DIFF	Bank1F channel5 High speed differential receiver Positive.
A53	GXBL1F_TX_CH5N	GXBL1F_TX_CH5N/ AB41	O, DIFF	Bank1F channel5 High speed differential transmitter Negative.
A52	GXBL1F_TX_CH5P	GXBL1F_TX_CH5P/ AB42	O, DIFF	Bank1F channel5 High speed differential transmitter Positive.
B35	REFCLK_GXBL1F_CHBN	REFCLK_GXBL1F_CHBN/ AF33	I, DIFF	Bank1F differential Bottom reference clock Negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
B34	REFCLK_GXBL1F_CHBP	REFCLK_GXBL1F_CHBP/ AF34	I, DIFF	Bank1F differential Bottom reference clock Positive.
B39	REFCLK_GXBL1F_CHTN	REFCLK_GXBL1F_CHTN/ AD33	I, DIFF	Bank1F differential Top reference clock Negative.
B38	REFCLK_GXBL1F_CHTP	REFCLK_GXBL1F_CHTP/ AD34	I, DIFF	Bank1F differential Top reference clock Positive.
BANK-1L Channels				
D50	GXBL1L_RX_CH0N	GXBL1L_RX_CH0N/ P37	I, DIFF	Bank1L channel0 High speed differential receiver Negative.
D51	GXBL1L_RX_CH0P	GXBL1L_RX_CH0P/ P38	I, DIFF	Bank1L channel0 High speed differential receiver Positive.
C53	GXBL1L_TX_CH0N	GXBL1L_TX_CH0N/ R39	O, DIFF	Bank1L channel0 High speed differential transmitter Negative.
C52	GXBL1L_TX_CH0P	GXBL1L_TX_CH0P/ R40	O, DIFF	Bank1L channel0 High speed differential transmitter Positive.
D42	GXBL1L_RX_CH1N	GXBL1L_RX_CH1N/ N35	I, DIFF	Bank1L channel1 High speed differential receiver Negative.
D43	GXBL1L_RX_CH1P	GXBL1L_RX_CH1P/ N36	I, DIFF	Bank1L channel1 High speed differential receiver Positive.
C56	GXBL1L_TX_CH1N	GXBL1L_TX_CH1N/ P41	O, DIFF	Bank1L channel1 High speed differential transmitter Negative.
C57	GXBL1L_TX_CH1P	GXBL1L_TX_CH1P/ P42	O, DIFF	Bank1L channel1 High speed differential transmitter Positive.
D15	GXBL1L_RX_CH2N	GXBL1L_RX_CH2N/ M37	I, DIFF	Bank1L channel2 High speed differential receiver Negative.
D14	GXBL1L_RX_CH2P	GXBL1L_RX_CH2P/ M38	I, DIFF	Bank1L channel2 High speed differential receiver Positive.
D30	GXBL1L_TX_CH2N	GXBL1L_TX_CH2N/ N39	O, DIFF	Bank1L channel2 High speed differential transmitter Negative.
D31	GXBL1L_TX_CH2P	GXBL1L_TX_CH2P/ N40	O, DIFF	Bank1L channel2 High speed differential transmitter Positive.
C44	GXBL1L_RX_CH3N	GXBL1L_RX_CH3N/ K37	I, DIFF	Bank1L channel3 High speed differential receiver Negative.
C45	GXBL1L_RX_CH3P	GXBL1L_RX_CH3P/ K38	I, DIFF	Bank1L channel3 High speed differential receiver Positive.
D55	GXBL1L_TX_CH3N	GXBL1L_TX_CH3N/ M41	O, DIFF	Bank1L channel3 High speed differential transmitter Negative.
D54	GXBL1L_TX_CH3P	GXBL1L_TX_CH3P/ M42	O, DIFF	Bank1L channel3 High speed differential transmitter Positive.
D46	GXBL1L_RX_CH4N	GXBL1L_RX_CH4N/ L35	I, DIFF	Bank1L channel4 High speed differential receiver Negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D47	GXBL1L_RX_CH4P	GXBL1L_RX_CH4P/ L36	I, DIFF	Bank1L channel4 High speed differential receiver Positive.
D59	GXBL1L_TX_CH4N	GXBL1L_TX_CH4N/ L39	O, DIFF	Bank1L channel4 High speed differential transmitter Negative.
D58	GXBL1L_TX_CH4P	GXBL1L_TX_CH4P/ L40	O, DIFF	Bank1L channel4 High speed differential transmitter Positive.
A57	GXBL1L_RX_CH5N	GXBL1L_RX_CH5N/ H37	I, DIFF	Bank1L channel5 High speed differential receiver Negative.
A56	GXBL1L_RX_CH5P	GXBL1L_RX_CH5P/ H38	I, DIFF	Bank1L channel5 High speed differential receiver Positive.
B47	GXBL1L_TX_CH5N	GXBL1L_TX_CH5N/ K41	O, DIFF	Bank1L channel5 High speed differential transmitter Negative.
B46	GXBL1L_TX_CH5P	GXBL1L_TX_CH5P/ K42	O, DIFF	Bank1L channel5 High speed differential transmitter Positive.
D3	REFCLK_GXBL1L_CHBN	REFCLK_GXBL1L_CHBN/ V33	I, DIFF	Bank1L differential Bottom reference clock Negative.
D2	REFCLK_GXBL1L_CHBP	REFCLK_GXBL1L_CHBP/ V34	I, DIFF	Bank1L differential Bottom reference clock Positive.
C49	REFCLK_GXBL1L_CHTN	REFCLK_GXBL1L_CHTN/ T33	I, DIFF	Bank1L differential Top reference clock Negative.
C48	REFCLK_GXBL1L_CHTP	REFCLK_GXBL1L_CHTP/ T34	I, DIFF	Bank1L differential Top reference clock Positive.
BANK-1N Channels				
C8	GXBL1N_RX_CH0N	GXBL1N_RX_CH0N/ C31	I, DIFF	Bank1N channel0 High speed differential receiver Negative.
C9	GXBL1N_RX_CH0P	GXBL1N_RX_CH0P/ C32	I, DIFF	Bank1N channel0 High speed differential receiver Positive.
C28	GXBL1N_RX_CH1N	GXBL1N_RX_CH1N/ B29	O, DIFF	Bank1N channel0 High speed differential transmitter Negative.
C29	GXBL1N_RX_CH1P	GXBL1N_RX_CH1P/ B30	O, DIFF	Bank1N channel0 High speed differential transmitter Positive.
D7	GXBL1N_RX_CH2N	GXBL1N_RX_CH2N/ E31	I, DIFF	Bank1N channel1 High speed differential receiver Negative.
D6	GXBL1N_RX_CH2P	GXBL1N_RX_CH2P/ E32	I, DIFF	Bank1N channel1 High speed differential receiver Positive.
C5	GXBL1N_RX_CH3N	GXBL1N_RX_CH3N/ A27	O, DIFF	Bank1N channel1 High speed differential transmitter Negative.
C4	GXBL1N_RX_CH3P	GXBL1N_RX_CH3P/ A28	O, DIFF	Bank1N channel1 High speed differential transmitter Positive.
C24	GXBL1N_RX_CH4N	GXBL1N_RX_CH4N/ D29	I, DIFF	Bank1N channel2 High speed differential receiver Negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C25	GXBL1N_RX_CH4P	GXBL1N_RX_CH4P/ D30	I, DIFF	Bank1N channel2 High speed differential receiver Positive.
B59	GXBL1N_RX_CH5N	GXBL1N_RX_CH5N/ F29	O, DIFF	Bank1N channel2 High speed differential transmitter Negative.
B58	GXBL1N_RX_CH5P	GXBL1N_RX_CH5P/ F30	O, DIFF	Bank1N channel2 High speed differential transmitter Positive.
C40	GXBL1N_TX_CH0N	GXBL1N_TX_CH0N/ F37	I, DIFF	Bank1N channel3 High speed differential receiver Negative.
C41	GXBL1N_TX_CH0P	GXBL1N_TX_CH0P/ F38	I, DIFF	Bank1N channel3 High speed differential receiver Positive.
C12	GXBL1N_TX_CH1N	GXBL1N_TX_CH1N/ C39	O, DIFF	Bank1N channel3 High speed differential transmitter Negative.
C13	GXBL1N_TX_CH1P	GXBL1N_TX_CH1P/ C40	O, DIFF	Bank1N channel3 High speed differential transmitter Positive.
D22	GXBL1N_TX_CH2N	GXBL1N_TX_CH2N/ D37	I, DIFF	Bank1N channel4 High speed differential receiver Negative.
D23	GXBL1N_TX_CH2P	GXBL1N_TX_CH2P/ D38	I, DIFF	Bank1N channel4 High speed differential receiver Positive.
C36	GXBL1N_TX_CH3N	GXBL1N_TX_CH3N/ B37	O, DIFF	Bank1N channel4 High speed differential transmitter Negative.
C37	GXBL1N_TX_CH3P	GXBL1N_TX_CH3P/ B38	O, DIFF	Bank1N channel4 High speed differential transmitter Positive.
C32	GXBL1N_TX_CH4N	GXBL1N_TX_CH4N/ A35	I, DIFF	Bank1N channel5 High speed differential receiver Negative.
C33	GXBL1N_TX_CH4P	GXBL1N_TX_CH4P/ A36	I, DIFF	Bank1N channel5 High speed differential receiver Positive.
A49	GXBL1N_TX_CH5N	GXBL1N_TX_CH5N/ B33	O, DIFF	Bank1N channel5 High speed differential transmitter Negative.
A48	GXBL1N_TX_CH5P	GXBL1N_TX_CH5P/ B34	O, DIFF	Bank1N channel5 High speed differential transmitter Positive.
C16	REFCLK_GXBL1N_CHBN	REFCLK_GXBL1N_CHBN/ K33	I, DIFF	Bank1N differential Bottom reference clock Negative.
C17	REFCLK_GXBL1N_CHBP	REFCLK_GXBL1N_CHBP/ K34	I, DIFF	Bank1N differential Bottom reference clock Positive.
C21	REFCLK_GXBL1N_CHTN	REFCLK_GXBL1N_CHTN/ H33	I, DIFF	Bank1N differential Top reference clock Negative.
C20	REFCLK_GXBL1N_CHTP	REFCLK_GXBL1N_CHTP/ H34	I, DIFF	Bank1N differential Top reference clock Positive.

2.9.2 Power

The Stratix® 10 GX/SX SoC FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Pin Name	CPU Bank	CPU Pin No	Signal Type/ Termination	Description
A3, A6, A7, A10, A11, A14, A15, A18, A19, A22, A23, A26, A27, A30, A31, A34, A35, A38, A39, A42, A43, A46, A47, A50, A51, A54, A55, A58, B1, B4, B5, B8, B9, B12, B13, B16, B17, B20, B21, B24, B25, B28, B29, B32, B33, B36, B37, B40, B41, B44, B45, B48, B49, B52, B53, B56, B57, B60, C2, C3, C6, C7, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54, C55, C58, C59, D1, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, D24, D25, D28, D29, D32, D33, D36, D37, D40, D41, D44, D45, D48, D49, D52, D53, D56, D57, D60,	GND	NA	NA	NA	Power	Ground.

2.10 Board to Board Connector4

The Stratix® 10 GX/SX SoC FPGA SOM Board to Board connector4 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector4 are explained in the following sections. The Board-to-Board Connector4 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 80

Connector Part Number - ADM6-20-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-20-03.5-L-4-2-A from Samtech

Staking Height - 5mm

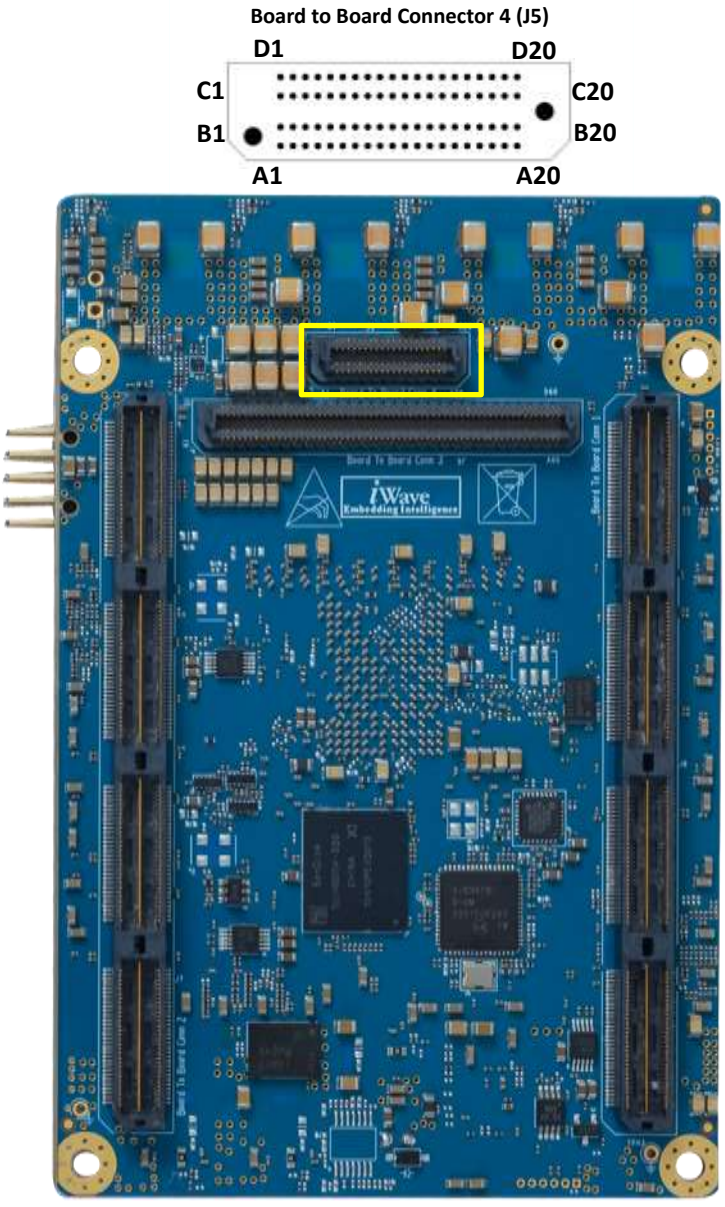


Figure 9: Board to Board Connector4

Table 13: Board to Board Connector4 Pinout

B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name
A1	GND	**B1**	FPGA_LVDS2A_19 N_IO11	**C1**	GND	**D1**	FPGA_LVDS2A_3 N_IO43
A2	FPGA_LVDS2A_24 N_IO1	**B2**	FPGA_LVDS2A_19 P_IO10	**C2**	FPGA_LVDS2A_9 P_IO30	**D2**	GND
A3	FPGA_LVDS2A_24 P_IO0	**B3**	GND	**C3**	FPGA_LVDS2A_9 N_IO31	**D3**	GND
A4	GND	**B4**	FPGA_LVDS2A_18 N_IO13	**C4**	GND	**D4**	FPGA_LVDS2A_4 P_IO40
A5	GND	**B5**	FPGA_LVDS2A_18 P_IO12	**C5**	GND	**D5**	FPGA_LVDS2A_4 N_IO41
A6	FPGA_LVDS2A_23 P_IO2	**B6**	GND	**C6**	FPGA_LVDS2A_8 P_IO32	**D6**	GND
A7	FPGA_LVDS2A_23 N_IO3	**B7**	GND	**C7**	FPGA_LVDS2A_8 N_IO33	**D7**	GND
A8	GND	**B8**	FPGA_LVDS2A_17 N_IO15	**C8**	GND	**D8**	FPGA_LVDS2A_1 1N_IO27
A9	GND	**B9**	FPGA_LVDS2A_17 P_IO14	**C9**	GND	**D9**	FPGA_LVDS2A_1 1P_IO26
A10	FPGA_LVDS2A_22 P_IO4	**B10**	GND	**C10**	FPGA_LVDS2A_7 N_IO35	**D10**	GND
A11	FPGA_LVDS2A_22 N_IO5	**B11**	GND	**C11**	FPGA_LVDS2A_7 P_IO34	**D11**	GND
A12	GND	**B12**	FPGA_LVDS2A_16 P_IO16	**C12**	GND	**D12**	FPGA_LVDS2A_2 N_IO45
A13	GND	**B13**	FPGA_LVDS2A_16 N_IO17	**C13**	GND	**D13**	FPGA_LVDS2A_2 P_IO44
A14	FPGA_LVDS2A_21 P_IO6	**B14**	GND	**C14**	FPGA_LVDS2A_6 P_IO36	**D14**	GND
A15	FPGA_LVDS2A_21 N_IO7	**B15**	GND	**C15**	FPGA_LVDS2A_6 N_IO37	**D15**	GND
A16	GND	**B16**	FPGA_LVDS2A_14 N_IO21	**C16**	GND	**D16**	FPGA_LVDS2A_1 2P/CLKIN_1P
A17	GND	**B17**	FPGA_LVDS2A_14 P_IO20	**C17**	GND	**D17**	FPGA_LVDS2A_1 2N/CLKIN_1N
A18	FPGA_LVDS2A_20 P_IO8	**B18**	GND	**C18**	FPGA_LVDS2A_5 N_IO39	**D18**	GND
A19	FPGA_LVDS2A_20 N_IO9	**B19**	GND	**C19**	FPGA_LVDS2A_5 P_IO38	**D19**	FPGA_LVDS2A_1 3N/CLKIN_0N
A20	GND	**B20**	FPGA_LVDS2A_3P _IO42	**C20**	GND	**D20**	FPGA_LVDS2A_1 3P/CLKIN_0P

2.10.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector4 from Stratix® 10 GX/SX SoC FPGA is explained in the following section.

2.10.1.1 FPGA IOs & General-Purpose Clocks – Bank2B

The Stratix® 10 GX/SX SoC FPGA SOM supports up to 20 LVDS IOs/42 Single Ended IOs and from Stratix® 10 GX/SX FPGA Bank2A on Board-to-Board connector4. In Stratix® 10 SoC/FPGA SOM, Bank2A signals are routed as LVDS IOs to Board-to-Board Connector4. Even though Bank2A signals are routed as LVDS IOs, these pins can be used as SE IOs if required. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Stratix® 10 GX/SX SoC FPGA SOM, upon these 20 LVDS IOs/42 Single Ended IOs from Stratix® 10 GX/SX SoC FPGA Bank2B, two General Purpose Clock input LVDS pair are supported on Board-to-Board connector4. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Stratix® 10 GX/SX SoC FPGA SOM, Bank2A I/O voltage is by default set to 1.8V. It can be configured to other supported voltages by controlling the LDO2 of the PMIC after Boot.

For more details on FPGA Bank2A pinouts on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D12	FPGA_LVDS2A_2N _IO45	LVDS2A_2N/ AM30	IO, 1.8V LVDS	Bank2A 2n differential Negative. Same pin can be configured as Single ended I/O.
D13	FPGA_LVDS2A_2P _IO44	LVDS2A_2P/ AL30	IO, 1.8V LVDS	Bank2A 2p differential Positive. Same pin can be configured as Single ended I/O.
D1	FPGA_LVDS2A_3N _IO43	LVDS2A_3N/ AP30	IO, 1.8V LVCMOS	Bank2A 3n Single ended I/O.
B20	FPGA_LVDS2A_3P _IO42	LVDS2A_3P/ AN30	IO, 1.8V LVCMOS	Bank2A 3p Single ended I/O.
D5	FPGA_LVDS2A_4N _IO41	LVDS2A_4N/ AR30	IO, 1.8V LVDS	Bank2A 4n differential Negative. Same pin can be configured as Single ended I/O.
D4	FPGA_LVDS2A_4P _IO40	LVDS2A_4P/ AP29	IO, 1.8V LVDS	Bank2A 4p differential Positive. Same pin can be configured as Single ended I/O.
C18	FPGA_LVDS2A_5N _IO39	LVDS2A_5N/ AR28	IO, 1.8V LVDS	Bank2A 5n differential Negative. Same pin can be configured as Single ended I/O.

B2B-4 Pin No	B2B Connector4 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C19	FPGA_LVDS2A_5P_IO38	LVDS2A_5P/ AP28	IO, 1.8V LVDS	Bank2A 5p differential Positive. Same pin can be configured as Single ended I/O.
C15	FPGA_LVDS2A_6N_IO37	LVDS2A_6N/ AT29	IO, 1.8V LVDS	Bank2A 6n differential Negative. Same pin can be configured as Single ended I/O.
C14	FPGA_LVDS2A_6P_IO36	LVDS2A_6P/ AR29	IO, 1.8V LVDS	Bank2A 6p differential Positive. Same pin can be configured as Single ended I/O.
C10	FPGA_LVDS2A_7N_IO35	LVDS2A_7N/ AL27	IO, 1.8V LVDS	Bank2A 7n differential Negative. Same pin can be configured as Single ended I/O.
C11	FPGA_LVDS2A_7P_IO34	LVDS2A_7P/ AM27	IO, 1.8V LVDS	Bank2A 7p differential Positive. Same pin can be configured as Single ended I/O.
C7	FPGA_LVDS2A_8N_IO33	LVDS2A_8N/ AK30	IO, 1.8V LVDS	Bank2A 8n differential Negative. Same pin can be configured as Single ended I/O.
C6	FPGA_LVDS2A_8P_IO32	LVDS2A_8P/ AK29	IO, 1.8V LVDS	Bank2A 8p differential Positive. Same pin can be configured as Single ended I/O.
C3	FPGA_LVDS2A_9N_IO31	LVDS2A_9N/ AN27	IO, 1.8V LVDS	Bank2A 9n differential Negative. Same pin can be configured as Single ended I/O.
C2	FPGA_LVDS2A_9P_IO30	LVDS2A_9P/ AP26	IO, 1.8V LVDS	Bank2A 9p differential Positive. Same pin can be configured as Single ended I/O.
D8	FPGA_LVDS2A_11N_IO27	LVDS2A_11N/ AN28	IO, 1.8V LVDS	Bank2A 11n differential Negative. Same pin can be configured as Single ended I/O.
D9	FPGA_LVDS2A_11P_IO26	LVDS2A_11P/ AM28	IO, 1.8V LVDS	Bank2A 11p differential Positive. Same pin can be configured as Single ended I/O.
D17	FPGA_LVDS2A_12N/CLKIN_1N	LVDS2A_12N/ AL29	IO, 1.8V LVDS	Bank2A 12n differential Negative. Same pin can be configured as Single ended I/O.
D16	FPGA_LVDS2A_12P/CLKIN_1P	LVDS2A_12P/ AM29	IO, 1.8V LVDS	Bank2A 12p differential Positive. Same pin can be configured as Single ended I/O.
D19	FPGA_LVDS2A_13N/CLKIN_0N	LVDS2A_13N/ AV26	IO, 1.8V LVDS	Bank2A 13n differential Negative. Same pin can be configured as Single ended I/O.

B2B-4 Pin No	B2B Connector4 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
D20	FPGA_LVDS2A_13P/CLKIN_0P	LVDS2A_13P/ AV27	IO, 1.8V LVDS	Bank2A 13p differential Positive. Same pin can be configured as Single ended I/O.
B16	FPGA_LVDS2A_14N_IO21	LVDS2A_14N/ BB27	IO, 1.8V LVDS	Bank2A 14n differential Negative. Same pin can be configured as Single ended I/O.
B17	FPGA_LVDS2A_14P_IO20	LVDS2A_14P/ BA27	IO, 1.8V LVDS	Bank2A 14p differential Positive. Same pin can be configured as Single ended I/O.
B13	FPGA_LVDS2A_16N_IO17	LVDS2A_16N/ BA25	IO, 1.8V LVDS	Bank2A 16n differential Negative. Same pin can be configured as Single ended I/O.
B12	FPGA_LVDS2A_16P_IO16	LVDS2A_16P/ BB25	IO, 1.8V LVDS	Bank2A 16p differential Positive. Same pin can be configured as Single ended I/O.
B8	FPGA_LVDS2A_17N_IO15	LVDS2A_17N/ AY26	IO, 1.8V LVDS	Bank2A 17n differential Negative. Same pin can be configured as Single ended I/O.
B9	FPGA_LVDS2A_17P_IO14	LVDS2A_17P/ AW26	IO, 1.8V LVDS	Bank2A 17p differential Positive. Same pin can be configured as Single ended I/O.
B4	FPGA_LVDS2A_18N_IO13	LVDS2A_18N/ BA24	IO, 1.8V LVDS	Bank2A 18n differential Negative. Same pin can be configured as Single ended I/O.
B5	FPGA_LVDS2A_18P_IO12	LVDS2A_18P/ BB24	IO, 1.8V LVDS	Bank2A 18p differential Positive. Same pin can be configured as Single ended I/O.
B1	FPGA_LVDS2A_19N_IO11	LVDS2A_19N/ AU24	IO, 1.8V LVDS	Bank2A 19n differential Negative. Same pin can be configured as Single ended I/O.
B2	FPGA_LVDS2A_19P_IO10	LVDS2A_19P/ AT24	IO, 1.8V LVDS	Bank2A 19p differential Positive. Same pin can be configured as Single ended I/O.
A19	FPGA_LVDS2A_20N_IO9	LVDS2A_20N/ AW25	IO, 1.8V LVDS	Bank2A 20n differential Negative. Same pin can be configured as Single ended I/O.
A18	FPGA_LVDS2A_20P_IO8	LVDS2A_20P/ AV25	IO, 1.8V LVDS	Bank2A 20p differential Positive. Same pin can be configured as Single ended I/O.
A15	FPGA_LVDS2A_21N_IO7	LVDS2A_21N/ AT26	IO, 1.8V LVDS	Bank2A 21n differential Negative. Same pin can be configured as Single ended I/O.

B2B-4 Pin No	B2B Connector4 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	FPGA_LVDS2A_21P_IO6	LVDS2A_21P/ AR27	IO, 1.8V LVDS	Bank2A 21p differential Positive. Same pin can be configured as Single ended I/O.
A11	FPGA_LVDS2A_22N_IO5	LVDS2A_22N/ AU27	IO, 1.8V LVDS	Bank2A 22n differential Negative. Same pin can be configured as Single ended I/O.
A10	FPGA_LVDS2A_22P_IO4	LVDS2A_22P/ AT27	IO, 1.8V LVDS	Bank2A 22p differential Positive. Same pin can be configured as Single ended I/O.
A7	FPGA_LVDS2A_23N_IO3	LVDS2A_23N/ AY24	IO, 1.8V LVDS	Bank2A 23n differential Negative. Same pin can be configured as Single ended I/O.
A6	FPGA_LVDS2A_23P_IO2	LVDS2A_23P/ AW24	IO, 1.8V LVDS	Bank2A 23p differential Positive. Same pin can be configured as Single ended I/O.
A2	FPGA_LVDS2A_24N_IO1	LVDS2A_24N/ AU25	IO, 1.8V LVDS	Bank2A 24n differential Negative. Same pin can be configured as Single ended I/O.
A3	FPGA_LVDS2A_24P_IO0	LVDS2A_24P/ AT25	IO, 1.8V LVDS	Bank2A 24p differential Positive. Same pin can be configured as Single ended I/O.

2.10.2 Power

The Stratix® 10 GX/SX SoC FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector4, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Pin Name	CPU Pin Name	Signal Type/ Termination	Description
A1, A4, A5, A8, A9, A12, A13, A16, A17, A20, B3, B6, B7, B10, B11, B14, B15, B18, B19, C1, C4, C5, C8, C9, C12, C13, C16, C17, C20, D2, D3, D6, D7, D10, D11, D14, D15, D18	GND	NA	Power	Ground.

2.11 Stratix® 10 SX SoC FPGA HPS Pin Multiplexing on Board to Board Connectors

The Stratix® 10 SX SoC FPGA HPS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Stratix® 10 SX HPS IO pins can be configured as GPIO if required. The below table provides the details of HPS pin connections on Stratix® 10 GX/SX SoC FPGA with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring HPS I/O configuration. To know the complete available alternate functions, refer the HPS I/O configuration in the latest Quartus Tool.

Table 14: HPS IOMUX on Stratix® 10 SX SoC FPGA SOM

Interface/ Function	B2B Connector Pin Number	Stratix® 10 GX/SX SoC FPGA Pin Name	GPIO	Function 8	Function 7	Function 6	Function 5	Function 4	Function 3	Function 2	Function 1	Function 0
On SOM Features from Stratix® 10 SX HPS												
eMMC FLASH	NA	HPS_IOB_13	GPIO1_IO12	GPIO1_IO12				I2C1_SDA	NAND_ALE	Trace_D10	SDMMC_DATA0	EMAC2_TX_CLK
	NA	HPS_IOB_14	GPIO1_IO13	GPIO1_IO13				I2C1_SCL	NAND_RB	Trace_D9	SDMMC_CMD	EMAC2_TX_CTL
	NA	HPS_IOB_15	GPIO1_IO14	GPIO1_IO14			UART1_TX		NAND_CE_N	Trace_D8	SDMMC_CCLK	EMAC2_RX_CLK
	NA	HPS_IOB_16	GPIO1_IO15	GPIO1_IO15			UART1_RX			Trace_D7	SDMMC_DATA1	EMAC2_RX_CTL
	NA	HPS_IOB_17	GPIO1_IO16	GPIO1_IO16			UART1_CTS_N		NAND_ADQ8	Trace_D6	SDMMC_DATA2	EMAC2_TXD0
	NA	HPS_IOB_18	GPIO1_IO17	GPIO1_IO17	SPIM0_SS1_N		UART1_RTS_N		NAND_ADQ9	Trace_D5	SDMMC_DATA3	EMAC2_TXD1
	NA	HPS_IOB_19	GPIO1_IO18	GPIO1_IO18	SPIM0_MISO		MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ10	Trace_D4	SDMMC_DATA4	EMAC2_RXD0
	NA	HPS_IOB_20	GPIO1_IO19	GPIO1_IO19	SPIM0_SS0_N		MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ11	Trace_CLK	SDMMC_DATA5	EMAC2_RXD1
	NA	HPS_IOB_21	GPIO1_IO20	GPIO1_IO20	SPIM0_CLK	SPIS1_CLK		I2C_EMAC2_SDA	NAND_ADQ12	Trace_D0	SDMMC_DATA6	EMAC2_TXD2
	NA	HPS_IOB_22	GPIO1_IO21	GPIO1_IO21	SPIM0_MOSI	SPIS1_MOSI		I2C_EMAC2_SCL	NAND_ADQ13	Trace_D1	SDMMC_DATA7	EMAC2_TXD3
	NA	HPS_IOB_23	GPIO1_IO22	GPIO1_IO22	SPIM0_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ14	Trace_D2	SDMMC_PWR_EN	EMAC2_RXD2
ENET	NA	HPS_IOB_1	GPIO1_IO0	GPIO1_IO0	SPIM1_CLK		UART0_CTS_N		NAND_ADQ0	Trace_D10		EMAC1_TX_CLK
	NA	HPS_IOB_2	GPIO1_IO1	GPIO1_IO1	SPIM1_MOSI		UART0_RTS_N		NAND_ADQ1	Trace_D9		EMAC1_TX_CTL
	NA	HPS_IOB_3	GPIO1_IO2	GPIO1_IO2	SPIM1_SS0_N		UART0_TX	I2C0_SDA	NAND_WE_N	Trace_D8		EMAC1_RX_CLK
	NA	HPS_IOB_4	GPIO1_IO3	GPIO1_IO3	SPIM1_SS1_N	SPIS1_CLK	UART0_RX	I2C0_SCL	NAND_RE_N	Trace_D7		EMAC1_RX_CTL
	NA	HPS_IOB_5	GPIO1_IO4	GPIO1_IO4		SPIS1_MOSI	UART1_CTS_N		NAND_WP_N	Trace_D6		EMAC1_TXD0
	NA	HPS_IOB_6	GPIO1_IO5	GPIO1_IO5		SPIS1_SS0_N	UART1_RTS_N		NAND_ADQ2	Trace_D5		EMAC1_TXD1
	NA	HPS_IOB_7	GPIO1_IO6	GPIO1_IO6		SPIS1_MISO	UART1_TX	I2C1_SDA	NAND_ADQ3	Trace_D4		EMAC1_RXD0
	NA	HPS_IOB_8	GPIO1_IO7	GPIO1_IO7		JTAG_TCK	UART1_RX	I2C1_SCL	NAND_CLE	Trace_D15		EMAC1_RXD1
	NA	HPS_IOB_9	GPIO1_IO8	GPIO1_IO8	JTAG_TMS	SPIS0_CLK	MDIO2_MDIO	I2C_EMAC2_SDA	NAND_ADQ4	Trace_D14		EMAC1_TXD2
	NA	HPS_IOB_10	GPIO1_IO9	GPIO1_IO9	JTAG_TDO	SPIS0_MOSI	MDIO2_MDC	I2C_EMAC2_SCL	NAND_ADQ5	Trace_D13		EMAC1_TXD3
	NA	HPS_IOB_11	GPIO1_IO10	GPIO1_IO10	JTAG_TDI	SPIS0_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	Trace_D12		EMAC1_RXD2
	NA	HPS_IOB_12	GPIO1_IO11	GPIO1_IO11		SPIS0_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	Trace_D11		EMAC1_RXD3
	NA	HPS_IOA_11	GPIO0_IO10	GPIO0_IO10	SPIM1_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	Trace_D12	USB0_DATA6	
	NA	HPS_IOA_9	GPIO0_IO8	GPIO0_IO8	SPIM1_CLK	SPIS1_CLK	MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ4	Trace_D14	USB0_DATA4	SDMMC_DATA6
	NA	HPS_IOA_10	GPIO0_IO9	GPIO0_IO9	SPIM1_MOSI	SPIS1_MOSI	MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ5	Trace_D13	USB0_DATA5	SDMMC_DATA7
USB2.0	NA	HPS_IOA_13	GPIO0_IO12	GPIO0_IO12					NAND_ALE	Trace_D10	USB1_CLK	EMAC0_TX_CLK
	NA	HPS_IOA_14	GPIO0_IO13	GPIO0_IO13					NAND_RB	Trace_D9	USB1_STP	EMAC0_TX_CTL
	NA	HPS_IOA_15	GPIO0_IO14	GPIO0_IO14					NAND_CE_N	Trace_D8	USB1_DIR	EMAC0_RX_CLK
	NA	HPS_IOA_16	GPIO0_IO15	GPIO0_IO15						Trace_D7	USB1_DATA0	EMAC0_RX_CTL
	NA	HPS_IOA_17	GPIO0_IO16	GPIO0_IO16					NAND_ADQ8	Trace_D6	USB1_DATA1	EMAC0_TXD0
	NA	HPS_IOA_18	GPIO0_IO17	GPIO0_IO17					NAND_ADQ9	Trace_D5	USB1_NXT	EMAC0_TXD1
	NA	HPS_IOA_19	GPIO0_IO18	GPIO0_IO18					NAND_ADQ10	Trace_D4	USB1_DATA2	EMAC0_RXD0
	NA	HPS_IOA_20	GPIO0_IO19	GPIO0_IO19	SPIM1_SS1_N				NAND_ADQ11	Trace_CLK	USB1_DATA3	EMAC0_RXD1
	NA	HPS_IOA_21	GPIO0_IO20	GPIO0_IO20	SPIM1_CLK	SPIS0_CLK	UART0_CTS_N	I2C1_SDA	NAND_ADQ12	Trace_D0	USB1_DATA4	EMAC0_TXD2
	NA	HPS_IOA_22	GPIO0_IO21	GPIO0_IO21	SPIM1_MOSI	SPIS0_MOSI	UART0_RTS_N	I2C1_SCL	NAND_ADQ13	Trace_D1	USB1_DATA5	EMAC0_TXD3
	NA	HPS_IOA_23	GPIO0_IO22	GPIO0_IO22	SPIM1_MISO	SPIS0_SS0_N	UART0_TX	I2C0_SDA	NAND_ADQ14	Trace_D2	USB1_DATA6	EMAC0_RXD2
	NA	HPS_IOA_24	GPIO0_IO23	GPIO0_IO23	SPIM1_SS0_N	SPIS0_MISO	UART0_RX	I2C0_SCL	NAND_ADQ15	Trace_D3	USB1_DATA7	EMAC0_RXD3
	NA	HPS_IOA_12	GPIO0_IO11	GPIO0_IO11	SPIM1_SS0_N	SPIS1_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	Trace_D11	USB0_DATA7	

Interface/ Function	B2B Connector Pin Number	Stratix® 10 GX/SX SoC FPGA Pin Name	GPIO	Function 8	Function 7	Function 6	Function 5	Function 4	Function 3	Function 2	Function 1	Function 0
Board-to-Board Connector2 Features from Stratix® 10 SX HPS												
UART0	61	HPS_IOA_1	GPIO0_IO0	GPIO0_IO0	SPIM0_SS1_N	SPIS0_CLK	UART0_CTS_N		NAND_ADQ0	Trace_D10	USB0_CLK	SDMMC_CCLK
	65	HPS_IOA_2	GPIO0_IO1	GPIO0_IO1	SPIM1_SS1_N	SPIS0_MOSI	UART0_RTS_N		NAND_ADQ1	Trace_D9	USB0_STP	SDMMC_CMD
	63	HPS_IOA_3	GPIO0_IO2	GPIO0_IO2		SPIS0_SS0_N	UART0_TX	I2C1_SDA	NAND_WE_N	Trace_D8	USB0_DIR	SDMMC_DATA0
	67	HPS_IOA_4	GPIO0_IO3	GPIO0_IO3		SPIS0_MISO	UART0_RX	I2C1_SCL	NAND_RE_N	Trace_D7	USB0_DATA0	SDMMC_DATA1
I2C	46	HPS_IOA_5	GPIO0_IO4	GPIO0_IO4	SPIM0_CLK		UART1_CTS_N	I2C0_SDA	NAND_WP_N	Trace_D6	USB0_DATA1	SDMMC_DATA2
	48	HPS_IOA_6	GPIO0_IO5	GPIO0_IO5	SPIM0_MOSI		UART1_RTS_N	I2C0_SCL	NAND_ADQ2	Trace_D5	USB0_NXT	SDMMC_DATA3
Debug UART	54	HPS_IOA_7	GPIO0_IO6	GPIO0_IO6	SPIM0_MISO	MDIO2_MDIO	UART1_TX	I2C_EMAC2_SDA	NAND_ADQ3	Trace_D4	USB0_DATA2	SDMMC_DATA4
	56	HPS_IOA_8	GPIO0_IO7	GPIO0_IO7	SPIM0_SS0_N	MDIO2_MDC	UART1_RX	I2C_EMAC2_SCL	NAND_CLE	Trace_D15	USB0_DATA3	SDMMC_DATA5

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Stratix® 10 GX/SX SoC FPGA SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Stratix® 10 GX/SX SoC FPGA SOM.

Table 15: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Stratix® 10 GX/SX SoC FPGA SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.

[2] Stratix® 10 GX/SX SoC FPGA SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Stratix® 10 GX/SX SoC FPGA SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board-to-Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

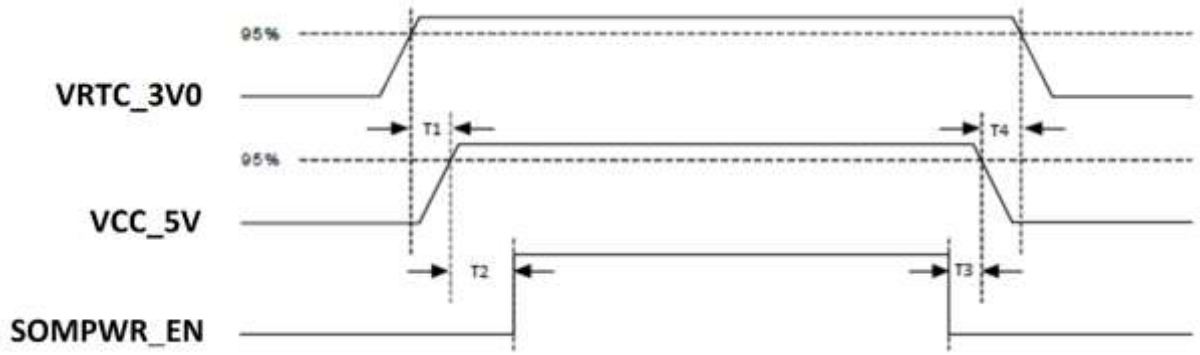


Figure 10: Power Input Sequencing

Table 16: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_5V input power to other all the powers are getting stable around 50ms in SOM. Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

TBD

For more accurate power estimation, iWave recommends to use Intel Power Estimator (IPE) tool and calculate the SoC and FPGA power. Also add extra power for other On-SOM peripherals power.

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Stratix® 10 GX/SX SoC FPGA SOM.

Table 17: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS3 Compliance

iWave's Stratix® 10 GX/SX SoC FPGA SOM is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Stratix® 10 GX/SX SoC FPGA SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

3.3 MechanicalCharacteristics

3.3.1 Stratix® 10 GX/SX SoC FPGA SOM Mechanical Dimensions

Stratix® 10 GX/SX SoC FPGA SOM PCB size is 110mm x 75mm x 2.8mm and weight is TBD. SOM mechanical dimension is shown below.

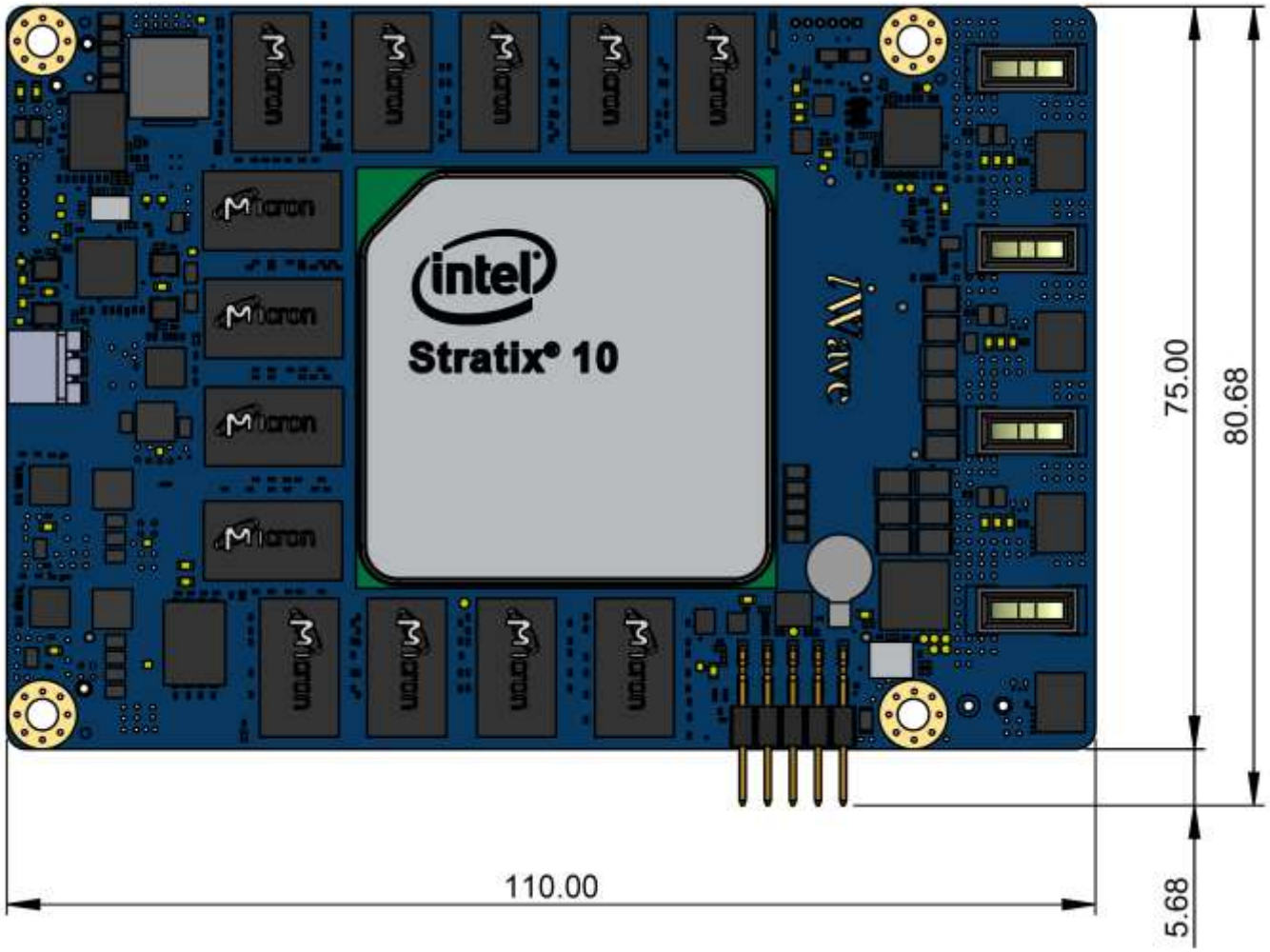


Figure 11: Mechanical dimension of Stratix® 10 GX/SX SoC FPGA SOM - Top View

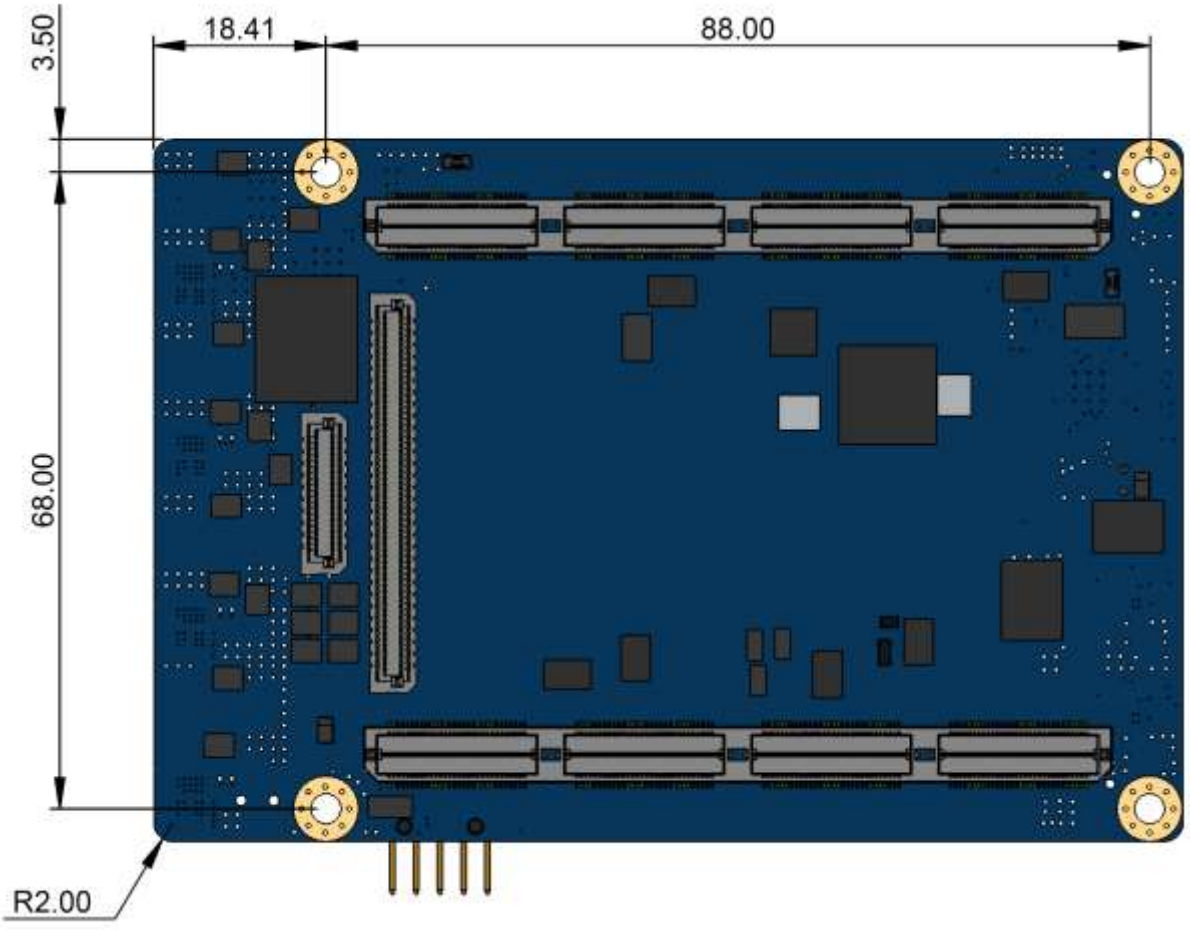


Figure 12: Mechanical dimension of Stratix® 10 GX/SX SoC FPGA SOM - Bottom View

Stratix® 10 GX/SX SoC FPGA PCB thickness is 2.8mm±0.1mm, top side maximum height component is Inductors L1, L2, L3 & L4 (6 mm) followed by JTAG Header J2 (5.08 mm) and bottom side maximum height component is Board-to-Board connector 1 & 2 (4.27mm) followed by Board-to-Board connector 3(4.02mm). Please refer the below figure which gives height details of the Stratix® 10 GX/SX SoC FPGA SOM.

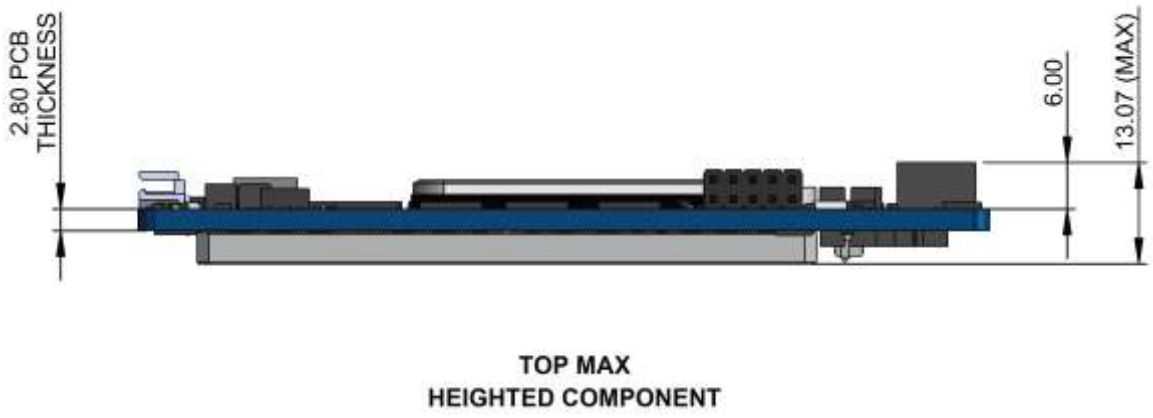


Figure 13: Mechanical dimension of Stratix® 10 GX/SX SoC FPGA SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Stratix® 10 GX/SX SoC FPGA SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 18: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G45M – SC850 (speed -2) Stratix 10 SOC SOM		
iW-G45M-S085-4E008G-E032G-BEA	SX850 (Speed - 2) Stratix 10 SOC, 8GB HPS DDR4 with ECC, Dual 8GB FPGA DDR4, 32GB EMMC, Extended	-40°C to 85°C

5. APPENDIX

5.1 Stratix® 10 GX/SX SoC FPGA SOM Development Platform

iWave Systems supports iW-RainboW-G45D – Stratix® 10 GX/SX SoC FPGA SOM Development Platform which is targeted for quick validation of Stratix® 10 GX/SX SoC FPGA based SOM. iWave's Stratix® 10 GX/SX SoC FPGA Development Board incorporates Stratix® 10 GX/SX SoC FPGA SOM and High-performance Carrier board with complete BSP support.

For more details on Stratix® 10 GX/SX SoC FPGA SOM Development Platform, visit the below web link.

Link: *https://www.iwavesystems.com/product/stratix-10-soc-fpga-som/*

Figure 14: Stratix® 10 GX/SX SoC FPGA SOM Development Platform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