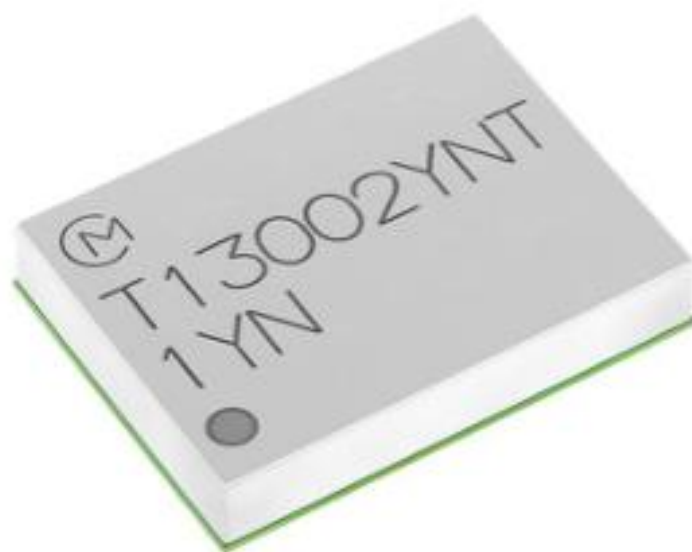


# Type 1YN Wi-Fi™ + Bluetooth® Module

Infineon CYW43439 Chipset for 802.11b/g/n + Bluetooth 5.1  
Datasheet – Rev. 8

- Design Name: Type 1YN
- Module P/N: LBEE5KL1YN-814



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## About This Document

Type 1YN is a small and high performance module based on Infineon CYW43439 combo chipset which supports Wi-Fi™ 802.11b/g/n + Bluetooth 5.1 BR/EDR/LE. This datasheet describes Type 1YN module in detail.



Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

## Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product; specifically RF, hardware, software, and systems engineers.

## Document Conventions

**Table 1** describes the document conventions.

**Table 1: Document Conventions**

| Conventions                                                                         | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Warning Note</b><br>Indicates very important note. Users are strongly recommended to review.                                                                                                                                                                                                                                                                                               |
|  | <b>Info Note</b><br>Intended for informational purposes. Users should review.                                                                                                                                                                                                                                                                                                                 |
|  | <b>Menu Reference</b><br>Indicates menu navigation instructions.<br><b>Example:</b> Insert → Tables → Quick Tables → Save Selection to Gallery                                                                                                                                                           |
|  | <b>External Hyperlink</b><br>This symbol indicates a hyperlink to an external document or website.<br><b>Example:</b> <a href="#">Murata</a> <br>Click on the text to open the external link.                                                                                                              |
|  | <b>Internal Hyperlink</b><br>This symbol indicates a hyperlink within the document.<br><b>Example:</b> <a href="#">Scope</a> <br>Click on the text to open the link.                                                                                                                                       |
| <code>Console input/output or code snippet</code>                                   | <b>Console I/O or Code Snippet</b><br>This text <b>Style</b> denotes console input/output or a code snippet.                                                                                                                                                                                                                                                                                  |
| <code># Console I/O comment<br/>// Code snippet comment</code>                      | <b>Console I/O or Code Snippet Comment</b><br>This text <b>Style</b> denotes a console input/output or code snippet comment. <ul style="list-style-type: none"> <li>• Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output.</li> <li>• Code Snippet comment (preceded by "//") may exist in the original code.</li> </ul> |

## 1 Scope

This specification characterizes the IEEE 802.11b/g/n + Bluetooth 5.1 BR/EDR/BLE combo module.

## 2 Key Features

- ◆ Infineon CYW43439 inside
- ◆ Supports IEEE 802.11b/g/n specification: 2.4 GHz.
- ◆ Up to 65 Mbps PHY data rates
- ◆ Supports Bluetooth specification version 5.1.
- ◆ For supported Bluetooth functions, refer to [Bluetooth SIG site](#) 
- ◆ WLAN interface: SDIO 2.0
- ◆ Bluetooth interface: HCI UART and PCM
- ◆ Reference clock is embedded.
- ◆ Temperature Range: - 40 °C to 85 °C
- ◆ Dimensions: 6.95 x 5.15 x 1.1 mm
- ◆ MSL: 3
- ◆ Surface-mount type
- ◆ RoHS compliant.
- ◆ MAC/BD address are embedded.
- ◆ Total Fit : 134

## 3 Ordering Information

**Table 2** describes the ordering information.

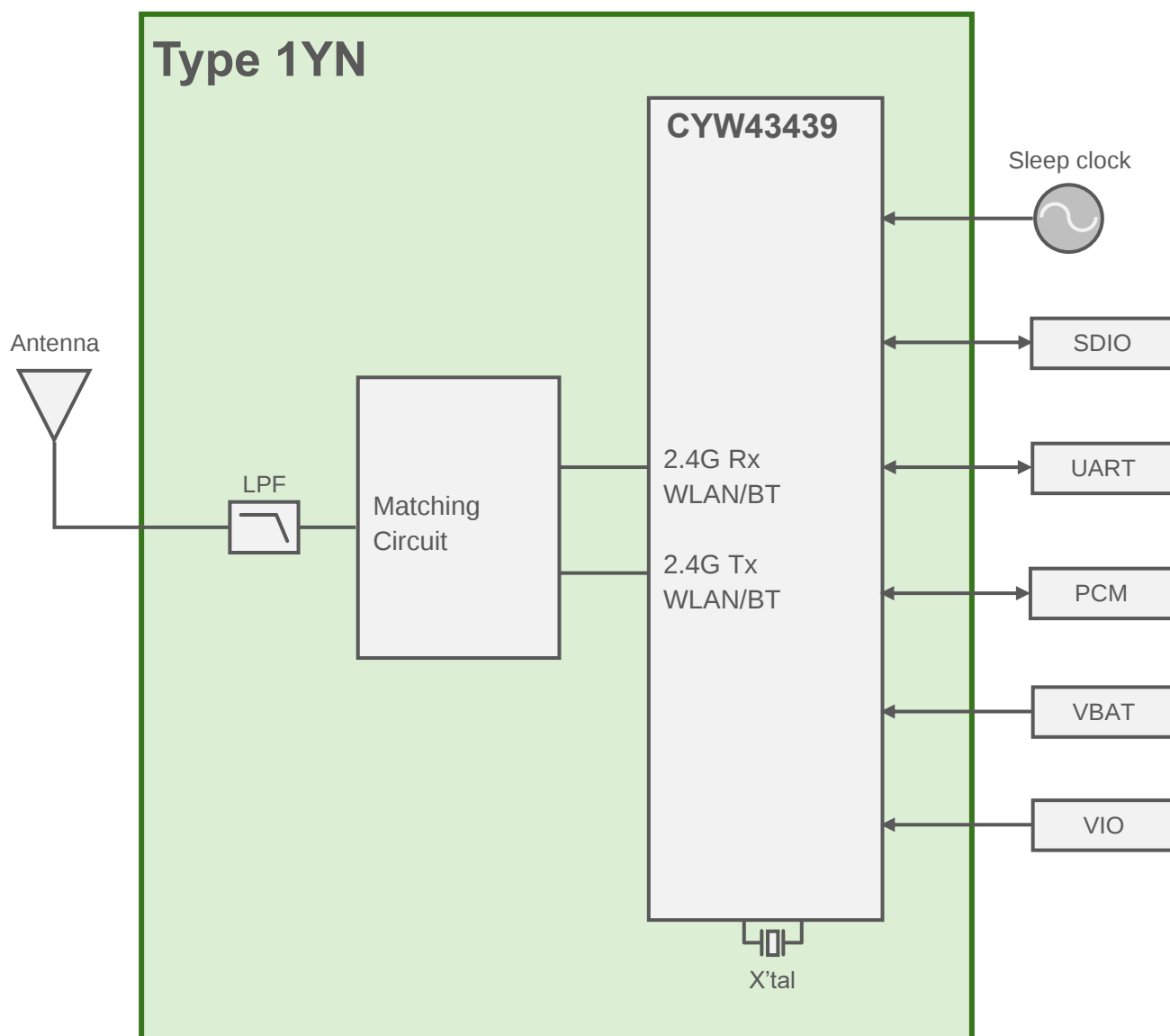
**Table 2: Ordering Information**

| Ordering Part Number | Description                                                                                                                 |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------|
| LBEE5KL1YN-814       | Module order                                                                                                                |
| LBEE5KL1YN-SMP       | Sample module order (If module samples are not available through distribution, contact Murata referencing this part number) |
| EAR00389             | Embedded Artists Type 1YN M.2 EVB (default EVB available through distribution)                                              |

## 4 Block Diagram

The Type 1YN block diagram is presented in **Figure 1**.

**Figure 1: Block Diagram**



## 5 Certification Information

This section has information about radio and Bluetooth certification.

### 5.1 Radio Certification

**Table 3** describes the radio certification for 1YN module.

**Table 3: Certification Information**

| Country     | ID                                                               | Country Code |
|-------------|------------------------------------------------------------------|--------------|
| USA (FCC)   | The ID VPYLB1DX of Type 1DX can be reused                        | US           |
| Canada (IC) | The ID 772C-LB1DX of Type 1DX can be reused                      | CA           |
| Europe      | EN300328 v2.2.2 conducted test report of Type 1DX can be reused. | DE           |
| Japan       | Japanese type certification is prepared.<br>[R] 01-P00840        | JP           |



Each country code is defined by Murata's clm Blob file.  
You can get Murata's clm Blob file at [Murata GitHub](#)

### 5.2 Radio Regulatory Certification by Country

Murata have prepared the document about Radio Regulatory Certification separately.

This document is designed to ensure that module manufacturers correctly communicate the necessary information to host manufacturers that incorporate their modules.

Refer to 【Regulatory Information】 : [Type 1YN Radio Law Approval Application Note](#) for Radio Law Certification user manual.



If you don't follow the rule written in Type 1YN Radio Law Approval Application Note, there is a risk of conflict Radio Law Certification.  
Please be sure to check the document.

### 5.3 Bluetooth Qualification

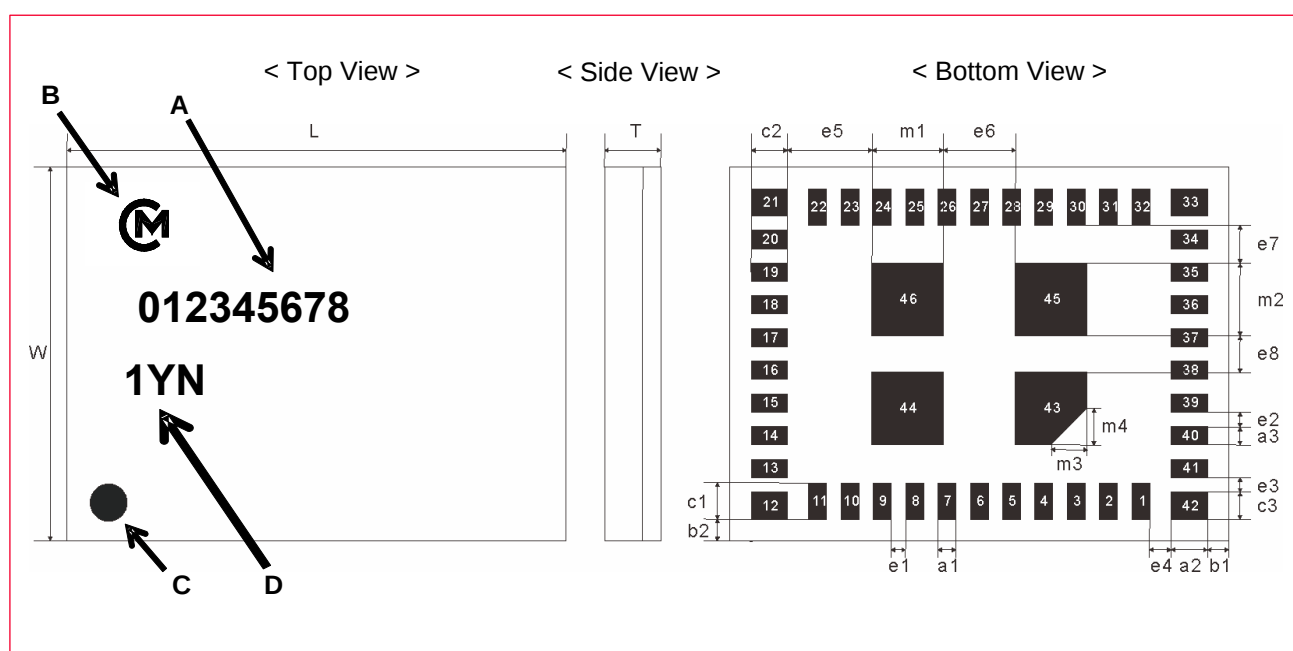
- QDID: 140301
- For supported Bluetooth functions, search ICS detail at [Bluetooth SIG site](#) .

## 6 Dimensions, Markings and Terminal Configurations

This section has information on dimensions, marking, and terminal configurations for Type 1YN.

**Figure 2** shows the dimensions, marking, and terminal configurations.

**Figure 2: Dimension, Markings and Terminal Configuration**



**Table 4** describes the Type 1YN markings.

**Table 4: Markings**

| Marking | Meaning           |
|---------|-------------------|
| A       | Inspection Number |
| B       | Murata Logo       |
| C       | Pin 1 Marking     |
| D       | Module Type       |

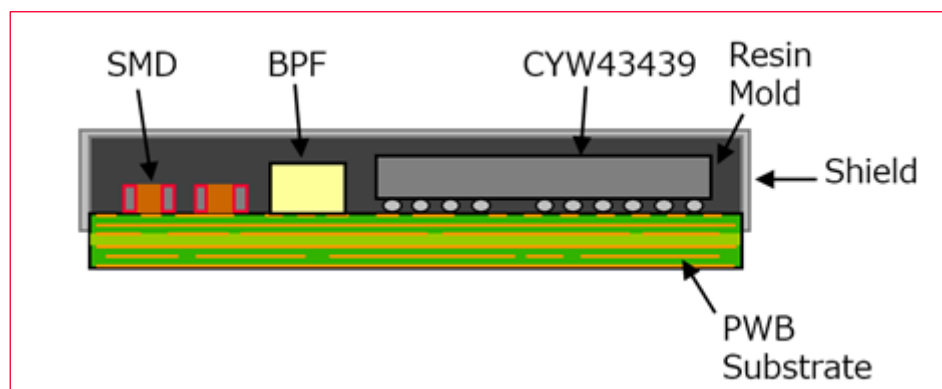
**Table 5** describes the Type 1YN dimensions.

**Table 5: Dimensions**

| Mark | Dimensions (mm) | Mark | Dimensions (mm) | Mark | Dimensions (mm) |
|------|-----------------|------|-----------------|------|-----------------|
| L    | 6.95 +/- 0.2    | W    | 5.15 +/- 0.2    | T    | 1.1 maximum     |
| a1   | 0.25 +/- 0.10   | a2   | 0.5 +/- 0.1     | a3   | 0.25 +/- 0.10   |
| b1   | 0.30 +/- 0.2    | b2   | 0.30 +/- 0.2    | c1   | 0.50 +/- 0.1    |
| c2   | 0.50 +/- 0.1    | c3   | 0.375 +/- 0.100 | e1   | 0.2 +/- 0.1     |
| e2   | 0.2 +/- 0.1     | e3   | 0.2 +/- 0.1     | e4   | 0.3 +/- 0.1     |
| e5   | 1.175 +/- 0.100 | e6   | 1.0 +/- 0.1     | e7   | 0.525 +/- 0.100 |
| e8   | 0.50 +/- 0.10   | m1   | 1.0 +/- 0.1     | m2   | 1.0 +/- 0.1     |
| m3   | 0.5 +/- 0.1     | m4   | 0.5 +/- 0.1     |      |                 |

**Figure 3** shows the structure of Type 1YN module.

**Figure 3: Structure**



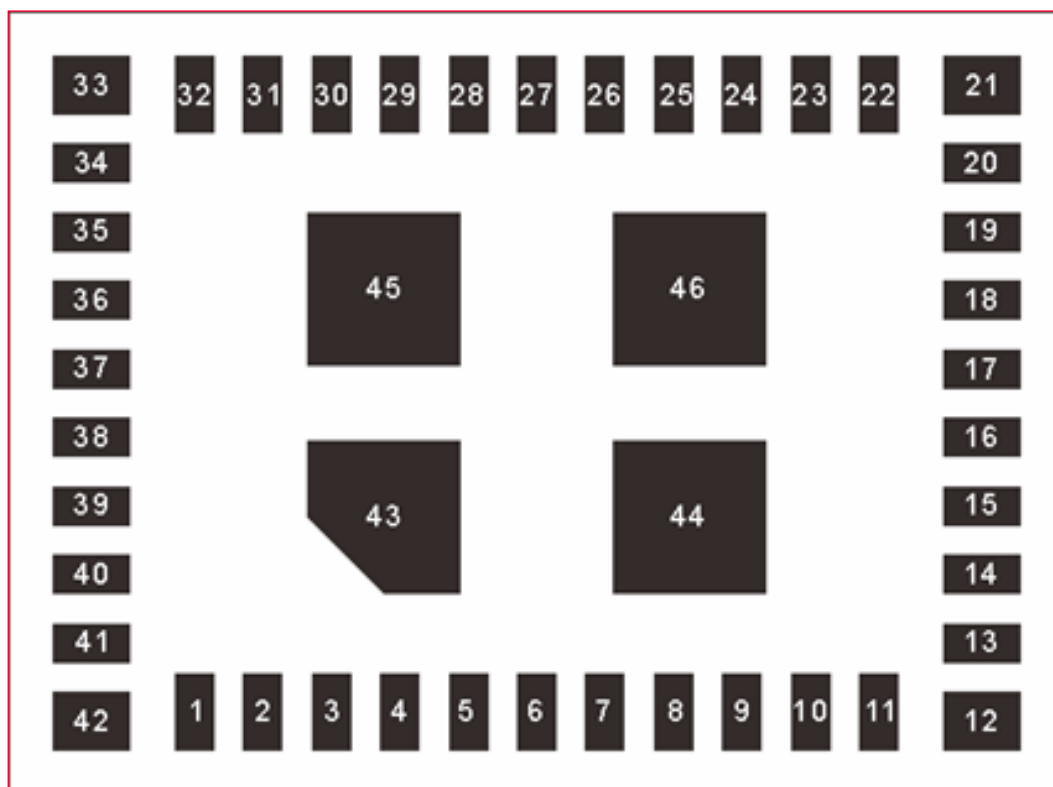
## 7 Module Pin Descriptions

This section has the pin descriptions of Type 1YN and pin assignments layout descriptions.

### 7.1 Module Pin Layout

The pin assignment (top view) layout is shown in **Figure 4**.

**Figure 4: Pin Assignments Top View**



**Table 6** illustrates the terminal configurations.

**Table 6: Terminal Configurations**

| No. | Terminal Name | No. | Terminal Name       | No.   | Terminal Name  |
|-----|---------------|-----|---------------------|-------|----------------|
| 1   | GND           | 15  | NC                  | 29    | GND            |
| 2   | BT_UART_RXD   | 16  | NC                  | 30    | VBAT           |
| 3   | BT_UART_TXD   | 17  | WL_GPIO_2           | 31    | VIN_LDO        |
| 4   | BT_UART_CTS_N | 18  | WL_GPIO_1           | 32    | GND (SR_PVSS)  |
| 5   | BT_UART_RTS_N | 19  | GND                 | 33    | GND (SR_PVSS)  |
| 6   | NC            | 20  | SDIO_CLK            | 34    | SR_VLX         |
| 7   | NC            | 21  | GND                 | 35    | GND            |
| 8   | BT_PCM_SYNC   | 22  | SDIO_CMD            | 36    | VIO            |
| 9   | BT_PCM_IN     | 23  | SDIO_DATA_2         | 37    | LPO_IN (32kHz) |
| 10  | BT_PCM_OUT    | 24  | SDIO_DATA_0         | 38    | BT_HOST_WAKE   |
| 11  | BT_PCM_CLK    | 25  | SDIO_DATA_3         | 39    | BT_DEV_WAKE    |
| 12  | GND           | 26  | SDIO_DATA_1         | 40    | GND            |
| 13  | NC            | 27  | WL_GPIO_0_HOST_WAKE | 41    | ANT            |
| 14  | BT_REG_ON     | 28  | WL_REG_ON           | 42~46 | GND            |

## 7.2 Pin Descriptions

**Table 7** describes Type 1YN Pins.

**Table 7: Pin Descriptions**

| No. | Pin name      | Type | Connection to IC Pin Name | Description                                                                                                                                                                                                                                                                               |
|-----|---------------|------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | GND           |      |                           | Ground                                                                                                                                                                                                                                                                                    |
| 2   | BT_UART_RXD   | I    | BT_UART_RXD               | UART serial input. Serial data input for the HCI UART interface.                                                                                                                                                                                                                          |
| 3   | BT_UART_TXD   | O    | BT_UART_TXD               | UART serial output. Serial data output for the HCI UART interface.                                                                                                                                                                                                                        |
| 4   | BT_UART_CTS_N | I    | BT_UART_CTS_N             | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.                                                                                                                                                                                                           |
| 5   | BT_UART_RTS_N | O    | BT_UART_RTS_N             | UART request-to-send. Active-low request-to-send signal for the HCI UART interface.                                                                                                                                                                                                       |
| 6   | NC            |      |                           |                                                                                                                                                                                                                                                                                           |
| 7   | NC            |      |                           |                                                                                                                                                                                                                                                                                           |
| 8   | BT_PCM_SYNC   | I/O  | BT_PCM_SYNC               | PCM sync; can be master (output) or slave (input)                                                                                                                                                                                                                                         |
| 9   | BT_PCM_IN     | I    | BT_PCM_IN                 | PCM data input sensing                                                                                                                                                                                                                                                                    |
| 10  | BT_PCM_OUT    | O    | BT_PCM_OUT                | PCM data output                                                                                                                                                                                                                                                                           |
| 11  | BT_PCM_CLK    | I/O  | BT_PCM_CLK                | PCM clock; can be master (output) or slave (input)                                                                                                                                                                                                                                        |
| 12  | GND           |      |                           |                                                                                                                                                                                                                                                                                           |
| 13  | NC            |      |                           |                                                                                                                                                                                                                                                                                           |
| 14  | BT_REG_ON     | I    | BT_REG_ON                 | Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when de-asserted, this pin holds the Bluetooth section in reset. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 15  | NC            |      |                           |                                                                                                                                                                                                                                                                                           |

| No.           | Pin name                | Type | Connection to IC Pin Name    | Description                                                                                                                                                                                                                                                                     |
|---------------|-------------------------|------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16            | NC                      |      |                              |                                                                                                                                                                                                                                                                                 |
| 17            | WL_GPIO_2               |      | GPIO_2                       |                                                                                                                                                                                                                                                                                 |
| 18            | WL_GPIO_1               |      | GPIO_1                       |                                                                                                                                                                                                                                                                                 |
| 19            | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 20            | SDIO_CLK                | I    |                              | SDIO clock input.                                                                                                                                                                                                                                                               |
| 21            | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 22            | SDIO_CMD                | I/O  | SDIO_CMD                     | SDIO command line                                                                                                                                                                                                                                                               |
| 23            | SDIO_DATA_2             | I/O  | SDIO_DATA_2                  | SDIO data line 2                                                                                                                                                                                                                                                                |
| 24            | SDIO_DATA_0             | I/O  | SDIO_DATA_0                  | SDIO data line 0                                                                                                                                                                                                                                                                |
| 25            | SDIO_DATA_3             | I/O  | SDIO_DATA_3                  | SDIO data line 3                                                                                                                                                                                                                                                                |
| 26            | SDIO_DATA_1             | I/O  | SDIO_DATA_1                  | SDIO data line 1                                                                                                                                                                                                                                                                |
| 27            | WL_GPIO_0_HO<br>ST_WAKE |      | GPIO_0                       |                                                                                                                                                                                                                                                                                 |
| 28            | WL_REG_ON               | I    | WL_REG_ON                    | Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 29            | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 30            | VBAT                    |      | LDO_VDDBAT5V,<br>SR_VDDBAT5V |                                                                                                                                                                                                                                                                                 |
| 31            | VIN_LDO                 |      | LDO_VDD1P5,<br>WLRV_VDD_1P35 |                                                                                                                                                                                                                                                                                 |
| 32            | GND (SR_PVSS)           |      |                              |                                                                                                                                                                                                                                                                                 |
| 33            | GND (SR_PVSS)           |      |                              |                                                                                                                                                                                                                                                                                 |
| 34            | SR_VLX                  |      | SR_VLX                       | CBUCK switching regulator output.                                                                                                                                                                                                                                               |
| 35            | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 36            | VIO                     |      | SCC_VDDIO,<br>SYS_VDDIO      |                                                                                                                                                                                                                                                                                 |
| 37            | LPO_IN (32 kHz)         | I    | LPO_IN                       | External sleep clock input (32.768kHz).                                                                                                                                                                                                                                         |
| 38            | BT_HOST_WAKE            | I/O  | BT_HOST_WAKE                 | HOST_WAKE or general-purpose I/O signal                                                                                                                                                                                                                                         |
| 39            | BT_DEV_WAKE             | I/O  | BT_DEV_WAKE                  | DEV_WAKE or general-purpose I/O signal                                                                                                                                                                                                                                          |
| 40            | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 41            | ANT                     |      |                              |                                                                                                                                                                                                                                                                                 |
| 42<br>~<br>46 | GND                     |      |                              |                                                                                                                                                                                                                                                                                 |

## 7.3 SDIO Pin Descriptions

This section describes the SDIO pins and UART connections. **Table 8** shows the SDIO pin descriptions.

**Table 8: SDIO Pin Descriptions**

| No. | Pin Name | (i) SD 4-bit Mode |       | (ii) SD 1-bit Mode |       |
|-----|----------|-------------------|-------|--------------------|-------|
| 20  | SDIO_CLK | CLK               | Clock | CLK                | Clock |

| No. | Pin Name | (i) SD 4-bit Mode |                        | (ii) SD 1-bit Mode |              |
|-----|----------|-------------------|------------------------|--------------------|--------------|
| 24  | SDIO_D0  | DATA0             | Data line 0            | DATA               | Data line    |
| 26  | SDIO_D1  | DATA1             | Data line 1 /Interrupt | IRQ                | Interrupt    |
| 23  | SDIO_D2  | DATA2             | Data line 2            | NC                 | Not used     |
| 25  | SDIO_D3  | DATA3             | Data line 3            | NC                 | Not used     |
| 22  | SDIO_CMD | CMD               | Command line           | CMD                | Command line |

Figure 5 shows the SDIO pins.

Figure 5: SDIO Pins

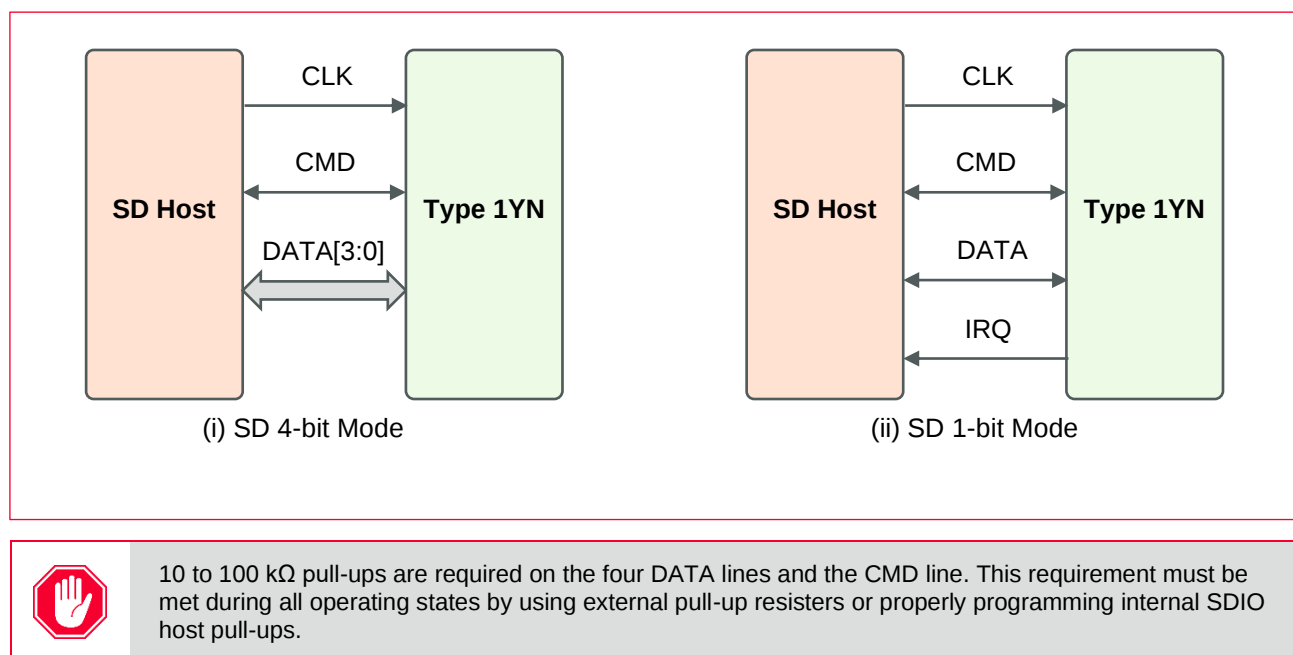
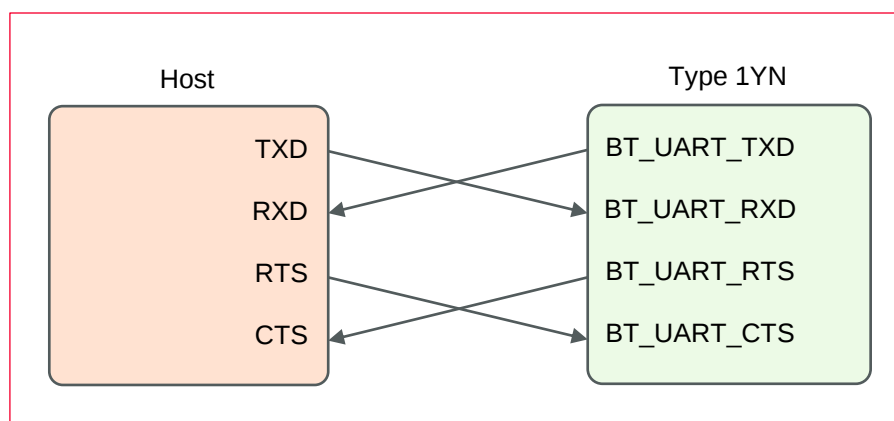


Figure 6 shows the UART connections.

Figure 6: UART Connection



## 8 Absolute Maximum Ratings

The absolute and maximum ratings are shown in **Table 9**.

**Table 9: Absolute Maximum Ratings**

| Parameter           |       | Minimum | Maximum | Unit |
|---------------------|-------|---------|---------|------|
| Storage Temperature |       | -40     | +85     | °C   |
| Supply Voltage      | VBAT  | -0.5    | 5.0     | V    |
|                     | VDDIO | -0.5    | 3.9     | V    |



Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

## 9 Operating Conditions

The operating conditions are shown in **Table 10**.

**Table 10: Operating Conditions**

| Parameter                       |       | Minimum | Typical    | Maximum | Unit |
|---------------------------------|-------|---------|------------|---------|------|
| Operating Temperature Range     |       | -40     | +25        | +85     | °C   |
| Specification Temperature Range |       | -10     | +25        | +55     | °C   |
| Operating Voltage               | VBAT  | 3.0     | 3.6        | 4.8     | V    |
|                                 | VDDIO | 1.71    | 1.8 or 3.3 | 3.63    | V    |
| Specification Voltage           | VBAT  | 3.2     | 3.6        | 4.2     | V    |
|                                 | VDDIO | 1.71    | 1.8 or 3.3 | 3.63    | V    |



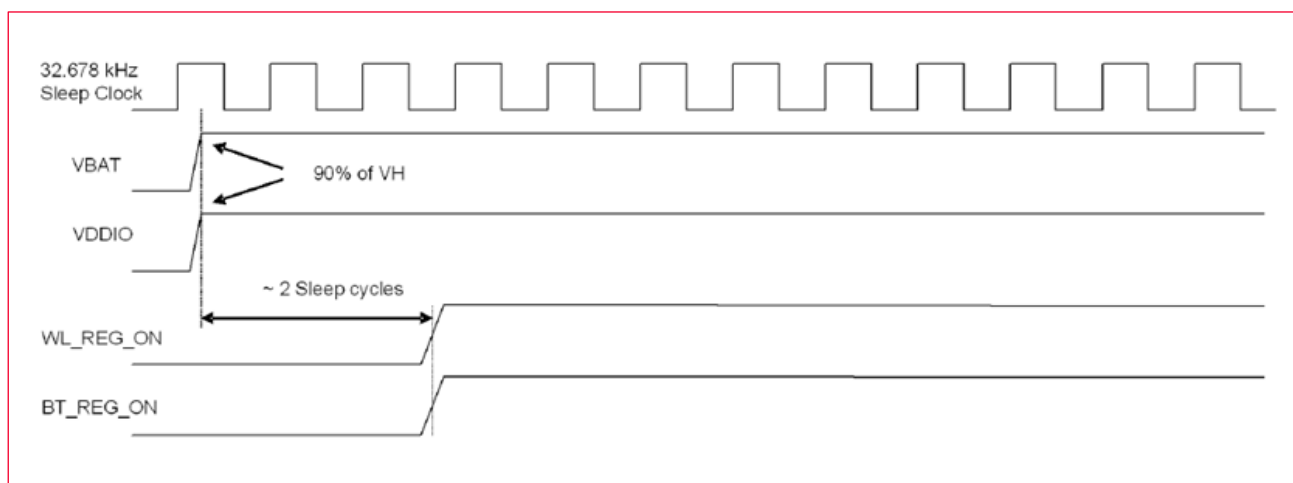
All RF characteristics in this datasheet are defined by Specification Temperature Range and Specification Voltage.

## 10 Power-On Sequences

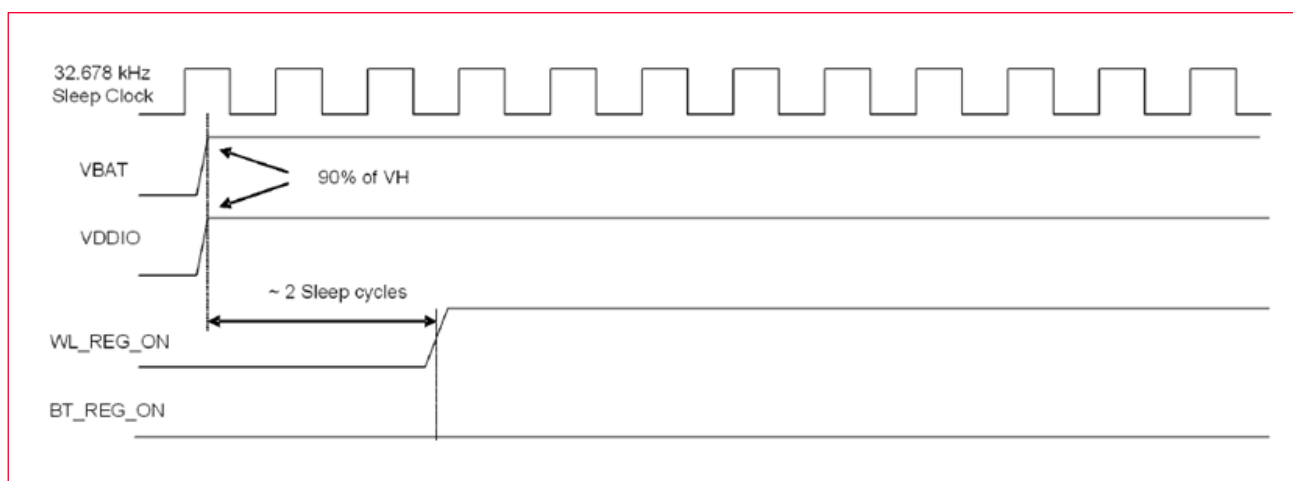
This section describes the power-on sequences along with their parameters.

- VBAT should not rise 10%-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VIO. VIO should NOT be present fast or be held high before VBAT is high.

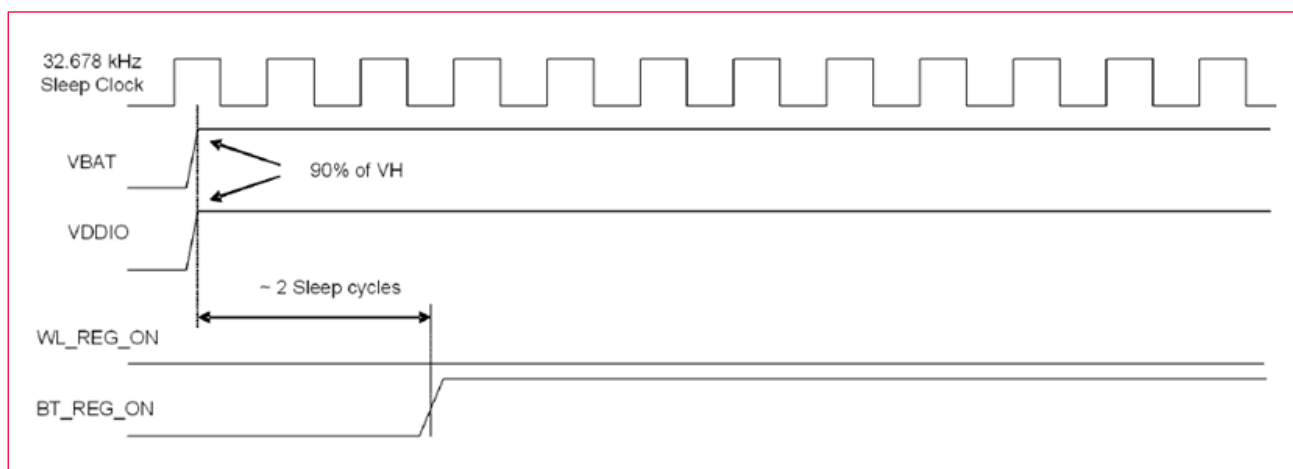
**Figure 7** shows the power-on sequence graphs for WLAN ON and BT ON.

**Figure 7: Power-On Sequence Graph - WLAN ON and BT ON**

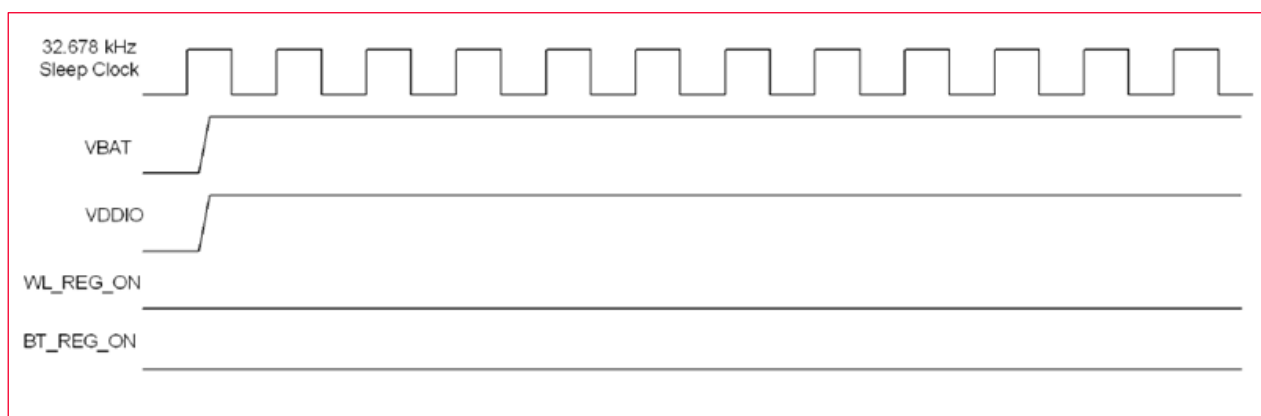
**Figure 8** shows the power-on sequence graph for WLAN ON and BT OFF.

**Figure 8: Power-On Sequence Graph - WLAN ON and BT OFF**

**Figure 9** shows the power-on sequence graph for WLAN OFF and BT ON.

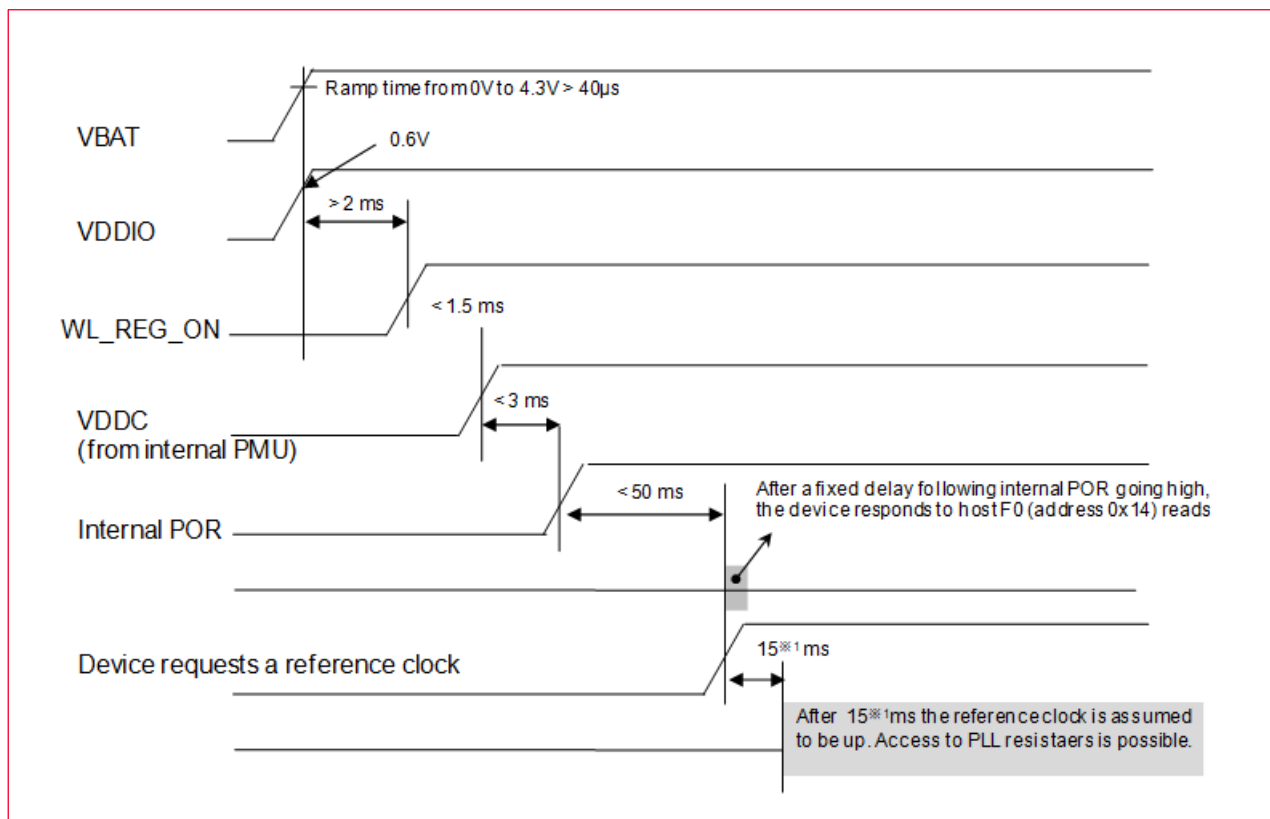
**Figure 9: Power-On Sequence Graph - WLAN OFF and BT ON**

**Figure 10** shows the power-on sequence graph for WLAN OFF and BT OFF.

**Figure 10: Power-On Sequence Graph - WLAN OFF and BT OFF**

**Figure 11** shows the WLAN boot up sequence.

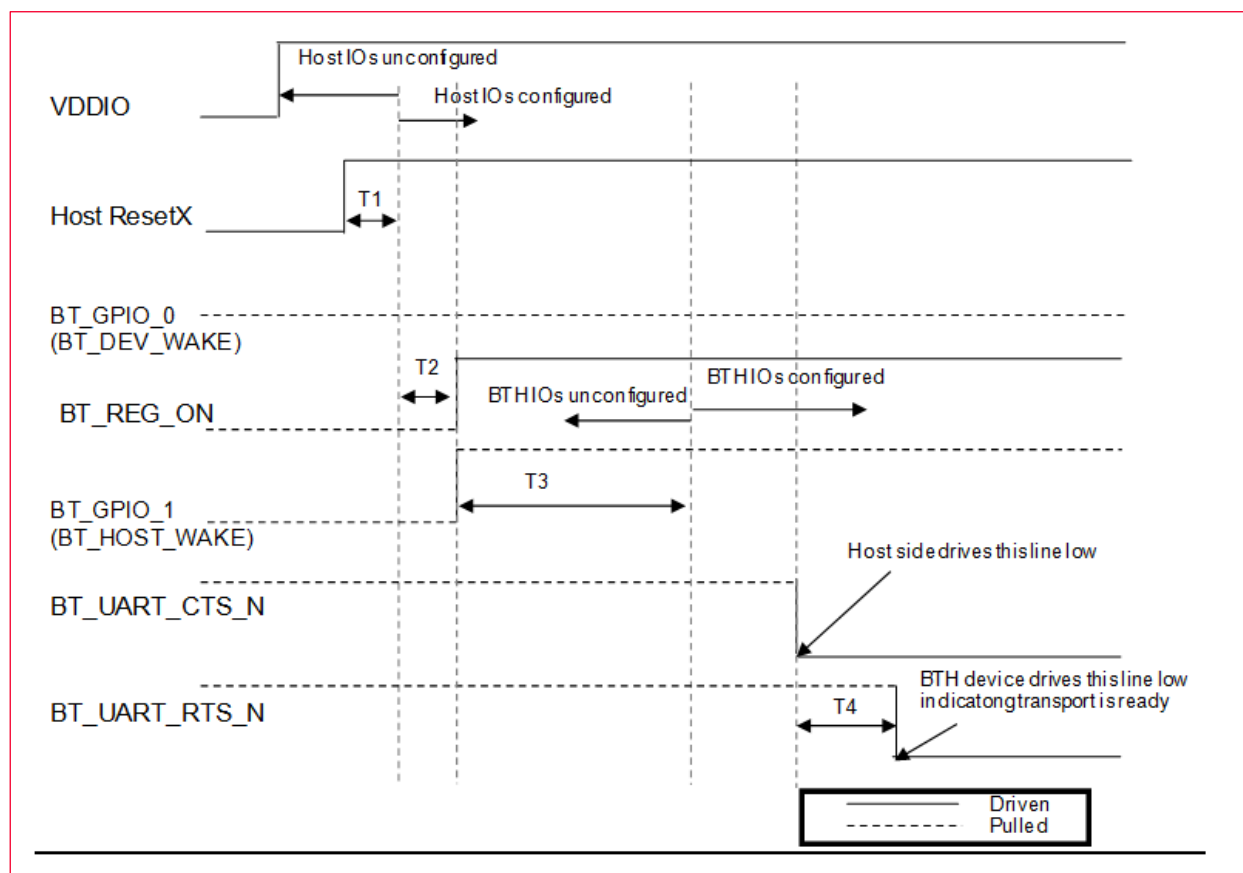
**Figure 11: WLAN Boot Up Sequence**



1 This wait time is programmable in sleep-clock increments from 1 to 255 (30 μs to 15 milliseconds).

Figure 12 shows the startup signaling sequence.

Figure 12: Startup Signaling Sequence



- T1 is the time for host to settle its IOs after a reset.
- T2 is the time for host to drive BT\_REG\_ON high after the Host IOs are configured.
- T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.
- T4 is the time for BTH device to drive BT\_UART\_RTS\_N low after the host drives BT\_UART\_CTS\_N low. This assumes the BTH device has already completed initialization.



Timing diagram assumes VBAT is present.

## 11 Digital I/O Requirements

**Table 11** shows the digital I/O requirements for Type 1YN module.

**Table 11: Digital I/O Requirement Pins**

| SDIO Interface I/O Pins            | Symbol          | Minimum     | Maximum     | Unit |
|------------------------------------|-----------------|-------------|-------------|------|
| Input low voltage (VDDIO = 3.3V)   | V <sub>IL</sub> |             | 0.25*VDDIO  | V    |
| Input high voltage (VDDIO = 3.3V)  | V <sub>IH</sub> | 0.625*VDDIO |             | V    |
| Input low voltage (VDDIO = 1.8V)   | V <sub>IL</sub> |             | 0.58        | V    |
| Input high voltage (VDDIO = 1.8V)  | V <sub>IH</sub> | 1.27        |             | V    |
| Output low voltage (VDDIO = 3.3V)  | V <sub>OL</sub> |             | 0.125*VDDIO | V    |
| Output high voltage (VDDIO = 3.3V) | V <sub>OH</sub> | 0.75*VDDIO  |             | V    |
| Output low voltage (VDDIO = 1.8V)  | V <sub>OL</sub> |             | 0.45        | V    |
| Output high voltage (VDDIO = 1.8V) | V <sub>OH</sub> | 1.40        |             | V    |

**Table 12** shows the other digital I/O pins.

**Table 12: Other Digital I/O Pins**

| Other Digital I/O Pins             | Symbol          | Minimum    | Maximum    | Unit |
|------------------------------------|-----------------|------------|------------|------|
| Input low voltage (VDDIO = 3.3V)   | V <sub>IL</sub> |            | 0.8        | V    |
| Input high voltage (VDDIO = 3.3V)  | V <sub>IH</sub> | 2.0        |            | V    |
| Input low voltage (VDDIO = 1.8V)   | V <sub>IL</sub> |            | 0.35*VDDIO | V    |
| Input high voltage (VDDIO = 1.8V)  | V <sub>IH</sub> | 0.65*VDDIO |            | V    |
| Output low voltage (VDDIO = 3.3V)  | V <sub>OL</sub> |            | 0.40       | V    |
| Output high voltage (VDDIO = 3.3V) | V <sub>OH</sub> | VDDIO-0.4  |            | V    |
| Output low voltage (VDDIO = 1.8V)  | V <sub>OL</sub> |            | 0.45       | V    |
| Output high voltage (VDDIO = 1.8V) | V <sub>OH</sub> | VDDIO-0.45 |            | V    |

## 12 External Sleep Clock Requirement

**Table 13** shows the external LPO specification for Type 1YN module.

**Table 13: External LPO Specification**

| Parameter                    | Condition/Notes          | Specification |         |         |         |
|------------------------------|--------------------------|---------------|---------|---------|---------|
|                              |                          | Minimum       | Typical | Maximum | Units   |
| Frequency                    |                          |               | 32.768  |         | KHz     |
| Frequency accuracy           |                          | -200          |         | +200    | ppm     |
| Duty Cycle                   |                          | 30            |         | 70      | %       |
| Input amplitude              |                          | 200           |         | 3300    | mV, p-p |
| Signal type                  | Square wave or sine wave |               |         |         |         |
| Input impedance <sup>1</sup> | Resistive                | 100           |         |         | kΩ      |
|                              | Capacitive               |               |         | 5       | pF      |
| Clock jitter                 |                          |               |         | 10,000  | ppm     |

<sup>1</sup> When power is applied or switched off.

## 13 Interface Timing

This section describes the interface timing, its speed modes, related parameters, and graphs.

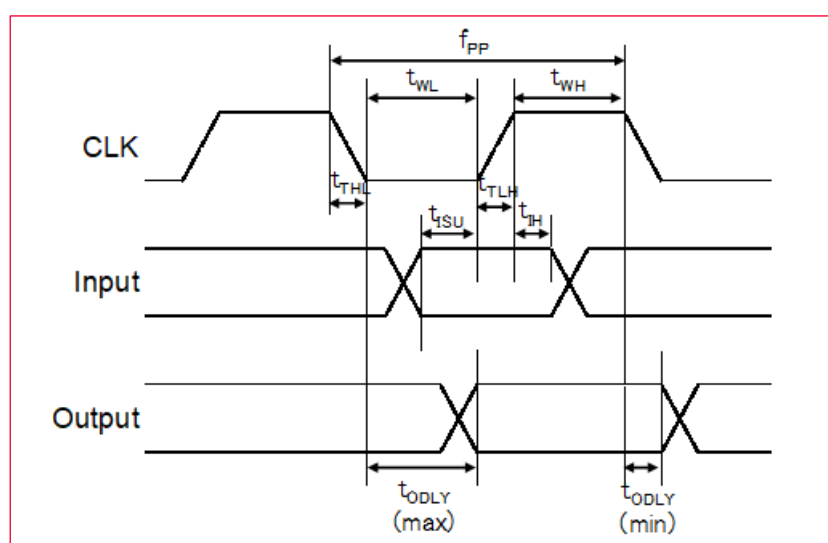
### 13.1 SDIO Timing

This section describes the SDIO timings for different modes.

#### 13.1.1 Default Mode

The default mode is shown in **Figure 13**.

**Figure 13: SDIO Timing Diagram - Default Mode**



**Table 14** Table 13 shows the SDIO timing parameters in default mode.

**Table 14: SDIO Timing Parameters - Default Mode**

| Parameter                                                                 | Symbol     | Minimum | Typical | Maximum | Unit |
|---------------------------------------------------------------------------|------------|---------|---------|---------|------|
| <b>Clock CLK (All values are referred to minimum VIH and maximum VIL)</b> |            |         |         |         |      |
| Frequency-Data Transfer Mode                                              | $f_{PP}$   | 0       |         | 25      | MHz  |
| Frequency-Identification Mode                                             | $f_{OD}$   | 0       |         | 400     | kHz  |
| Clock Low Time                                                            | $t_{WL}$   | 10      |         |         | ns   |
| Clock High Time                                                           | $t_{WH}$   | 10      |         |         | ns   |
| Clock Rise Time                                                           | $t_{TLH}$  |         |         | 10      | ns   |
| Clock Fall Time                                                           | $t_{THL}$  |         |         | 10      | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                               |            |         |         |         |      |
| Input Setup Time                                                          | $t_{SU}$   | 5       |         |         | ns   |
| Input Hold Time                                                           | $t_{H}$    | 5       |         |         | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                              |            |         |         |         |      |
| Output Delay Time-Data Transfer Mode                                      | $t_{ODLY}$ | 0       |         | 14      | ns   |

| Parameter                             | Symbol     | Minimum | Typical | Maximum | Unit |
|---------------------------------------|------------|---------|---------|---------|------|
| Output Delay Time-Identification Mode | $t_{ODLY}$ | 0       |         | 50      | ns   |

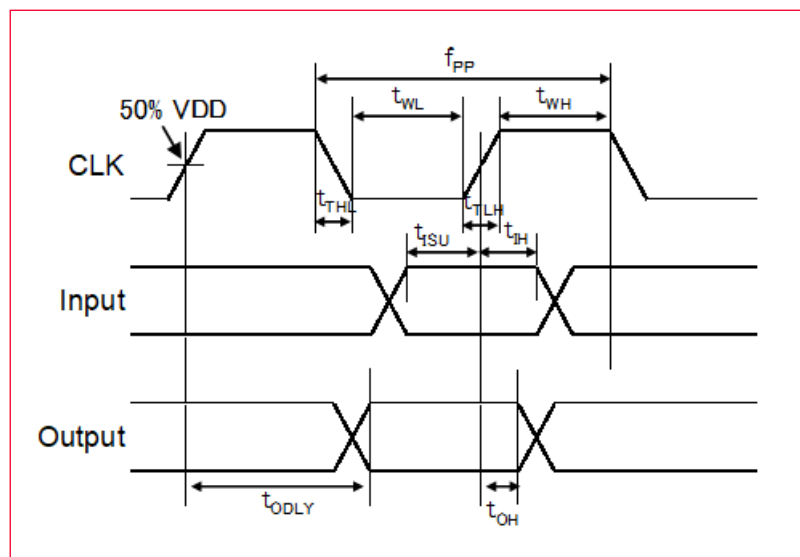


Timing is based on  $CL < 40$  pF load on CMD and Data.  
 Minimum ( $V_{ih}$ ) =  $0.7 \cdot V_{DDIO}$  and maximum ( $V_{il}$ ) =  $0.2 \cdot V_{DDIO}$

### 13.1.2 High Speed Mode

**Figure 14** shows the SDIO timing diagram in high-speed mode.

**Figure 14: SDIO Timing Diagram - High Speed Mode**



**Table 15** shows the SDIO timing parameters in high-speed mode.

**Table 15: SDIO Timing Parameters - High Speed Mode**

| Parameter                                                                                                 | Symbol    | Minimum | Typical | Maximum | Unit |
|-----------------------------------------------------------------------------------------------------------|-----------|---------|---------|---------|------|
| <b>Clock CLK (All values are referred to minimum <math>V_{IH}</math> and maximum <math>V_{IL}</math>)</b> |           |         |         |         |      |
| Frequency-Data Transfer Mode                                                                              | $f_{PP}$  | 0       |         | 50      | MHz  |
| Frequency-Identification Mode                                                                             | $f_{OD}$  | 0       |         | 400     | kHz  |
| Clock Low Time                                                                                            | $t_{WL}$  | 7       |         |         | ns   |
| Clock High Time                                                                                           | $t_{WH}$  | 7       |         |         | ns   |
| Clock Rise Time                                                                                           | $t_{TLH}$ |         |         | 3       | ns   |
| Clock Fall Time                                                                                           | $t_{THL}$ |         |         | 3       | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                                                               |           |         |         |         |      |
| Input Setup Time                                                                                          | $t_{SU}$  | 6       |         |         | ns   |
| Input Hold Time                                                                                           | $t_{H}$   | 2       |         |         | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                                                              |           |         |         |         |      |

| Parameter                            | Symbol     | Minimum | Typical | Maximum | Unit |
|--------------------------------------|------------|---------|---------|---------|------|
| Output Delay Time-Data Transfer Mode | $t_{ODLY}$ |         |         | 14      | ns   |
| Output Hold time                     | $t_{OH}$   | 2.5     |         |         | ns   |
| Total System Capacitance (each line) | CL         |         |         | 40      | pF   |

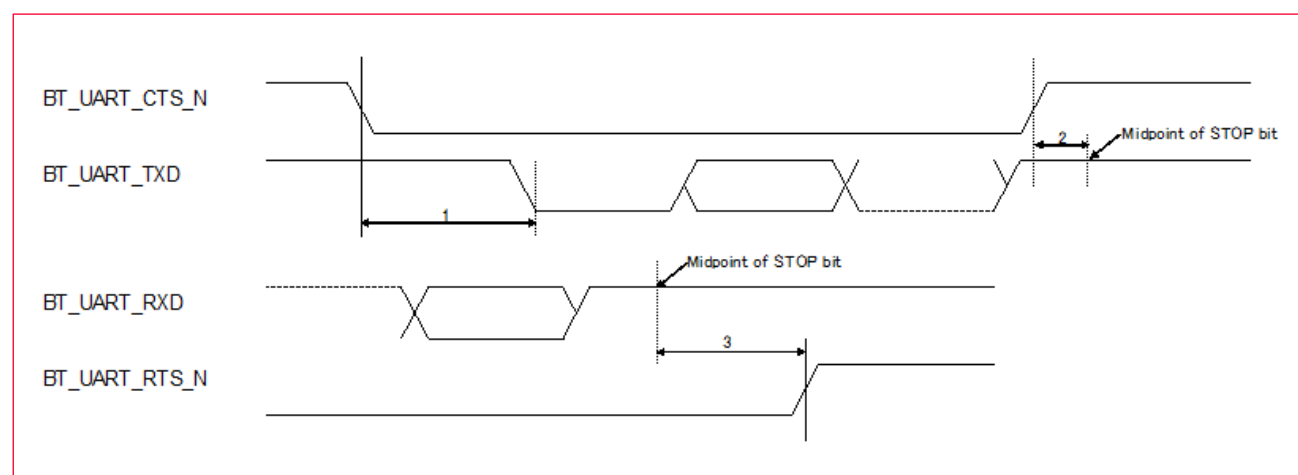


Timing is based on CL < 40 pF load on CMD and Data.  
 Minimum (V<sub>IH</sub>) = 0.7\*VDDIO and maximum (V<sub>IL</sub>) = 0.2\*VDDIO

## 13.2 Bluetooth UART Timing - Default Mode

Bluetooth UART timing diagram in default mode is shown in **Figure 15**.

**Figure 15: Bluetooth UART Timing Diagram - Default Mode**



Bluetooth UART timing parameters in default mode are shown in **Table 16**.

**Table 16: Bluetooth UART Timing Parameters - Default Mode**

| Reference | Description                                             | Minimum | Typical | Maximum | Unit        |
|-----------|---------------------------------------------------------|---------|---------|---------|-------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid            |         |         | 1.5     | Bit periods |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit |         |         | 0.5     | Bit periods |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high     |         |         | 0.5     | Bit periods |

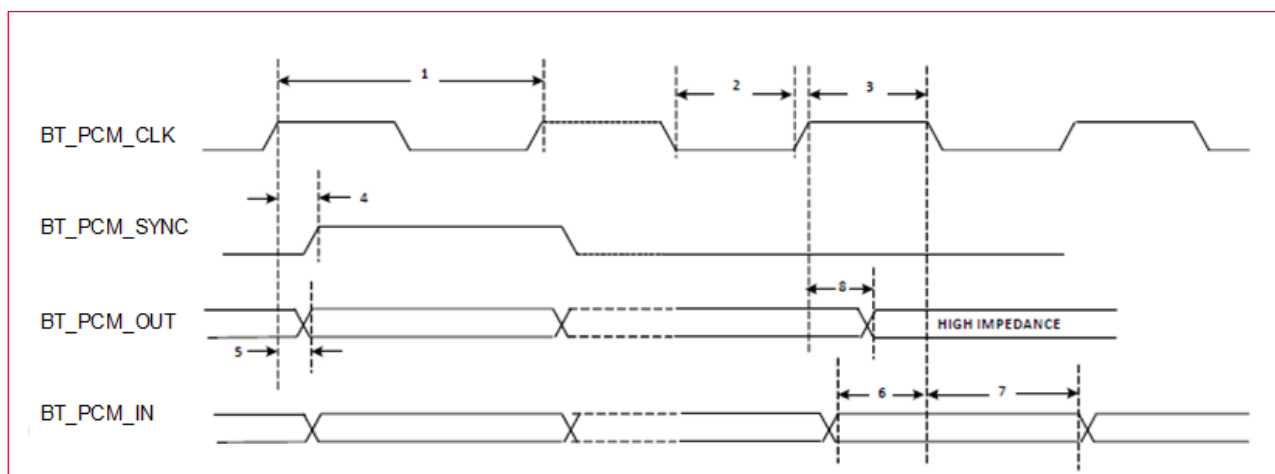
## 13.3 Bluetooth PCM Timing

This section describes the Bluetooth PCM timing sync signals along with their parameters for both long frame and short frame, as well as master and slave modes.

### 13.3.1 PCM Timing Short Frame Sync - Master Mode

**Figure 16** shows the PCM short frame sync signal in master mode.

**Figure 16: PCM Timing Short Frame Sync Signal - Master Mode**



**Table 17** lists information about PCM short frame sync in master mode.

**Table 17: Symbol Definitions for PCM Timing Short Frame Sync Signal - Master Mode**

| Reference | Description                                                                                 | Minimum | Typical | Maximum | Unit |
|-----------|---------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                     |         |         | 12      | MHz  |
| 2         | PCM bit clock Low                                                                           | 41      |         |         | ns   |
| 3         | PCM bit clock High                                                                          | 41      |         |         | ns   |
| 4         | PCM_SYNC delay                                                                              | 0       |         | 25      | ns   |
| 5         | PCM_OUT delay                                                                               | 0       |         | 25      | ns   |
| 6         | PCM_IN setup                                                                                | 8       |         |         | ns   |
| 7         | PCM_IN hold                                                                                 | 8       |         |         | ns   |
| 8         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0       |         | 25      | ns   |

### 13.3.2 PCM Timing Short Frame Sync - Slave Mode

Figure 17 shows the PCM short frame sync signal in slave mode.

Figure 17: PCM Timing Short Frame Sync Signal - Slave Mode

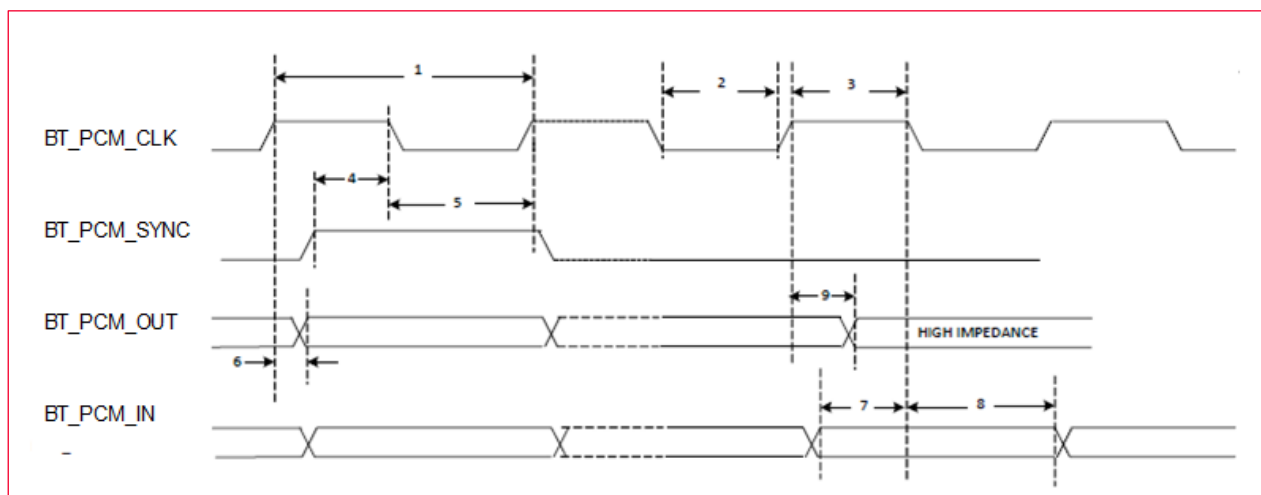


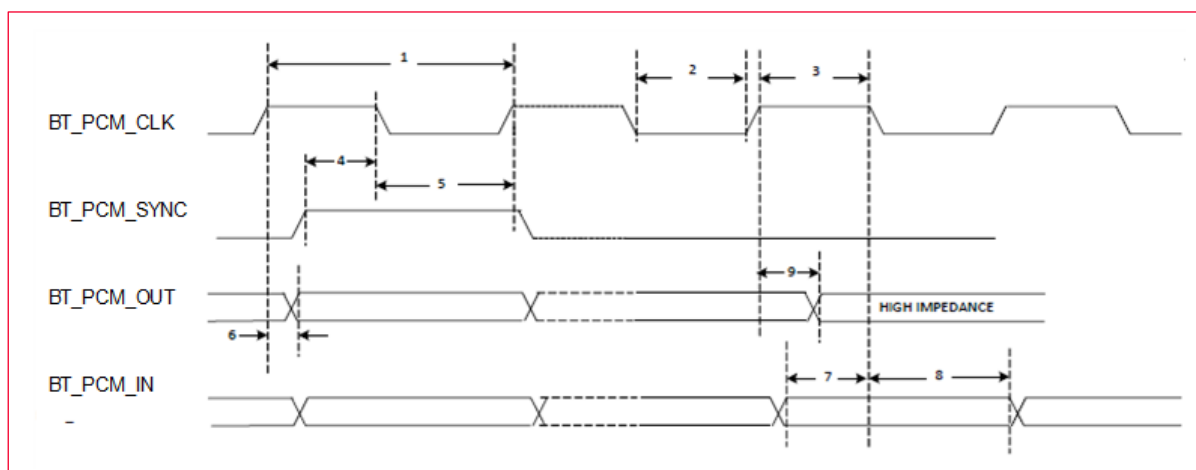
Table 18 lists information about PCM short frame sync in slave mode.

Table 18: Symbol Definitions for PCM Timing Short Frame Sync Signal - Slave Mode

| Reference | Description                                                                                 | Minimum | Typical | Maximum | Unit |
|-----------|---------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                     |         |         | 12      | MHz  |
| 2         | PCM bit clock Low                                                                           | 41      |         |         | ns   |
| 3         | PCM bit clock High                                                                          | 41      |         |         | ns   |
| 4         | PCM_SYNC setup                                                                              | 8       |         |         | ns   |
| 5         | PCM_SYNC hold                                                                               | 8       |         |         | ns   |
| 6         | PCM_OUT delay                                                                               | 0       |         | 25      | ns   |
| 7         | PCM_IN setup                                                                                | 8       |         |         | ns   |
| 8         | PCM_IN hold                                                                                 | 8       |         |         | ns   |
| 9         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0       |         | 25      | ns   |

### 13.3.3 PCM Timing Long Frame Sync - Master Mode

Figure 18 shows the PCM long frame sync signal in master mode.

**Figure 18: PCM Timing Long Frame Sync Signal - Master Mode**

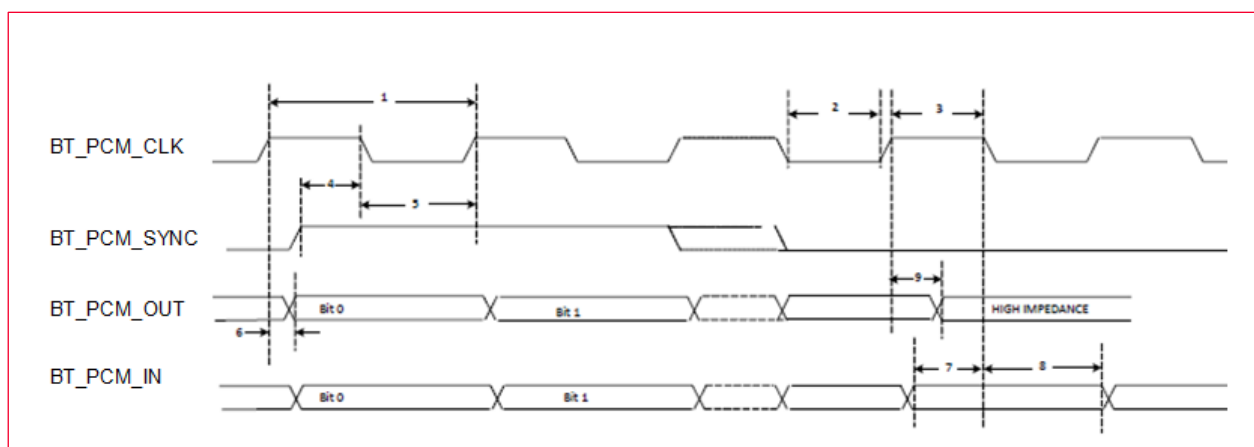
**Table 19** lists information about PCM long frame sync in master mode.

**Table 19: Symbol Definitions for PCM Timing Long Frame Sync Signal - Master Mode**

| Reference | Description                                                                                 | Minimum | Typical | Maximum | Unit |
|-----------|---------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                     |         |         | 12      | MHz  |
| 2         | PCM bit clock low                                                                           | 41      |         |         | ns   |
| 3         | PCM bit clock high                                                                          | 41      |         |         | ns   |
| 4         | PCM_SYNC delay                                                                              | 0       |         | 25      | ns   |
| 5         | PCM_OUT delay                                                                               | 0       |         | 25      | ns   |
| 6         | PCM_IN setup                                                                                | 8       |         |         | ns   |
| 7         | PCM_IN hold                                                                                 | 8       |         |         | ns   |
| 8         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0       |         | 25      | ns   |

### 13.3.4 PCM Timing Long Frame Sync - Slave Mode

**Figure 19** shows PCM long frame sync signal in slave mode.

**Figure 19: PCM Timing Long Frame Sync Signal - Slave Mode**

**Table 20** lists information about PCM short frame sync in slave mode.

**Table 20: Symbol Definitions for PCM Timing Long Frame Sync Signal - Slave Mode**

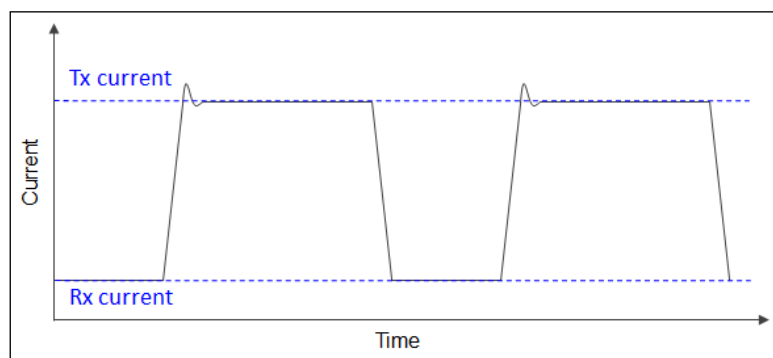
| Reference | Description                                                                                 | Minimum | Typical | Maximum | Unit |
|-----------|---------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                     |         |         | 12      | MHz  |
| 2         | PCM bit clock low                                                                           | 41      |         |         | ns   |
| 3         | PCM bit clock high                                                                          | 41      |         |         | ns   |
| 4         | PCM_SYNC setup                                                                              | 8       |         |         | ns   |
| 5         | PCM_SYNC hold                                                                               | 8       |         |         | ns   |
| 6         | PCM_OUT delay                                                                               | 0       |         | 25      | ns   |
| 7         | PCM_IN setup                                                                                | 8       |         |         | ns   |
| 8         | PCM_IN hold                                                                                 | 8       |         |         | ns   |
| 9         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0       |         | 25      | ns   |

## 14 DC/RF Characteristics

This section describes the electrical characteristics of the Type 1YN module.

Burst current definition is shown in **Figure 20**.

**Figure 20: Burst Current Definition**



### 14.1 DC/RF Characteristics for IEEE 802.11b

**Table 21: Characteristics Values for IEEE 802.11b**

| Items         | Contents           |
|---------------|--------------------|
| Specification | IEEE 802.11b       |
| Mode          | DSSS / CCK         |
| Frequency     | 2400 - 2483.5 MHz  |
| Data Rate     | 1, 2, 5.5, 11 Mbps |

**Conditions:** 25 °C, VBAT = 3.6V, VDDIO = 3.3V, Output power setting = 17 dBm, 11 Mbps mode

**Table 22: DC/RF Characteristics for IEEE 802.11b**

| Items                                 | Contents |         |         |      |
|---------------------------------------|----------|---------|---------|------|
| DC Characteristics                    | Minimum  | Typical | Maximum | Unit |
| DC Current                            |          |         |         |      |
| • Tx mode (1024 byte, 20 μs interval) |          | 320     | 370     | mA   |
| • Rx mode                             |          | 47      | 60      | mA   |
| TX Characteristics                    | Minimum  | Typical | Maximum | Unit |
| Output Power (Tolerance)              | 15       | 17      | 19      | dBm  |
| Spectrum Mask Margin                  |          |         |         |      |
| • 1st side lobes (-30 dBr)            | 0        |         |         | dB   |
| • 2nd side lobes (-50 dBr)            | 0        |         |         | dB   |
| Power-on and Power-off ramp           |          |         | 2.0     | μs   |
| RF Carrier Suppression                | 15       |         |         | dB   |
| Modulation Accuracy (EVM)             |          | 15      | 35      | %    |
| Spurious Emissions                    |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)          |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)          |          |         | -54     | dBm  |

| Items                                 | Contents |         |         |      |
|---------------------------------------|----------|---------|---------|------|
| • 74 - 87.5 MHz (BW = 100 kHz)        |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)       |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)        |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)        |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)        |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)        |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)       |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)       |          |         | -30     | dBm  |
| Rx Characteristics                    | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level (FER ≤ 8%)        |          | -89     | -76     | dBm  |
| Maximum Input Level (FER ≤ 8%)        | -10      |         |         | dBm  |
| Adjacent Channel Rejection (FER ≤ 8%) | 35       |         |         | dB   |

## 14.2 DC/RF Characteristics for IEEE 802.11g

**Table 23: Characteristics Values for IEEE 802.11g**

| Items         | Contents                          |
|---------------|-----------------------------------|
| Specification | IEEE 802.11g                      |
| Mode          | OFDM                              |
| Frequency     | 2400 - 2483.5 MHz                 |
| Data Rate     | 6, 9, 12, 18, 24, 36, 48, 54 Mbps |

**Conditions:** 25 °C, VBAT = 3.6V, VDDIO = 3.3V, Output power setting = 13 dBm, 54 Mbps mode

**Table 24: DC/RF Characteristics for IEEE 802.11g**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 270     | 310     | mA   |
| • Rx mode                                   |          | 47      | 60      | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power (Tolerance)                    | 11       | 13      | 15      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          | -30     | -25     | dB   |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level (PER $\leq$ 10%)        |          | -75     | -65     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -1       |         |         | dB   |

## 14.3 DC/RF Characteristics for IEEE 802.11n

**Table 25: Characteristics Values for IEEE 802.11n**

| Items         | Contents                                 |
|---------------|------------------------------------------|
| Specification | IEEE 802.11n                             |
| Mode          | OFDM                                     |
| Frequency     | 2400 - 2483.5 MHz                        |
| Data Rate     | 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps |

**Conditions:** 25 °C, VBAT = 3.6V, VDDIO = 3.3V, Output power setting = 12 dBm, 65 Mbps mode

**Table 26: DC/RF Characteristics for IEEE 802.11n**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 260     | 300     | mA   |
| • Rx mode                                   |          | 47      | 60      | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power (Tolerance)                    | 10       | 12      | 14      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          | -31     | -27     | dB   |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level (PER $\leq$ 10%)        |          | -73     | -64     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -2       |         |         | dB   |

## 14.4 DC/RF Characteristics for Bluetooth

**Normal conditions:** 25 °C, VBAT = 3.6V, VDDIO = 3.3V

**Table 27: DC/RF Characteristics for Bluetooth**

| Items                                                          | Contents                 |                |                |             |
|----------------------------------------------------------------|--------------------------|----------------|----------------|-------------|
| Bluetooth Specification (power class)                          | Ver 5.1 (Class 1)        |                |                |             |
| Channel Frequency (spacing)                                    | 2402 to 2480 MHz (1 MHz) |                |                |             |
| Current Consumption                                            | Minimum                  | Typical        | Maximum        | Unit        |
| • Tx = Rx = DH5 (fully occupied)                               |                          | 28             | 60             | mA          |
| • Tx = Rx = 2DH5 (fully occupied)                              |                          | 25             | 50             | mA          |
| • Tx = Rx = 3DH5 (fully occupied)                              |                          | 25             | 50             | mA          |
| <b>Transmitter</b>                                             | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| Output Power                                                   | 6                        | 10             | 14             | dBm         |
| Frequency Range                                                | 2400                     |                | 2483.5         | MHz         |
| 20 dB Bandwidth                                                |                          |                | 1              | MHz         |
| Adjacent Channel Power <sup>2</sup>                            |                          |                |                |             |
| [M-N] = 2                                                      |                          |                | -20            | dBm         |
| [M-N] ≥ 3                                                      |                          |                | -40            | dBm         |
| <b>Modulation Characteristics</b>                              | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| • Modulation $\Delta f_{1\text{avg}}$                          | 140                      |                | 175            | kHz         |
| • Modulation $\Delta f_{2\text{max}}$                          | 115                      |                |                | kHz         |
| • Modulation $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                      |                |                |             |
| <b>Carrier Frequency Drift</b>                                 | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| • 1slot                                                        | -25                      |                | +25            | kHz         |
| • 3slot / 5slot                                                | -40                      |                | +40            | kHz         |
| • Maximum drift rate                                           |                          |                | +20            | kHz/50μs    |
| EDR Relative Power                                             | -4                       |                | +1             | dB          |
| EDR Carrier Frequency Stability and Modulation Accuracy        |                          |                |                |             |
| • $\omega_i$                                                   | -75                      |                | +75            | kHz         |
| • $\omega_i + \omega_o$                                        | -75                      |                | +75            | kHz         |
| • $\omega_o$                                                   | -10                      |                | +10            | kHz         |
| • RMS DEVM (DQPSK)                                             |                          |                | 20             | %           |
| • Peak DEVM (DQPSK)                                            |                          |                | 35             | %           |
| • 99% DEVM (DQPSK)                                             |                          |                | 30             | %           |
| • RMS DEVM (8DPSK)                                             |                          |                | 13             | %           |
| • Peak DEVM (8DPSK)                                            |                          |                | 25             | %           |
| • 99% DEVM (8DPSK)                                             |                          |                | 20             | %           |
| Spurious Emissions                                             |                          |                |                |             |
| • 30 - 47 MHz (BW = 100 kHz)                                   |                          |                | -36            | dBm         |
| • 47 - 74 MHz (BW = 100 kHz)                                   |                          |                | -54            | dBm         |
| • 74 - 87.5 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |
| • 87.5 - 118 MHz (BW = 100 kHz)                                |                          |                | -54            | dBm         |
| • 118 - 174 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |
| • 174 - 230 MHz (BW = 100 kHz)                                 |                          |                | -54            | dBm         |
| • 230 - 470 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |

<sup>2</sup> Up to three spurious responses within Bluetooth limits are allowed.

| Items                                     | Contents |         |         |         |
|-------------------------------------------|----------|---------|---------|---------|
| • 470 - 862 MHz (BW = 100 kHz)            |          |         | -54     | dBm     |
| • 862 - 1000 MHz (BW = 100 kHz)           |          |         | -36     | dBm     |
| • 1000 - 12750 MHz (BW = 1 MHz)           |          |         | -30     | dBm     |
| Receiver                                  | Minimum  | Typical | Maximum | Minimum |
| Sensitivity (BER ≤ 0.1%)                  |          | -91     | -80     | dBm     |
| C/I Performance (BER ≤ 0.1%) <sup>3</sup> |          |         |         |         |
| • co-channel                              |          |         | 11      | dB      |
| • 1 MHz                                   |          |         | 0       | dB      |
| • 2 MHz                                   |          |         | -30     | dB      |
| • 3 MHz                                   |          |         | -40     | dB      |
| • image (+4 MHz)                          |          |         | -9      | dB      |
| • image +/- 1 MHz                         |          |         | -20     | dB      |
| Maximum Input Level (PER ≤ 0.1%)          | -20      |         |         | dBm     |
| EDR(8DPSK) Sensitivity (PER ≤ 0.007%)     |          | -88     | -77     | dBm     |

<sup>3</sup> Up to five spurious responses within Bluetooth limits are allowed.

## 14.5 DC/RF Characteristics for Bluetooth Low Energy

**Conditions:** 25 °C, VBAT = 3.6V, VDDIO = 3.3V

**Table 28: DC/RF Characteristics for BLE**

| Items                                               | Contents                 |         |         |      |
|-----------------------------------------------------|--------------------------|---------|---------|------|
| Bluetooth Specification (power class)               | Version 5.1 (LE)         |         |         |      |
| Channel Frequency (spacing)                         | 2402 to 2480 MHz (2 MHz) |         |         |      |
| Number of RF Channel                                | 40                       |         |         |      |
| Transmitter                                         | Minimum                  | Typical | Maximum | Unit |
| Center Frequency                                    | 2402                     |         | 2480    | MHz  |
| Channel Spacing                                     |                          | 2       |         | MHz  |
| Number of RF Channels                               |                          | 40      |         |      |
| Output Power                                        |                          |         | 10      | dBm  |
| Modulation Characteristics                          |                          |         |         |      |
| • $\Delta f_{1\text{avg}}$                          | 225                      |         | 275     | kHz  |
| • $\Delta f_{2\text{max}}$ (at 99.9%)               | 185                      |         |         | kHz  |
| • $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                      |         |         |      |
| Carrier frequency offset and drift                  |                          |         |         |      |
| • Frequency offset                                  |                          |         | 150     | kHz  |
| • Frequency drift                                   |                          |         | 50      | kHz  |
| • Drift rate                                        |                          |         | 20      | kHz  |
| Spurious Emissions                                  |                          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                        |                          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                        |                          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)                     |                          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)                      |                          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)                      |                          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)                     |                          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)                     |                          |         | -30     | dBm  |
| Receiver                                            | Minimum                  | Typical | Maximum | Unit |
| Receiver sensitivity (PER < 30.8%)                  |                          | -95     | -70     | dBm  |
| Maximum input signal level (PER < 30.8%)            | -10                      |         |         | dBm  |
| PER Report Integrity (-30 dBm input)                | 50                       |         | 65.4    | %    |

The land pattern is shown in **Figure 21**.

## 16 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

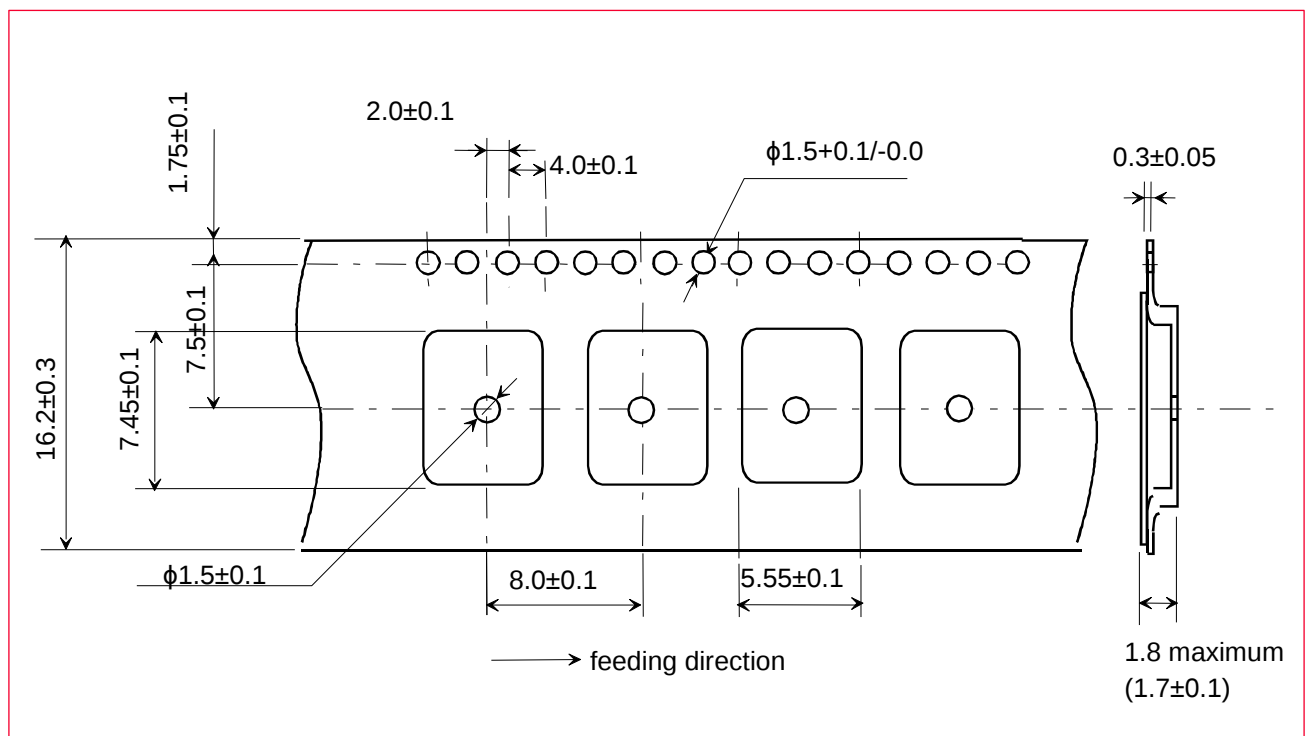
### 16.1 Dimensions of Tape (Plastic Tape)

The dimension of the tape is as follows:

- The corner and ridge radiuses (R) of inside cavity are 0.3 mm maximum.
- Cumulative tolerance of 10 pitches of the sprocket hole is  $\pm 0.2$  mm
- Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

**Figure 22** is a graphical representation of the tape dimension (plastic tape).

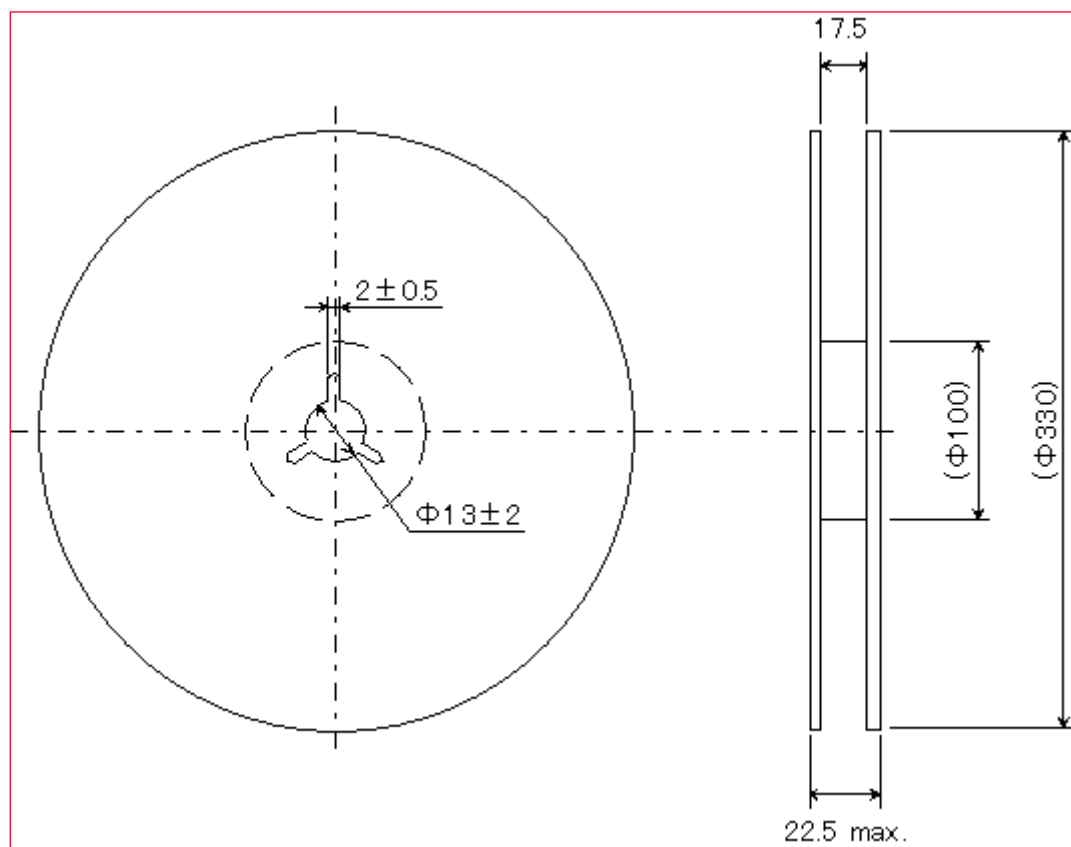
**Figure 22: Dimensions of Tape (Plastic Tape)**



## 16.2 Dimension of Reel

**Figure 23** shows the reel dimensions in millimeters.

**Figure 23: Dimensions of Reel (Unit: mm)**



## 16.3 Taping Diagrams

Figure 24 shows the tapings diagrams.

Figure 24: Taping Diagrams

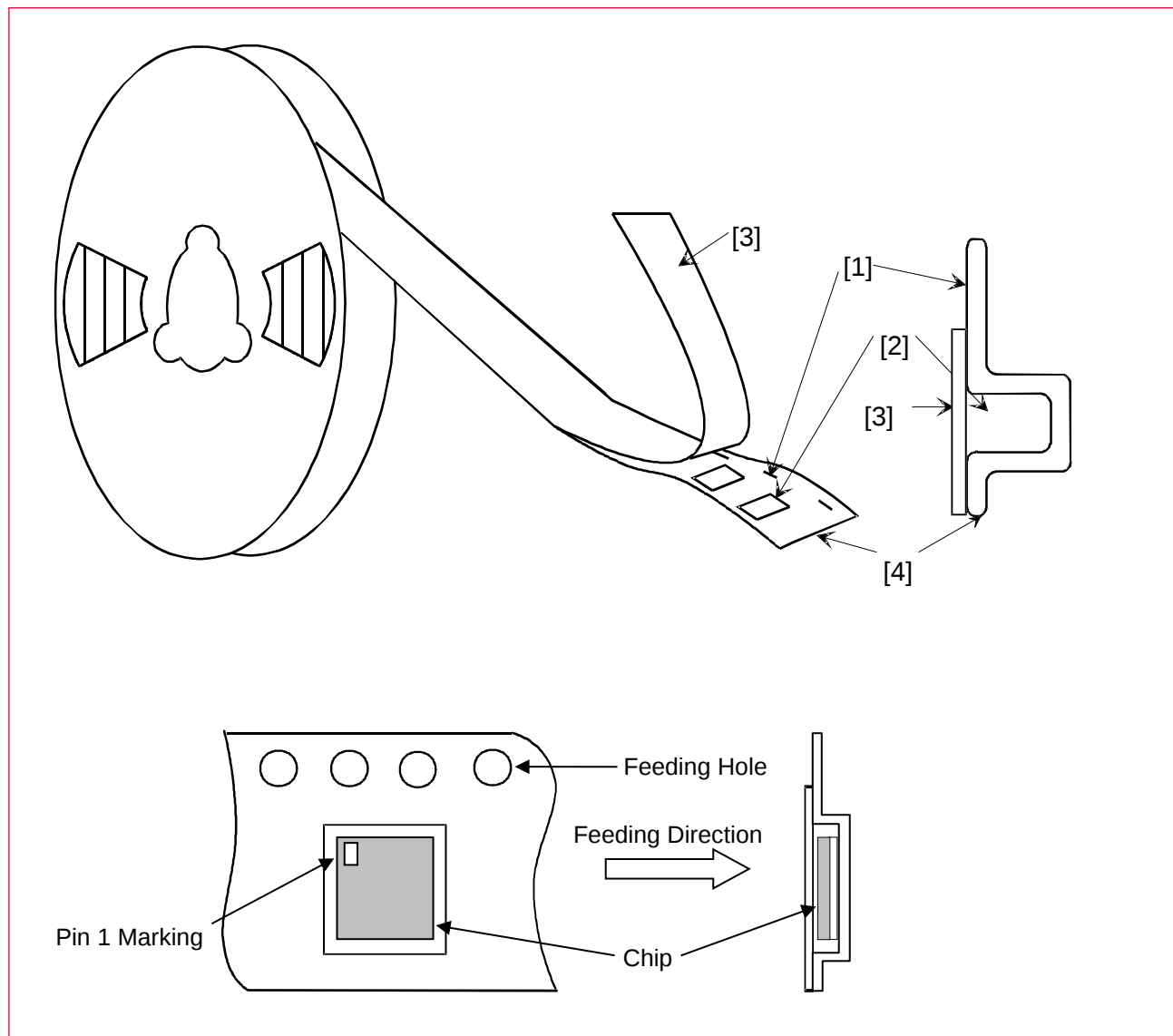


Table 29 shows the taping specifications.

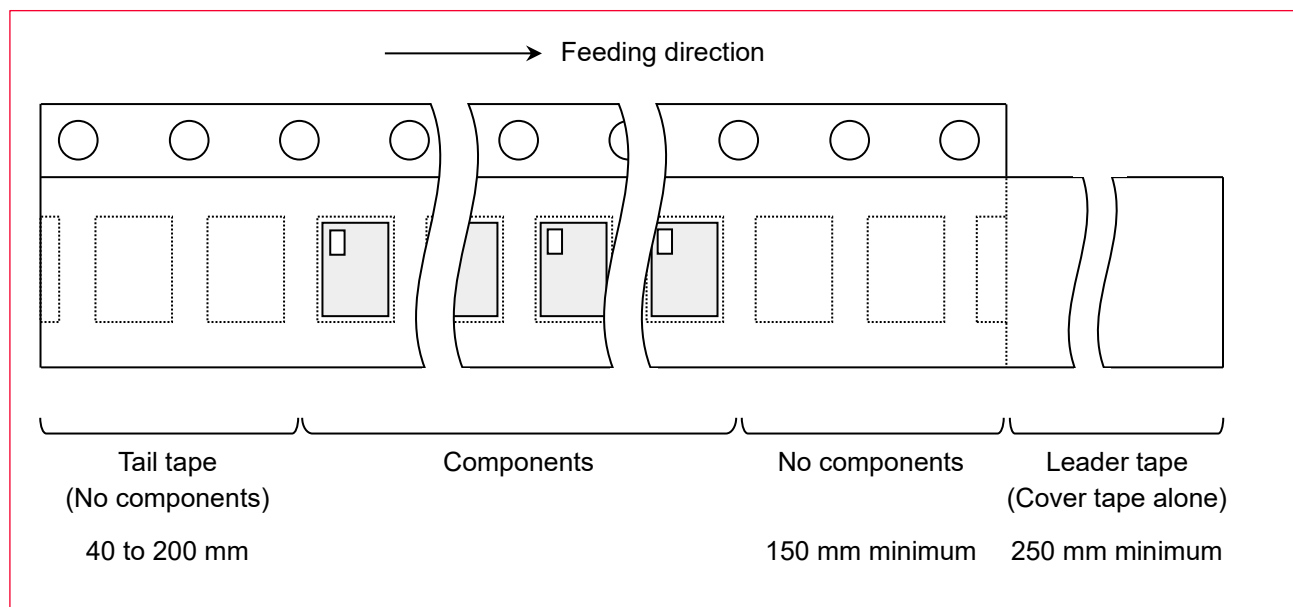
Table 29: Taping Specifications

| Mark | Description                                                                         |
|------|-------------------------------------------------------------------------------------|
| 1    | Feeding Hole. As specified in <a href="#">Dimensions of Tape (Plastic tape)</a> ☐.  |
| 2    | Hole for chip. As specified in <a href="#">Dimensions of Tape (Plastic tape)</a> ☐. |
| 3    | Cover tape. 62 μm in thickness.                                                     |
| 4    | Base tape. As specified in <a href="#">Dimensions of Tape (Plastic tape)</a> ☐.     |

## 16.4 Leader and Tail Tape

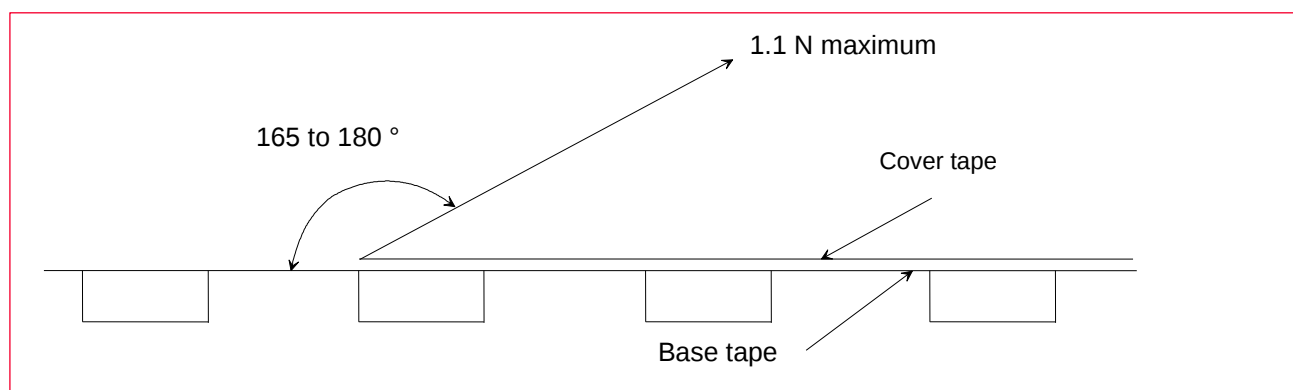
The leader and tail tape are shown in **Figure 25**.

**Figure 25: Leader and Tail Tape**



1. The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
2. The cover tape and base tape are not adhered at no components area for 250 mm minimum.
3. Tear off strength against pulling of cover tape: 5 N minimum.
4. Packaging unit: 1000 pcs. / Reel
5. Material:
  - Base tape: Plastic
  - Reel: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
6. Peeling off force: 1.1 N maximum in the direction of peeling as shown in **Figure 26**.

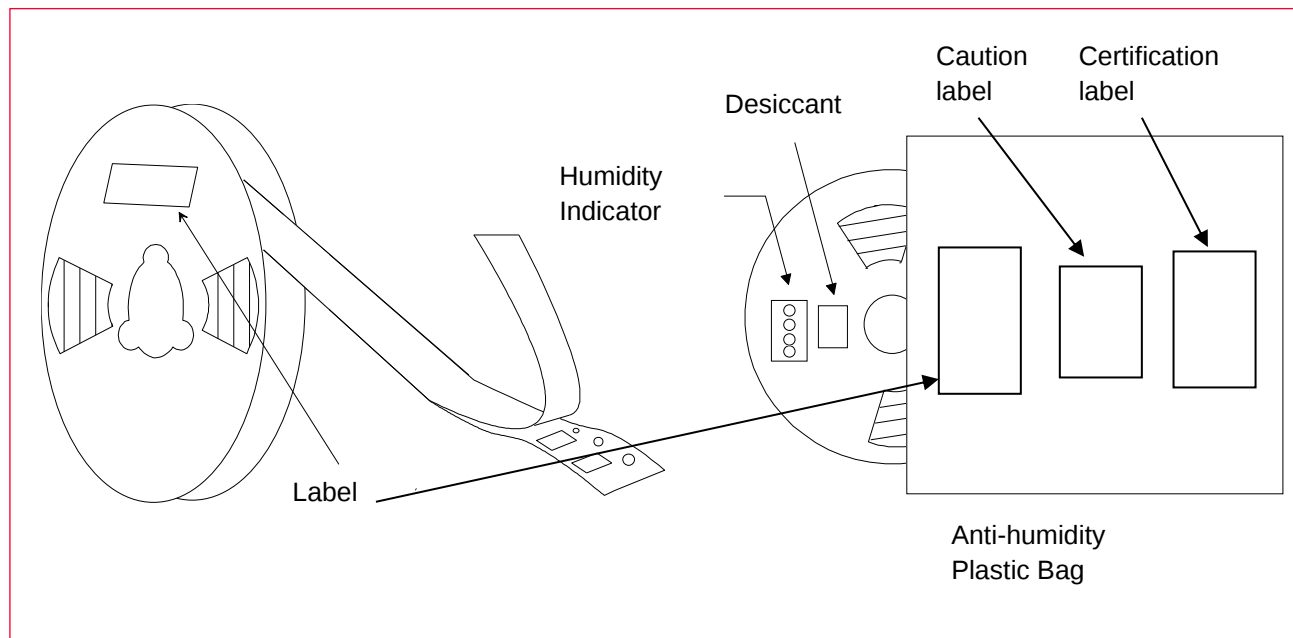
**Figure 26: Peeling Off Force**



## 16.5 Packaging (Humidity Proof Packing)

**Figure 27** shows the humidity proof packaging.

**Figure 27: Humidity Proof Packaging**



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

## 17 Notice

### 17.1 Storage Conditions

- Please use this product within 6 months after receipt.
- The product must be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (packing materials, in particular, may be deformed at the temperature over 40 °C).
- The product left more than 6 months after receipt, the solderability needs to be confirmed the before it is used.
- The product shall be stored in non-corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>2</sub>, NO<sub>x</sub>, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object, and dropping the product, shall not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on JEDEC standard J-STD-020)
  - After the packing opened, the product shall be stored at ≤ 30 °C / ≤ 60 %RH and the product shall be used within 168 hours.
  - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

### 17.2 Handling Conditions

Be careful while handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

### 17.3 Standard PCB Design (Land Pattern and Dimensions)

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions should be as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

## 17.4 Notice for Chip Placer

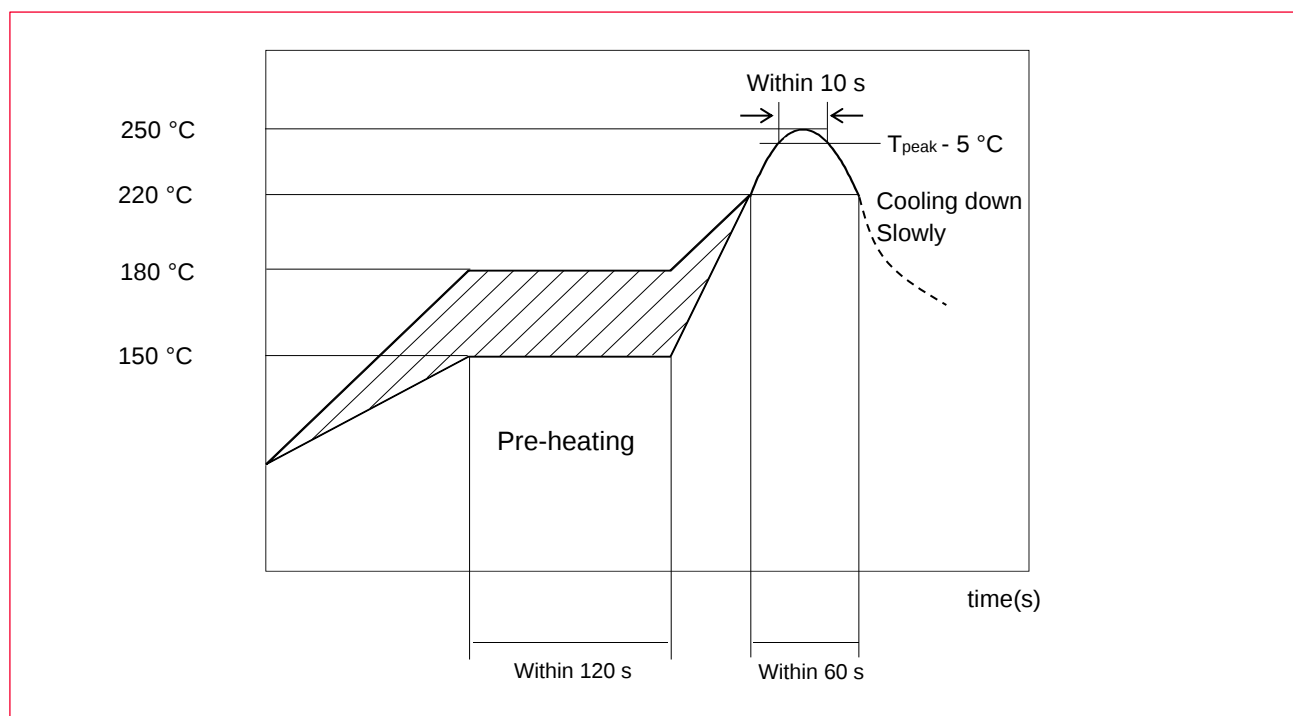
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

## 17.5 Soldering Conditions

The recommendation conditions of soldering are as in **Figure 28**.

Soldering must be carried out by the above-mentioned conditions to prevent products damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use concerning other soldering conditions.

**Figure 28: Reflow Soldering Standard Conditions (Example)**



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt. % or less.

## 17.6 Cleaning

This product is moisture sensitive therefore, cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

## 17.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas ( $\text{Cl}_2$ ,  $\text{NH}_3$ ,  $\text{SO}_x$ ,  $\text{NO}_x$  etc).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.



If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.



Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

## 17.8 Input Power Capacity

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

## 18 Precondition to Use Our Products



PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

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- Traffic signal equipment.

- Burning / explosion control equipment.
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## Revision History

| Revision | Date          | Changed Item                                                                                                   | Comment                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|---------------|----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1        | Dec 10, 2020  |                                                                                                                | First Issue                                                                                                                                                                                                                                                                                                                                                                                     |
| 2<br>(A) | Jun 01, 2021  | 1. Scope<br>4. Certification Information<br>14. Tape and Reel Packing<br>Appendix                              | Update<br>Update<br>Update<br>Added                                                                                                                                                                                                                                                                                                                                                             |
| 3<br>(B) | Jun 14, 2022. | 1. Scope                                                                                                       | Update                                                                                                                                                                                                                                                                                                                                                                                          |
| 4<br>(C) | Dec 10, 2022  | 1. Scope<br><br>3. Ordering Information<br><br>13. Reference Circuit<br>Appendix                               | <ul style="list-style-type: none"> <li>Updated information. Created new section 'Key Features'.</li> <li>Added Embedded Artists' M.2 module information. Renamed section.</li> <li>Moved section to HW app note.</li> <li>Moved Appendix information into Section 16.</li> <li>Added transmit power tables.</li> <li>Moved antenna sections to HW app note.</li> </ul><br>Updated to new format |
| 5<br>(D) | Feb 02, 2023  | 2. Key Features                                                                                                | <ul style="list-style-type: none"> <li>Changes the operating temperature range from -30 ~ 70 °C to -40 ~ 85 °C</li> </ul>                                                                                                                                                                                                                                                                       |
| 6<br>(E) | Jul 07, 2023  | 5. Certification Information                                                                                   | <ul style="list-style-type: none"> <li>Added more Certification ID information.</li> </ul>                                                                                                                                                                                                                                                                                                      |
| 7<br>(F) | Sep 10, 2024  | 2. Key Features<br>5. Certification Information<br>16 Radio Regulatory Certification by Country for LBEE5KL1YN | <ul style="list-style-type: none"> <li>Add Fit value</li> <li>Remove certification information</li> </ul>                                                                                                                                                                                                                                                                                       |
| 8        | Mar 31, 2025  | ALL<br>5. Certification Information<br>13 DC/RF Characteristics                                                | <ul style="list-style-type: none"> <li>Modify BT ver</li> <li>Add certification information</li> <li>Format change</li> <li>Updated (Base IC datasheet revision: F)</li> </ul>                                                                                                                                                                                                                  |



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