60mΩ Adjustable Current Limited Power Switches

General Description

The ET2016 are current limited P-channel MOSFET power switch designed for high-side load switching applications. This switch operates with inputs ranging from 2.5V to 5.5V, making it ideal for both 3.3V and 5V systems. An integrated current-limiting circuit protects the input supply against large currents which may cause the supply to fall out of regulation. The ET2016 is also protected from thermal overload which limits power dissipation and junction temperatures. It can be used to control loads that require from 0.4A to 2.5A. Current limit threshold is programmed with a resistor from SET to ground. The quiescent supply current in active mode is only 25μA. In shutdown mode, the supply current decreases to less than 1μA.

The ET2016 is available in Pb-free packages and is specified over the -40°C to +85°C ambient temperature range.

Features

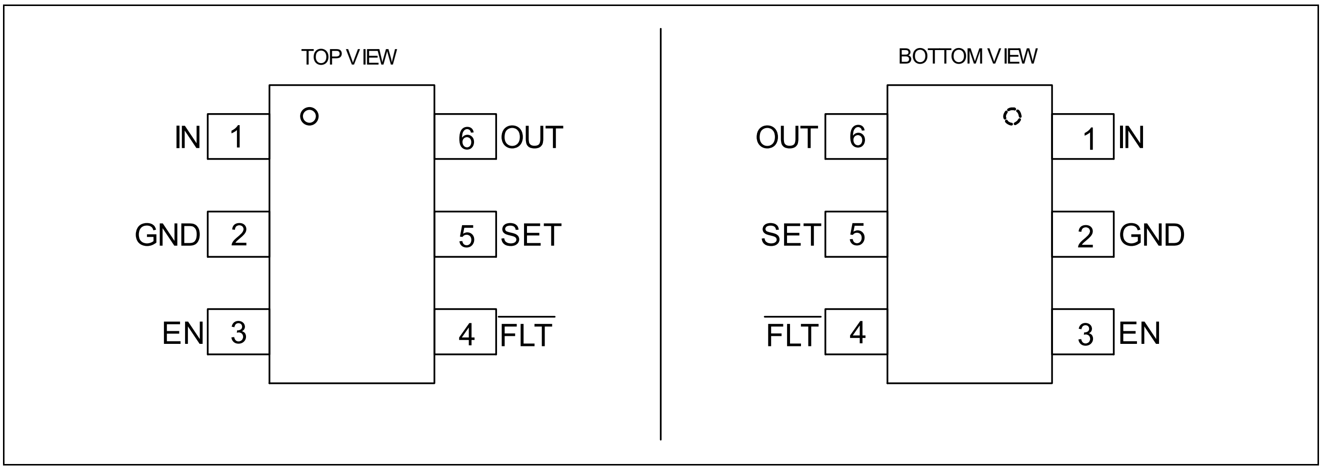
- Input Voltage Range: 2.5V to 5.5V
- Programmable Current Limit
- Reverse Current Blocking
- Short-Circuit Response: 2us
- Very Low Quiescent Current: 25μA (Typ)
- 1μA Max Shutdown Supply Current
- Under-Voltage Lockout
- Thermal Shutdown
- 4kV ESD Rating
- Part No. and Package

Part No.	Package
ET2016	SOT23-6

Application

- Laptop/Desktop Computers and NootBooks
- LCD TVs and Monitors
- Set-Top-Boxes
- Printers
- Portable Media Players and MIDs
- USB Keyboards
- USB Hard Disk Drives
- USB Memory Drives
- USB Hubs

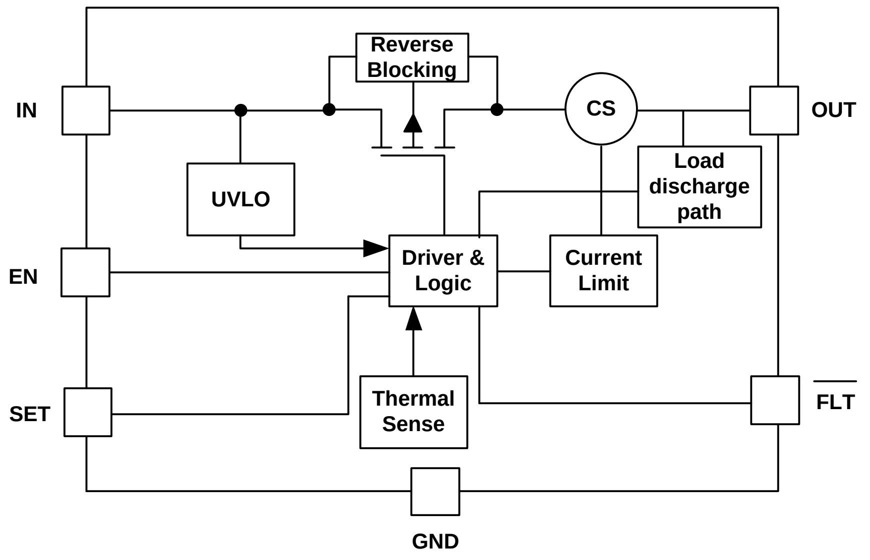
Pin Configuration



Pin Function

Pin	Name	Description
1	IN	Power supply input. Must be closely decoupled to GND pins with a 1μF or greater ceramic capacitor.
2	GND	Ground Pin.
3	EN	Enable input.
4	$\overline{\text{FLT}}$	Over-current, reverse-voltage and over-temperature fault reporting signal output, active low with 6ms blanking time for over-current.
5	SET	Current limit programming pin.
6	OUT	Power output.

Block Diagram



Functional Description

ET2016 is an integrated power switch with a low Rdson P-channel MOSFET, internal gate rive circuit, programmable current limiting. When the ET2016 turns on, it can deliver up to 2.5A continuous current to load. When the device is active, if there is no load, the device only consumes 25uA supply current, which makes the device suitable for battery powered applications.

Power Supply Considerations

A 0.01µF to 0.1µF ceramic bypass capacitor between IN and GND, close to the device, is recommended.

Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input and minimize the input voltage droops. Additionally, bypassing the output with a 0.01µF to 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Power Dissipation and Junction Temperature

The low on-resistance on the P-channel MOSFET allows the small surface-mount packages to pass large currents. It is good design practice to check power dissipation and junction temperature for each application. Begin by determining the $R_{DS(ON)}$ of the P-channel MOSFET relative to the input voltage and operating temperature. Using the highest operating ambient temperature of interest and $R_{DS(ON)}$, the power dissipation per switch can be calculated by:

$$P_D = R_{DS(ON)} \times I_{OUT}^{\ 2} \qquad (1)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \qquad (2)$$

Where:

T_A= Ambient temperature

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

Compare the calculated junction temperature with the maximum junction temperature which is 150°C. If they are within degrees, either the maximum load current needs to be reduced or another package option will be required.

Soft Start for Hot Plug-In Application

In order to eliminate the upstream voltage drop caused by the large inrush current during hot-plug events, the "soft-start" feature effectively isolates the power source from extremely large capacitive loads, satisfying the USB voltage drop requirements.

Over Current

A sense FET is employed to check for over-current conditions. When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. ET2016 will limit the current until the overload condition is removed or the device begins to thermal cycle.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied. The ET2016 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react .

After the current-limit circuit reached the over-current trip threshold, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The ET2016 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{FLT}}$ Output

The FAULT Flag ($\overline{\text{FLT}}$) is provided to alert the system if a ET2016 load is not receiving sufficient voltage to operate properly. If current limiting circuit is active for more than approximately 6ms, the FAULT Flag is pulled to ground through an approximately 100Ω resistor. The filtering of voltage or current transients of less than 6ms prevents capacitive loads connected to the ET2016 output from activating the FAULT Flag when they are initially attached. However, if the device is entering over-temperature conditions, the $\overline{\text{FLT}}$ will be pulled low without delay or deglitch. Pull-up resistance of 1kΩ to 100kΩ on $\overline{\text{FLT}}$ pin is recommended. Since $\overline{\text{FLT}}$ is an open drain terminal, it may be pulled up to any unrelated voltage less than the maximum operating voltage of 5.5V, allowing for level shifting between circuits.

Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The ET2016 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an over-current or short-circuit condition, the junction temperature rises due to excessive power dissipation.

Once the die temperature rises to approximately 155℃ due to over-current conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 25℃, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

Current Limiting Setting

Current limit is programmable to protect the power source from over current and short circuit conditions. Connect a resistor R_{SET} from SET pin to GND to program the current limit:

$$I_{LIM}(A) = 6800/R_{SET}\ (\Omega) \qquad (3)$$

The minimum current limit is 0.4A. Current limit beyond 2.5A is not recommended. The formula is for reference only, please refer to the actual test flow limiting curve.

Table1. Common R_{SET} Resistor Selections

Ideal R_{SET} (Ω)	Ideal I_{LIMIT} (mA)	Closest R_{SET} (Ω)	Actual I_{LIMIT} (mA)
16K	425	16.00K	440
15K	453	15.04K	471
13K	523	13.06K	546
12K	567	12.03K	596
11K	618	11.01K	655
10K	680	10.05K	723
8.2K	829	8.21K	888
7.5K	907	7.40K	990
6.8K	1000	6.78K	1088
6.2K	1097	6.19K	1193
5.6K	1214	5.61K	1318
5.1K	1333	5.01K	1477
4.7K	1447	4.75K	1558
4.3K	1581	4.33K	1708
3.9K	1744	3.91K	1888

PCB Layout Guide

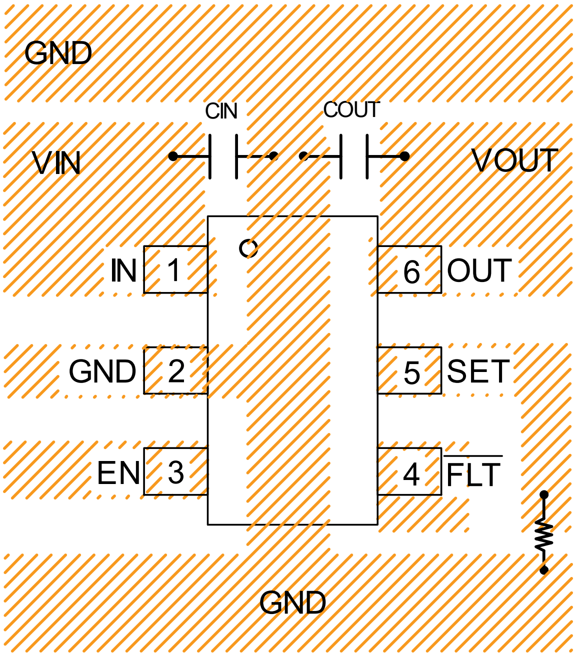
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1) Keep the path of current short and minimize the loop area formed by Input and output capacitor.

2) Output capacitor and IC must be on the same side, The distance of OUT pin and output capacitor <3mm is recommended.

3) Bypass ceramic capacitors are suggested to be put close to the IN Pin.

4) Connect IN, OUT, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



PCB Layout Reference

Absolute Maximum Ratings

Parameter	Rating	Unit
IN, EN, $\overline{FLT}$ Voltage	-0.3 to 6.0	V
OUT Voltage	-0.3 to V_{IN} + 0.3	V
OUT Current	Adjustable Current	A
Power Dissipation (T_A = 25°C)	500	mW
Package Thermal Resistance (θ_{JA})	250	°C/W
Operating Junction Temperature (T_J)	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

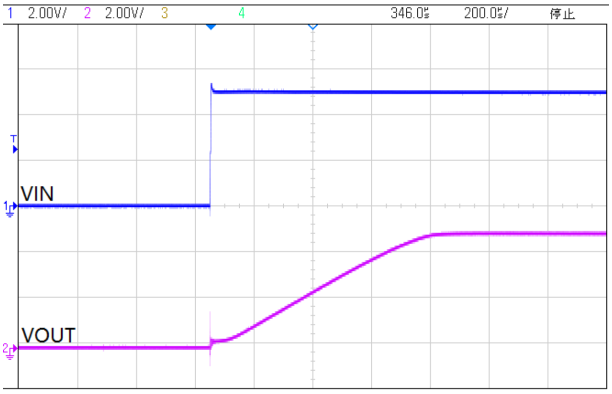
Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Electrical Characteristics

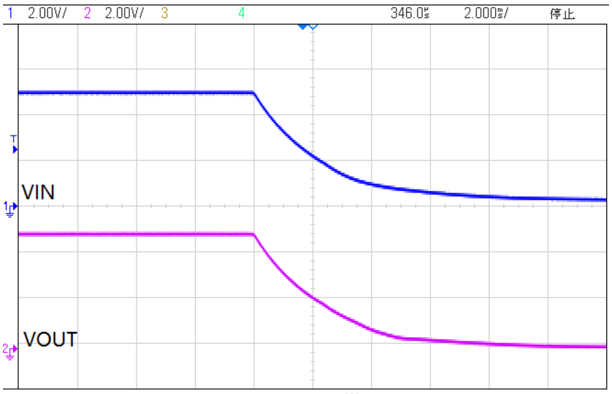
(V_{IN} = +5.0V, T_A = -40°C to 85°C, typical values at T_A=25°C, unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.5		5.5	V
V_{UVLO}	Input UVLO Voltage		1.4	1.8	2.3	V
$V_{UVLOHys}$	UVLO Hysteresis			0.25		V
I_{SHDN}	Input Shutdown Quiescent Current	Disabled,OUT floating or shorted to ground		0.1	1	uA
I_Q	Input Quiescent Current	Enabled, V_{EN}=V_{IN}, I_{OUT}= 0A	10	25	60	uA
$R_{DS(ON)}$	Switch on-resistance	V_{IN}=5V, I_{OUT}=0.6A		60	120	mΩ
I_{LMT}	Current Limit	V_{IN}=5V, V_{OUT}=4.5V, R_{SET}=6.8K	0.75	1	1.25	A
		V_{IN}=5V, V_{OUT}=4.5V, R_{SET}=5.6K	0.91	1.21	1.51	A
		Min Current Limit		0.4		A
V_{IL}	EN Input Logic Low Voltage				0.8	V
V_{IH}	EN Input Logic High Voltage		2.0			V
I_{SINK}	EN Input leakage	V_{EN} = 5V		0.01	1	uA
T_{ON}	Output Turn-on Delay Time	V_{IN} =5V, C_L=1uF, R_L=100Ω	0.2	0.6	1.0	ms
T_R	Output Turn-on Rise Time	V_{IN} =5V, C_L=1uF, R_L=100Ω	0.2	0.5	0.8	ms
T_{OFF}	Output Turn-off Delay Time	V_{IN} =5V, C_L=1uF, R_L=100Ω	0.1	0.3	0.5	ms
T_F	Output Turn-off Fall Time	V_{IN} =5V, C_L=1uF, R_L=100Ω	50	120	200	us
R_{DIS}	Output Discharge FET R_{DSON}	V_{IN} = 5V, V_{EN} =0V, V_{OUT}=5V	200	400	800	Ω
T_{FLT_BLANK}	FLT Blanking Time		2	6	10	ms
V_{FLT_Lo}	FLT Logic Low Voltage	$I_{FLT(SINK)}$ =1mA			0.2	V
I_{FLT}	FLT Leakage Current	V_{FLT} = 5V, Enabled, No Fault Conditions		0.1	1	uA
I_{REV}	Reverse leakage current	V_{OUT} = 5V , V_{IN} = 0V measure I_{VOUT}	0.1	1	3	uA
T_{SHDN}	Thermal shutdown threshold	V_{IN} = 5V	140	155	165	°C
T_{HYS}	Thermal shutdown hysteresis	V_{IN} = 5V		25		°C

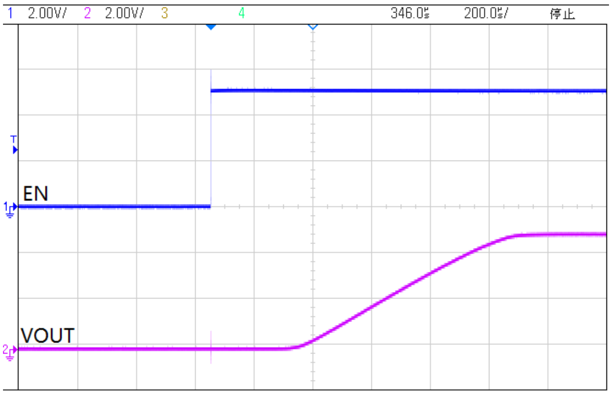
Typical Performance Characteristics



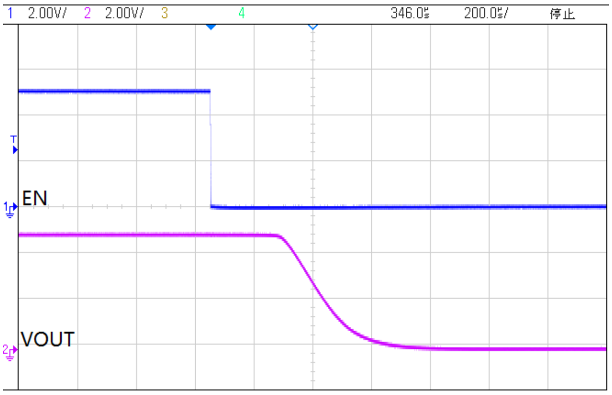
UVOL at Rising



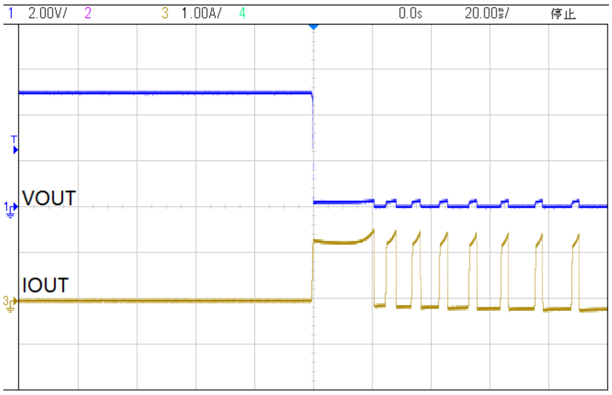
UVOL at Falling



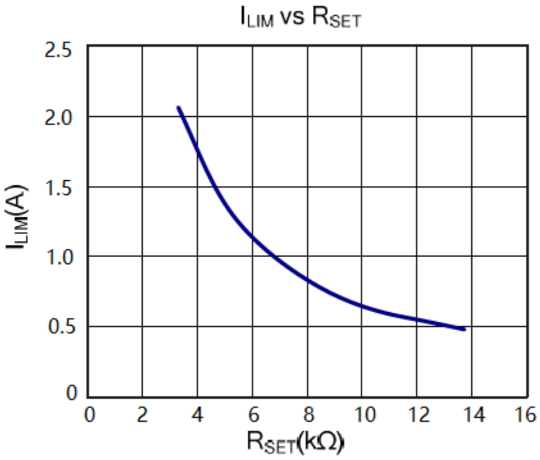
Turn on delay



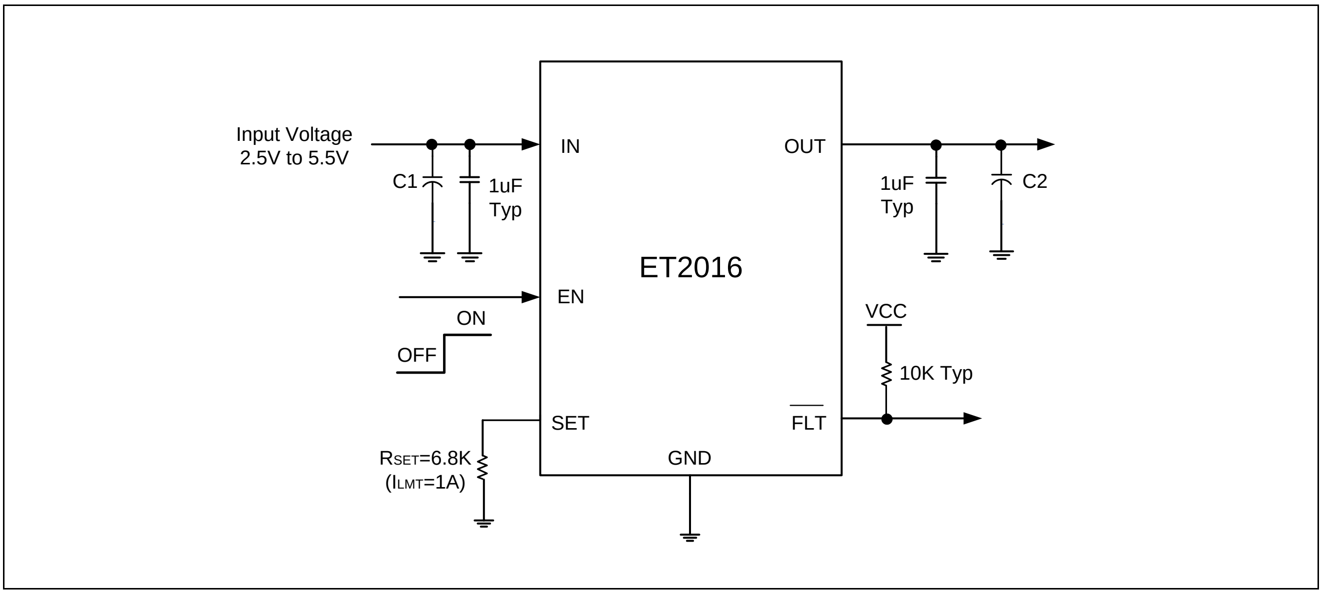
Turn off delay



Short circuit response and Thermal shut down



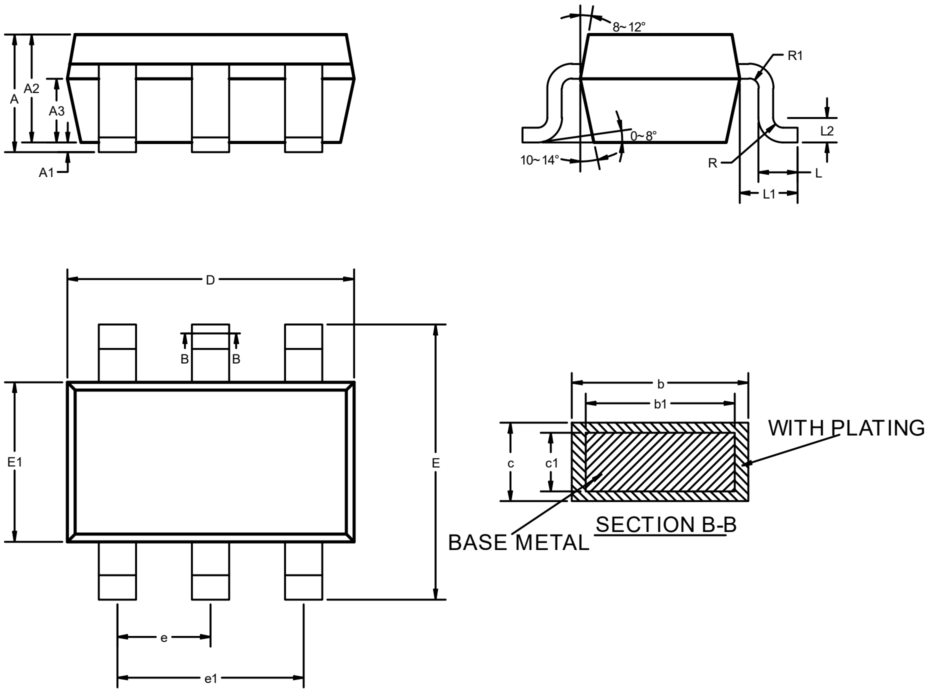
Application Circuits



Note*: Tantalum or Aluminum Electrolytic capacitors (C1 and C2) may be required for USB applications.

Package Dimension

SOT23-6



Dimensions Table (Units:mm)

Symbol	Min	Typ	Max
A	—	—	1.250
A1	0	—	0.150
A2	0.750	—	1.200
A3	0.350	0.650	0.700
b	0.360	—	0.460
b1	0.350	0.380	0.430
c	0.130	—	0.200
c1	0.120	0.150	0.160
D	2.820	2.926	3.026
E	2.600	2.800	3.000
E1	1.500	1.626	1.726
e	0.900	0.950	1.000
e1	1.800	1.900	2.000
L	0.300	0.400	0.500
L1	0.590 REF		
L2	0.250 BSC		
R	0.050	—	0.200
R1	0.050	—	0.200

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-04-22	Original version	Liu Yi Guo	Liu Yi Guo	Zhujl
1.1	2017-03-14	Updated $R_{DS(ON)}$	Shibo	Shibo	Zhujl
1.2	2017-08-03	Updated Ilim. vs. Rset	Liu Yi Guo	Liu Yi Guo	Zhujl
1.3	2018-11-19	Add Rset selection	Liu Yi Guo	Liu Yi Guo	Zhujl
1.4	2020-04-26	Document check and formalize	Shibo	Liu Yi Guo	Zhujl
1.5	2022-09-23	Update format	Wu He Song	Wu Hesong	Zhujl
1.6	2023-02-24	Update R_{SET}	Wu He Song	Wu Hesong	Zhujl
1.7	2024-07-22	Update Soft Start	Zou Chao Min	Wu Hesong	Zhujl