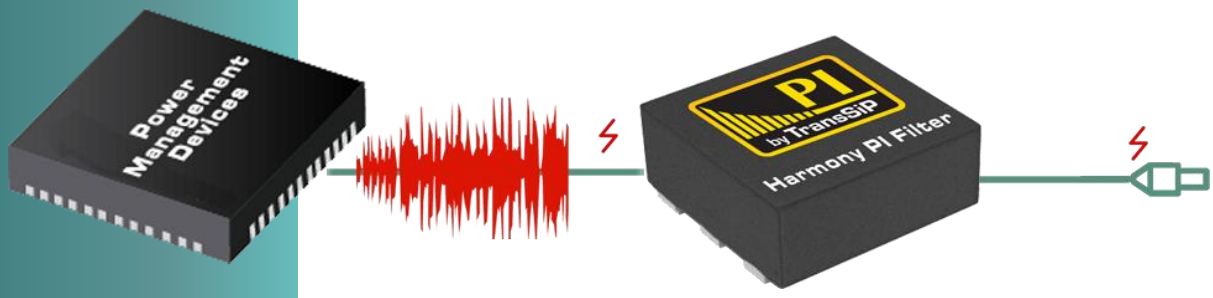
Harmony PI Filter™

Enables Noise Free by SNJ Conditioning



Applications:

- Power Source
- Wirelss
- Telecommunications
- Computing
- Signal Processing
- Noise-Sensitive Devices

MAKING IT POSSIBLE ™

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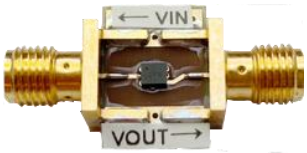
Revision History

3/2025 Revision 7.0

Design Resources

Evaluation Kits

- Harmony Evaluation Board with SMA



Reference Materials

- Harmony App Note: For more information, please contact us at contactus@transsip.com to request the application note “EVB Read Me.”

Where to buy

DigiKey MFG PN: TSNJ-5A6L26

Credentials

ULP UNIVERSITY LAB PARTNERS

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2021 WINNER TransSiP TECHNOLOGY

u-blox + PI by TransSiP

Check Out Switching Noise Jitter (SNJ)

WIKIPEDIA The Free Encyclopedia

KEYSIGHT TECHNOLOGIES

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Contents

1.0 Introduction

The **Harmony PI Filter** (TSNJ-5A6L26) is the world's first power integrity (PI) filter designed to enable Noise-Free circuit designs, leaving the noise floor as the only limit for your noise-sensitive applications. Our patented Switching Noise Jitter (SNJ) conditioning technology provides robust noise elimination from DC up to 20 GHz in both time and frequency domains. The Harmony PI Filter can free up 90% of valuable PCB board space by eliminating 80% of passive components on a power distribution network (PDN). This allows for the addition of more high-value chips within the same PCB real estate, achieving exceptional levels of signal clarity, accuracy, and reliability. Despite its powerful capabilities, the Harmony PI Filter comes in a tiny package of just 2.2 mm x 2.6 mm x 0.9 mm and does not consume power.

Harmony can be applied in both the power chain and signal chain. When used in the power chain, its time-domain feature suppresses SNJ and chaotic noise at the output of a switching mode power supply. This results in smaller high-speed current loops, eliminating EMI, stabilizing switching power supplies, and increasing power conversion efficiency. Harmony also helps isolate noise generated from other parts of a circuit, preventing it from affecting the entire system, including simultaneous switching noise (SSN) and ground bounce. Additionally, Harmony eliminates problematic anti-resonance peaks, impedance violations, LC tank oscillations, voltage overshoot, and incorrect operations commonly caused by ferrite beads, capacitor banks, and EMI filters.

For small signals produced by sensors below 1Hz to a few hundred Hz, such as geophones, applying Harmony to the signal chain provides a native 3dB cutoff at 700 Hz and eliminates all unwanted signals and noise beyond that. This helps simplify system architecture and reduce costs by eliminating the need for power-hungry and complex digital filtering, such as delta-sigma A/D converters.

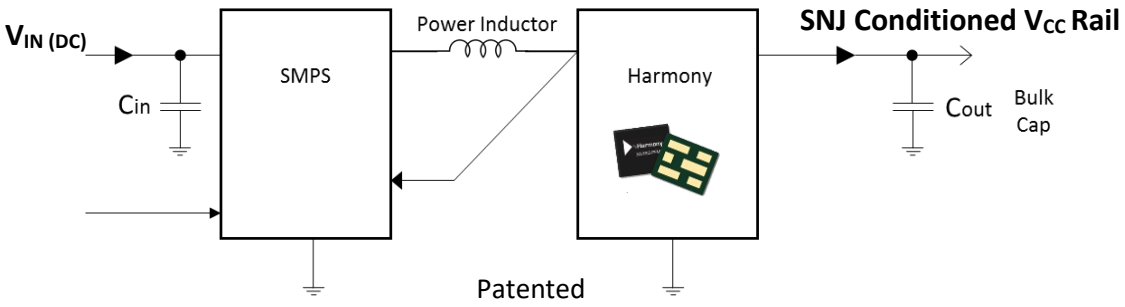
1.1 Applications

- **Power Source:** PMIC, SMPS, LDO, Energy Harvesting
- **RF, Microwave, and Optical Components**
- **Computing**
- **Signal Processing:** A/D, D/A, Audio, Video
- **Sensors:** LEDs, Photodetectors, Geophones, MEMS, biomedical

Key Features:

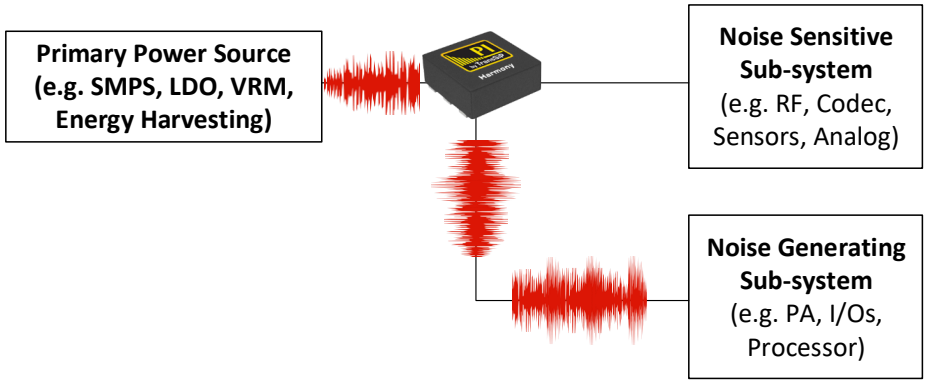
- Ampacity: 5A at 25°C
- Voltage Rating: 6V DC
- Time Domain SNJ Conditioning
- Native 3dB Cutoff: 700 Hz
- Noise Suppression from DC up to 20 GHz
- DC Resistance: 39 mΩ
- Operating Temperature: -55°C to +85°C
- RoHS
- 2.2 x 2.6 x 0.9 [mm]

1.2 Circuit Topology in Power Chain (Simplified Schematic)



1.3 Application Examples

Noise Free Power Rails and Insolation

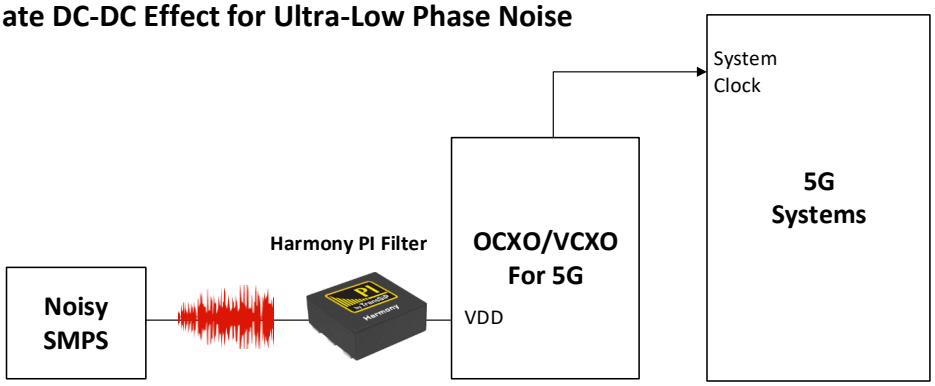


Check out the videos for Noise Free Switcher:

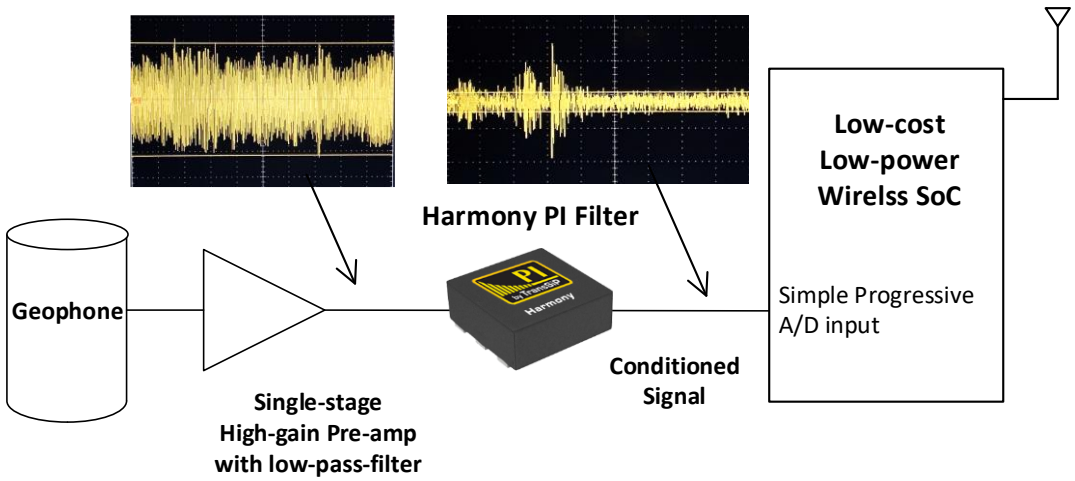
TransSiP PI Series - Part 2: ADI Silent Switcher LT8622S Becomes Noise-Free

TransSiP PI Series - Infiniium MXR B-Series, Part 1 of ADI Silent Switcher LT8622S

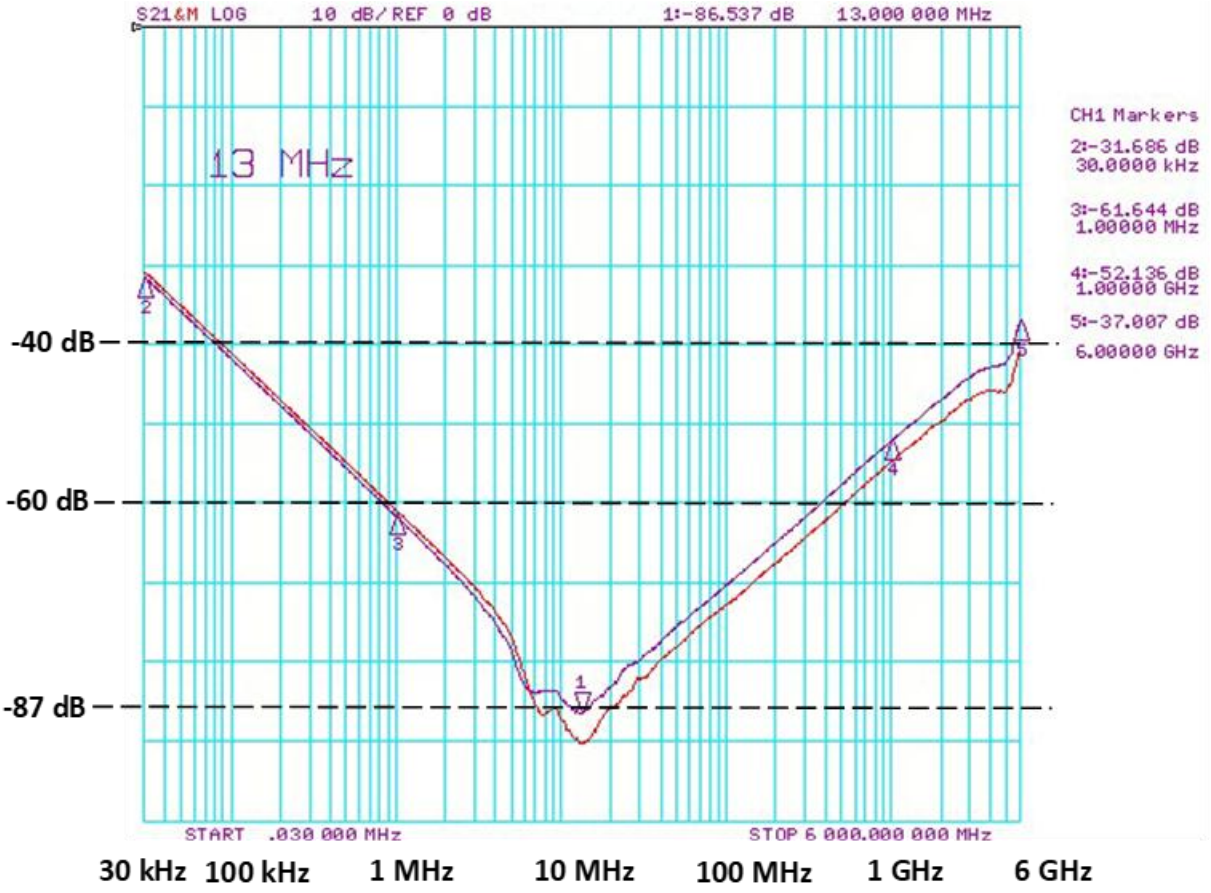
Eliminate DC-DC Effect for Ultra-Low Phase Noise



Simplify Signal Chain and Significantly Lower Energy Consumption



1.4 Insertion Loss Characteristics (Native, without Bulk Capacitor)

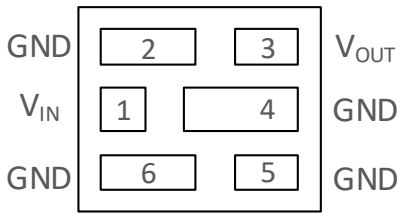


2.0 MFG PN: TSNJ-5A6L26

Harmony PN TSNJ-①②③④	Characteristics	SYMBOL	DESCRIPTION
①	Rated Current	5	Ampacity = 5A at 25°C [1]
②	Reserved	A	Current Identifier
③	Rated Voltage	6	Rated voltage = 6 V DC
④	Package	L26	LGA-2226 / 2.2 mm x 2.6mm x 0.9 mm

*Note: The maximum ampacity is rated at 25°C with adequate ventilation. Derating is required to prevent thermal damage to the internal structures.

2.1 Pin Assignment and Package Type

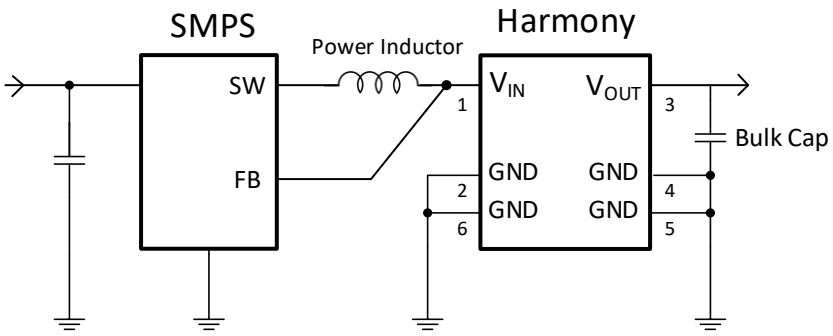


LGA-2226
(BOTTOM VIEW)

Harmony LGA-2226	Pin Name	Function
1	V_{IN}	Voltage / Signal Input
2	GND	Ground
3	V_{OUT}	Voltage / Signal Output
4	GND	Ground
5	GND	Ground
6	GND	Ground

3.0 Application Information

3.1 Circuit Topology for SMPS



Note [1]: For the best result of SNJ elimination, place the Harmony in close proximity to the power inductor and feedback (FB) node with traces as wide and as short as possible. Pay attention to the Grounding Guidelines in section 3.2.

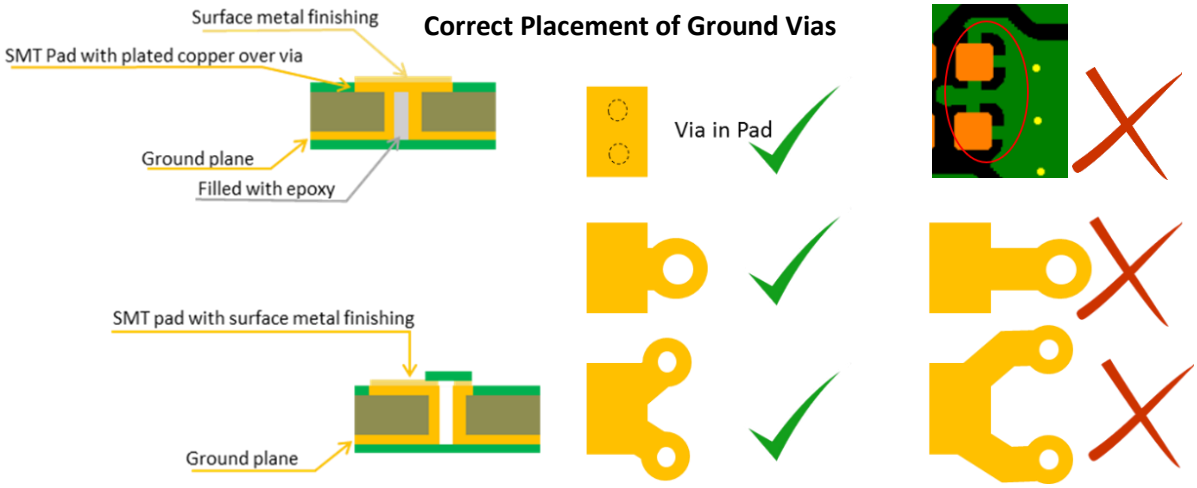
Note [2]: To enhance the noise suppression bandwidth (S21) of Harmony, connect bulk capacitors to its output. This will significantly deepen and widen the S21 compared to its native performance, as detailed in section 1.4. Bulk capacitors typically have large capacitance or consist of a bank of large capacitors. Small value capacitors are not necessary. For more information, please contact us at contactus@transsip.com to request the application note "EVB Read Me."

Glossary: SMPS stands for Switching Mode Power Supply

3.2 Harmony Grounding and SMPS Layout Guidelines

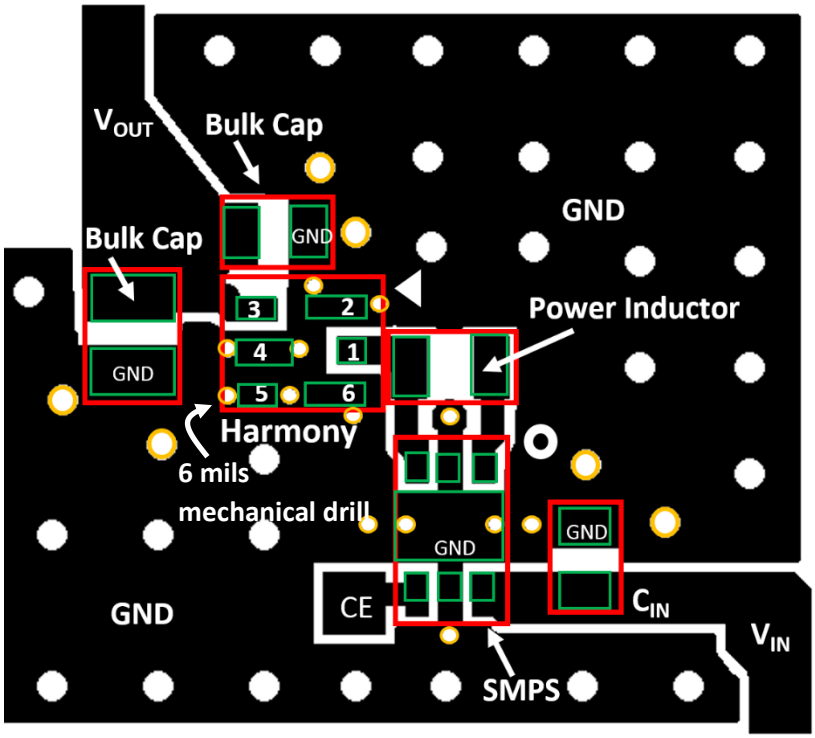
The layout of grouding vias is of utmost importance. Key notes on layout are listed as follows:

1. **Ground Plane** – Use a ground plane in the inner layer immediately below the Harmony. Connect each GND terminals directly to the ground plane using ground vias. Mechanical drill holes of 0.2 mm (8 mil) are adequate and must be placed immediately adjacent to the ground terminals, as shown in the pictures below. At least one ground via should be used at each end of the GND terminals. Do not use long trace and thermal reliefs to connect the GND terminals. The ground plane should be directly connected to a battery or power source using the widest and shortest connection possible.
2. **Via-in-Pad** – For a compact design, using via-in-pad to connect all the GND terminals of Harmony is highly recommended.
3. **Laser Drill** – Since the typical diameter of a laser drill via is 50 µm or less, use multiple laser vias instead of placing one in each of the GND terminals of Harmony.
4. **Signal and Power Traces** – Do not run signal and power traces under or in the inner layer below the Harmony without a ground plane inserted in between.
5. **SMPS** – When using the Harmony with an SMPS, place the Harmony (Pin 1 - Vin) in close proximity to the power inductor and feedback node, with traces as wide and as short as possible. Do not route traces under the power inductor.
6. **Stitching Vias** – Ground planes between different layers should be interconnected with as many ground vias in close proximity as possible. Avoid using a single via or vias with large separation to connect different layers of ground planes.



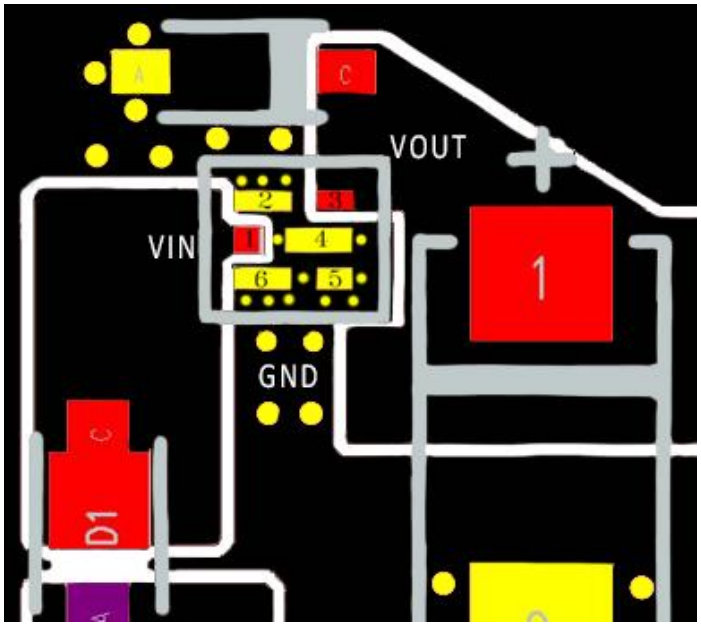
Example Layout: Harmony for SMPS

(TOP LAYER PLACEMENT)



Example Layout: Harmony for Power Rail Isolation

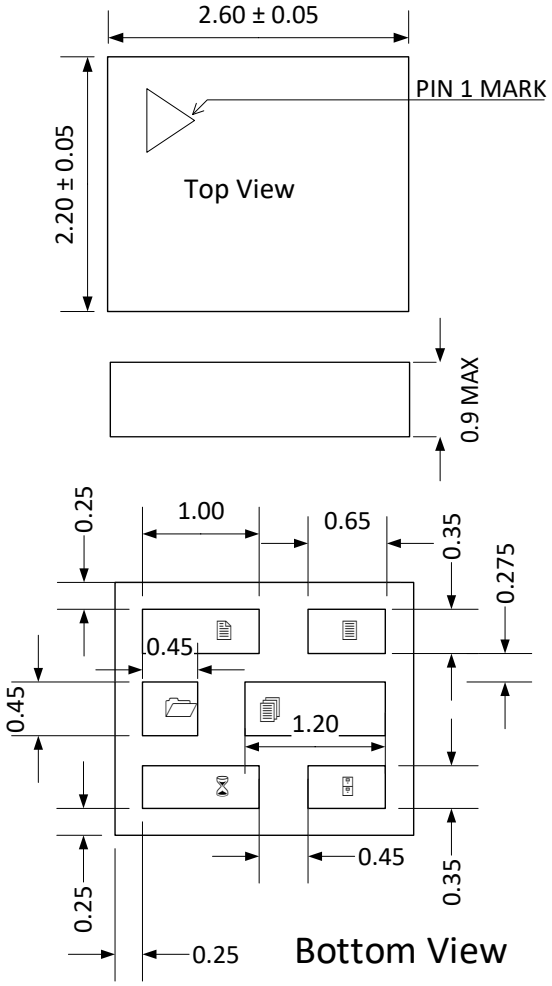
(BOTTOM LAYER PLACEMENT)



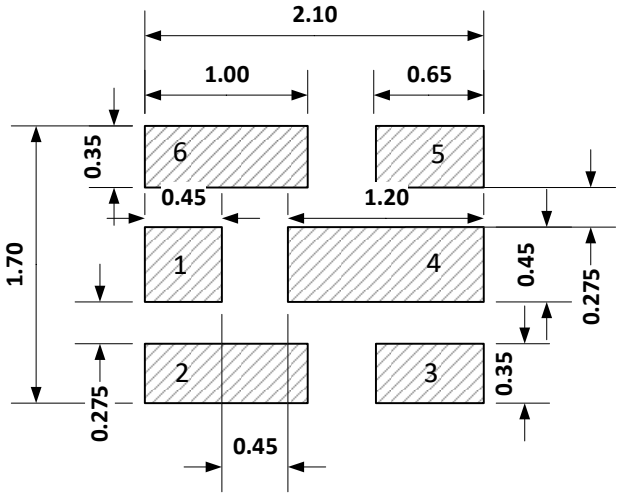
4.0 Package and PCB Land Pattern Information

Unit: mm

Harmony LGA-2226



LGA-2226 PCB Land Pattern (Top View)



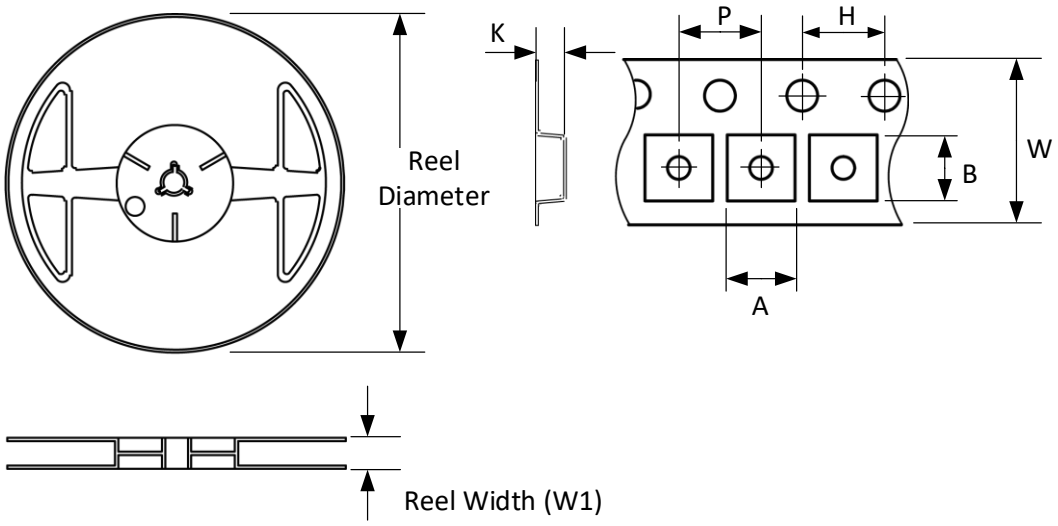
Marking

4-Digit Date Code Syntax: Week No. Year

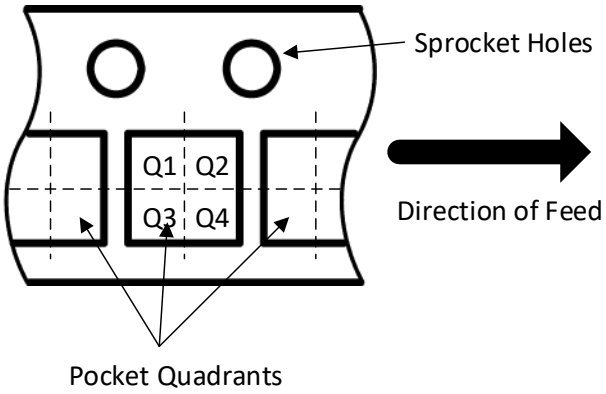
5.0 Tape and Reel Information

Reel Dimensions

Tape Dimensions



Quadrant Assignments for Pin 1 Orientation in Tape



Device	Package Type	Pins	Pin 1 Quadrant	Reel Diameter	Reel Width W1	A	B	K	P	H	W	Qty/ Reel
Harmony	LGA-2226	6	Q2	180	12.0	2.4	2.8	1.1	4.0	4.0	8.0	3000

6.0 Handling and Soldering

6.1 Moisture Sensitivity Level 2a (MSL 2a) Handling at PCB Assembly

The Harmony PI Filter is rated as MSL 2a and needs to be handled with proper MSL 2a guidelines to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation.

MSL 2a devices are dry-packed before shipment from TransSiP. The packing uses a Moisture Barrier Bag (MBB). A Humidity Indicator Card (HIC) and drying desiccant are included inside the MBB. Shelf life of devices in a sealed bag is 12 months at <40°C and <90% room humidity (RH).

Upon opening of MBB, the HIC should be checked immediately; devices require baking before board mounting if the HIC is >10% when read at 23°C ±5°C.

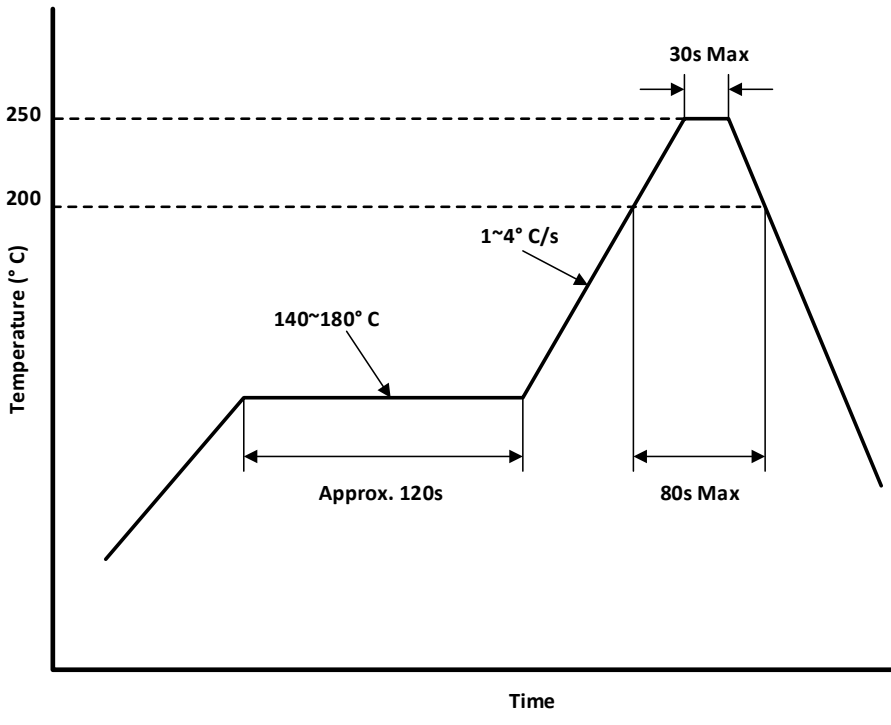
After MBB is opened, devices should go through reflow for board assembly within 4 weeks at factory conditions of <30°C/60% RH, or stored at <10% RH. If both of these conditions are not met, baking is required before board mounting.

If baking is required, devices should be baked for a minimum of 9 days at 40°C, ≤5% RH, or 60 hours at *60°C +5/-0°C, ≤ 5% RH.

*Note: DO NOT bake parts over 65°C while contained in tape/reels as shipped from TransSiP. For baking over 65°C, remove individual parts and place onto oven tray. If shorter bake times are desired, refer to IPC/JEDEC J-STD-033 for baking procedure.

6.2 Reflow

The Harmoy is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, “Classification Reflow Profiles”.



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