4Gb / 8Gb / 16Gb 4-bit ECC, x8 I/O, 1.8V Vcc

NAND Flash Memory Datasheet

4Gbit x8, 1.8V, 4K page, 256byte Spare: JS27HP4G08SF-SU

8Gbit x8, 1.8V, 4K page, 256byte Spare: JS27HP8G08SF-SU

16Gbit x8, 1.8V, 4K page, 256byte Spare: JS27HPAG08SF-SU

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	May. 2023	

Product Information

Device Name	Voltage		Density	NAND Org.		Cell Type		Option		Package Type	
JS27HP4G08SFDA-45	P	1.8V	4G	08	x8	S	SLC	F	4K Page/ 256B spare	DA	63-Ball FBGA (9.0 x 11.0)
JS27HP8G08SFDA-45	P	1.8V	8G	08	x8	S	SLC	F	4K Page/ 256B spare	DA	63-Ball FBGA (9.0 x 11.0)
JS27HPAG08SFDA-45	P	1.8V	16G	08	x8	S	SLC	F	4K Page/ 256B spare	DA	63-Ball FBGA (9.0 x 11.0)

Features Summary

- **Single-level Cell(SLC) Technology**
  - Cost effective solutions for mass storage applications
- **Open NAND Flash Interface (ONFI) 1.0 compliant**
- **POWER SUPPLY VOLTAGE**
  - VCC/VCCQ = 1.7V ~ 1.95V
- **MEMORY CELL ARRAY (with SPARE)**
  - Page size : (4K+256 spare) bytes
  - Block size : (256K+16K) bytes
  - Plane size : 2,048 Blocks per Plane
  - Device size
    4Gb: 1 Plane per Device or 512Mbytes
    8Gb: 4Gb DDP (2 stack, 1 CE#)
    16Gb: 4Gb QDP (4 stack, 1 CE#)
- **PAGE READ / PROGRAM**
  - Random access: 30 µs (Max)
  - Sequential access: 45 ns (Min)
  - Program time / Multiplane Program time: 300 µs (Typ)
- **BLOCK ERASE / MULTIPLANE ERASE**
  - Block Erase time: 3.5 ms (Typ)
- **OPERATING TEMPERATURE**
  : -40°C ~ 85 °C (Industrial)
- **COMMAND SET**
  - ONFI1.0 Compliant command set
  - Read Unique ID
- **SECURITY**
  - One Time Programmable (OTP) area
  - Voltage/Non-Voltage Protection
  - Serial number (unique ID)
- **PACKAGE**
  - 63-Ball FBGA (9.0 x 11 x 1.0 mm)
  - Lead/Halogen Free
- **ADDITIONAL FEATURES**
  - Supports Copy Back Program
  - Supports Read Cache
- **ELECTRONIC SIGNATURE**
  - Manufacturer ID: ADh or 01h
- **RELIABILITY**
  - 100,000 Program / Erase cycles (Typ)
    (with 4-bit ECC per 528 bytes (x8) or 264 words (x16))
  - 10 Year Data retention (Typ)
  - Block zero is a valid block and will be valid for at least 1000 program-erase cycles
- **OTHERS**
  - This product is compliance with the RoHS directive

1. General Description

The JSC NAND Flash is offered in 1.8 VCC and VCCQ power supply, and with x8 or x16 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

Each block can be programmed and erased up to 60,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

The devices have a Read Cache feature that improves the read throughput for large files. During cache reading, the devices load the data in a cache register while the previous data is transferred to the I/O buffers to be read.
In addition, thanks to multiplane architecture, it is possible to program two pages at a time (one per plane) or to erase two blocks at a time (again, one per plane). The multiplane architecture allows program and erase time to be reduced by 50%.
In multiplane operations, data in the page can be read out at 45 ns cycle time per byte. The I/O pins serve as the ports for command and address input as well as data input/output. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of the footprint.

Commands, Data, and Addresses are asynchronously introduced using CE#, WE#, ALE, and CLE control pins.
The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data. A WP# pin is available to provide hardware protection against program and erase operations.

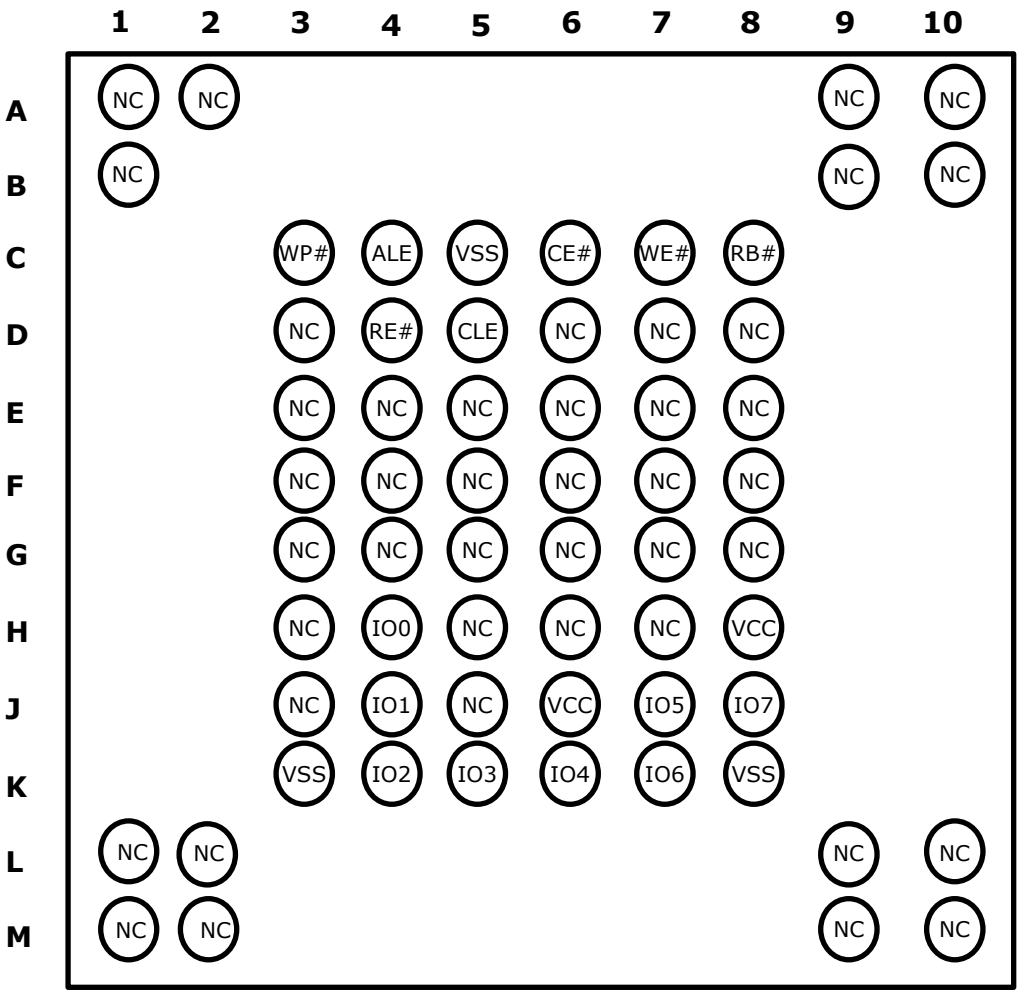
The output pin R/B# (open drain buffer) signals the status of the device during each operation. It identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to connect to a single pull-up resistor. In a system with multiple memories the R/B# pins can be connected all together to provide a global status signal.

The Reprogram function allows the optimization of defective block management — when a Page Program operation fails the data can be directly programmed in another page inside the same array section without the time-consuming serial data insertion phase. The Copy Back operation automatically executes embedded error detection operation: 1-bit error out of every 528 bytes (x8) or 256 words (x16) can be detected. With this feature it is no longer necessary to use an external mechanism to detect Copy Back operation errors.

Multiplane Copy Back is also supported. Data read out after Copy Back Read (both for single and multiplane cases) is allowed.
In addition, Cache Program and Multiplane Cache Program operations improve the programming throughput by programming data using the cache register.
The devices provide two innovative features: Page Reprogram and Multiplane Page Reprogram. The Page Reprogram re-programs one page. Normally, this operation is performed after a failed Page Program operation. Similarly, the Multiplane Page Reprogram re-programs two pages in parallel, one per plane. The first page must be in the first plane while the second page must be in the second plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The Page Reprogram and Multiplane Page Reprogram guarantee improved performance, since data insertion can be omitted during re-program operations.

Note: This device do not support EDC.

PIN CONFIGURATION (63Ball FBGA, 9mm x 11mm, x8)



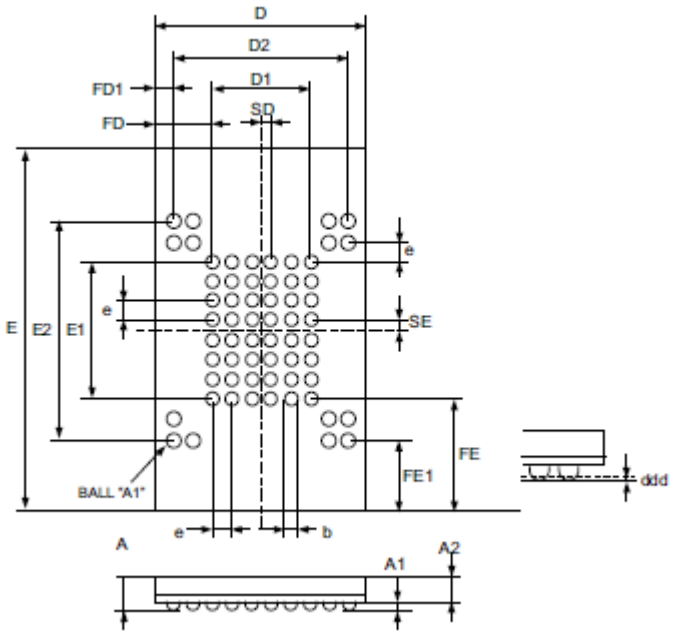


Figure 1.0 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Package Outline

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
B	0.40	0.45	0.50
D	8.9	9.00	9.10
D1		4.00	
D2		7.20	
E	10.90	11.00	11.10
E1		5.60	
E2		8.80	
e		0.80	
FD		2.50	
FD1		0.90	
FE		2.70	
FE1		1.10	
SD		0.40	
SE		0.40	

Table 1.0 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Package Mechanical Data

The devices come with the following security features:
◆ OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
◆ Serial number (unique identifier), which allows the devices to be uniquely identified.
These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the data sheet. For more details about them, contact your nearest JSC sales office.

Device	Density (bits)		Number of Planes	Number of Blocks per Plane
	Main	Spare		
4Gb	512M x 8 256M x 16	32M x 8 16M x16	1	2,048

1.1 Logic Diagram

Figure 1.1 Logic Diagram

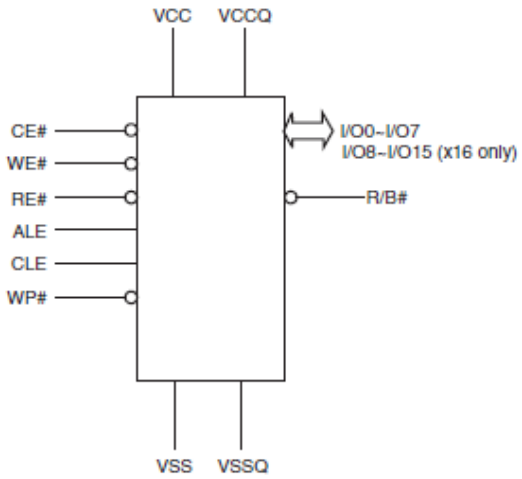


Table 1.1 Signal Names

I/O7 - I/O0 **(x8)**	Data Input / Outputs
I/O8 - I/O15 **(x16)**	
CLE	Command Latch Enable
ALE	Address Latch Enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
R/B#	Read/Busy
VCC	Power Supply
VSS	Ground
NC	Not Connected

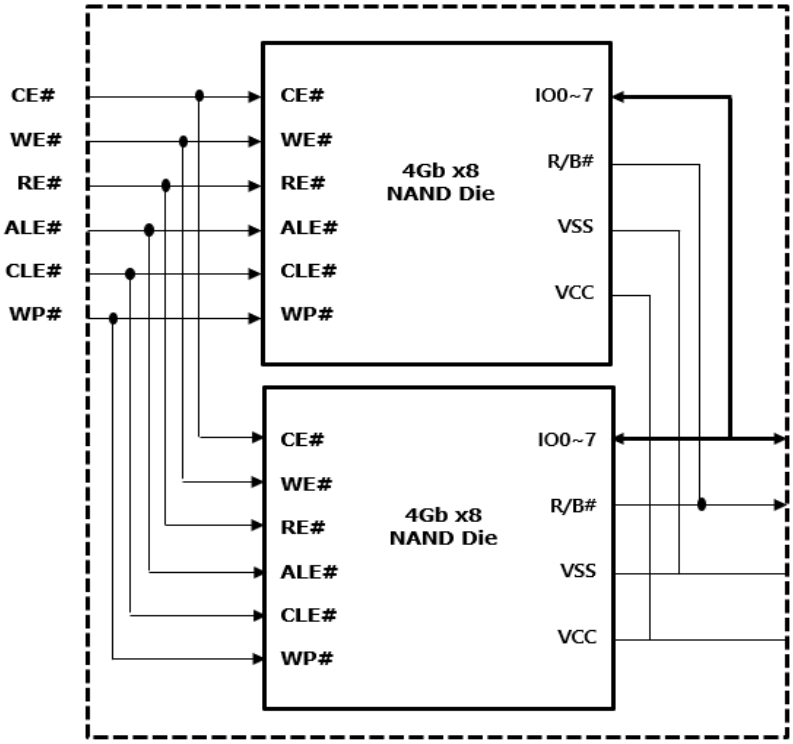


Figure 1.12 : 8Gb PKG Block diagram

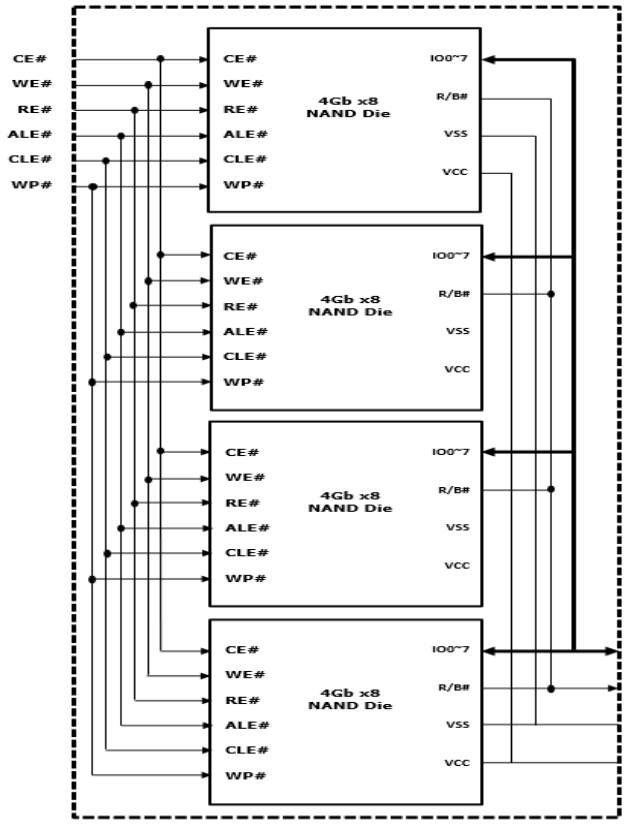


Figure 1.13 : 16Gb PKG Block diagram

1.2 Pin Description

Table 1.2 Pin Description

Pin Name	Pin Function
I/O0 - I/O7 (x8)	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O8 - I/O15 (x16) I/O pins float to High-Z when the device is deselected, or the outputs are disabled.
I/O8 - I/O15 (x16)	
CLE	**Command Latch Enable**. This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#)
ALE	**Address Latch Enable**. This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable**. This input controls the selection of the device. When the device is not busy CE# low selects the memory
WE#	**Write Enable**. This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable**. The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect**. The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when VCC is less than VLKO.
VSS	**Ground**
NC	**Not connected**.

Notes:
1. A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever VCC is below 1.1V to protect the device from any involuntary program/erase during power transitions.

1.3 Block Diagram

Figure 1.2 Functional Block Diagram

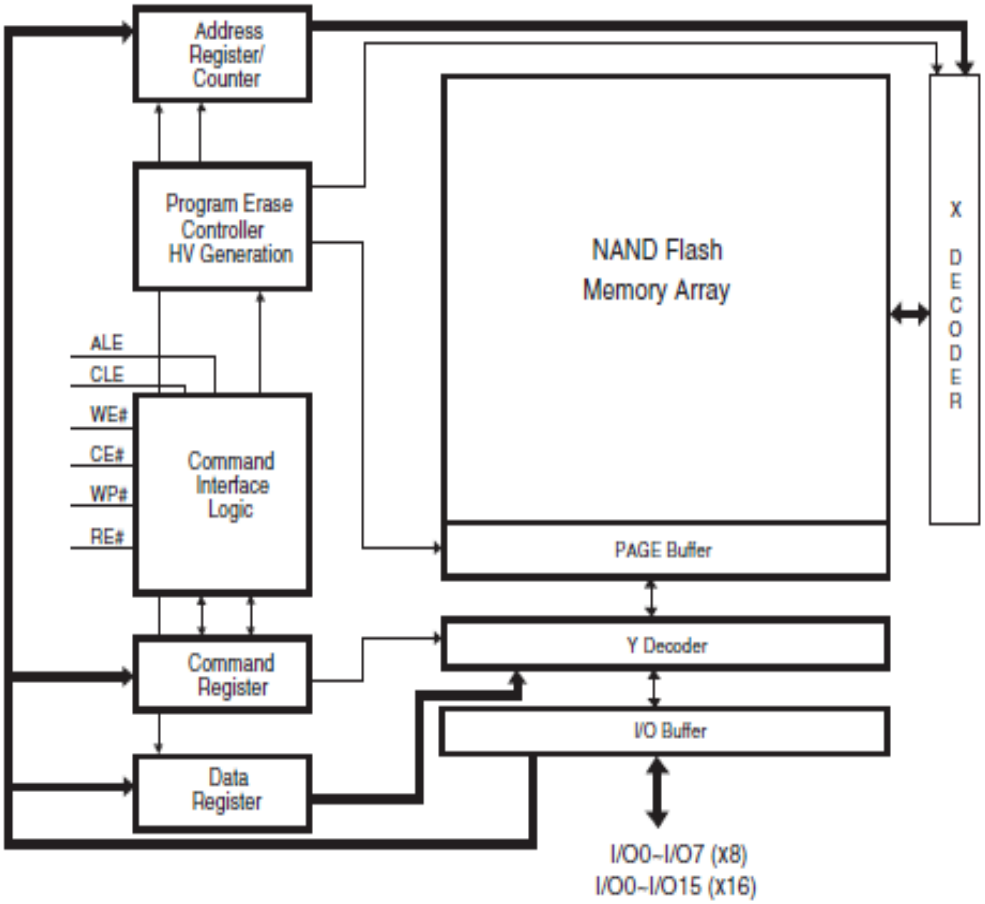
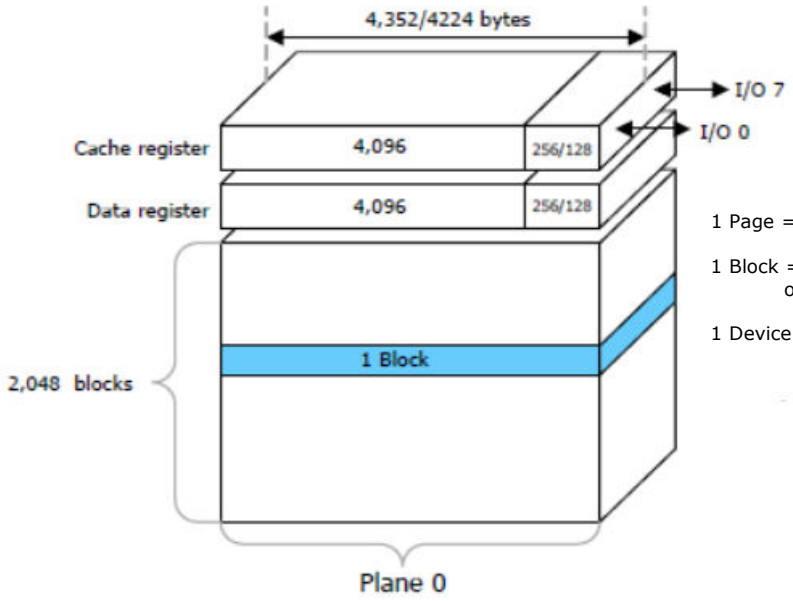


Figure 1.3 Array Organization — For each 4Gb device



1 Page = (4k + 256) bytes or (4k + 128) bytes

1 Block = (4k + 256) bytes x 64 pages = (256k + 16k) bytes
or (4k + 128) bytes x 64 pages = (256k + 8k) bytes

1 Device = (256k + 16k) bytes x 2048 blocks
or (256k + 8k) bytes x 2048 blocks

Table 1.4 4Gb Address Cycle Map

Bus Cycle	I/O[15:8]	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	-	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	-	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	A12(CA12)	Low	Low	Low
3rd	-	A13(PA0)	A14(PA1)	A15(PA2)	A16(PA3)	A17(PA4)	A18(PA5)	A19(BA0)	A20(BA1)
4th	-	A21(BA2)	A22(BA3)	A23(BA4)	A24(BA5)	A25(BA6)	A26(BA7)	A27(BA8)	A28(BA9)
5th	-	A29(BA10)	Low	Low	Low	Low	Low	Low	Low
X16									
1st	Low	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	Low	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	Low	Low	Low	Low
3rd	Low	A12(PA0)	A13(PA1)	A14(PA2)	A15(PA3)	A16(PA4)	A17(PA5)	A18(BA0)	A19(BA1)
4th	Low	A20(BA2)	A21(BA3)	A22(BA4)	A23(BA5)	A24(BA6)	A25(BA7)	A26(BA8)	A27(BA9)
5th	Low	A28(BA10)	Low	Low	Low	Low	Low	Low	Low

Notes 1:
1. CAx = Column Address bit.
2. PAx = Page Address bit.
3. PA0 = Plane Address bit zero.
3. BAx = Block Address bit.
4. Block address concatenated with page address = actual page address.
5. I/O[15:8] are not used during the addressing sequence and should be driven Low.

For the x8 address bits, the following rules apply:
A0 - A12: column address in the page
A13 - A18: page address in the block
A19 - A29: block address

Notes 2:
1. Low must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

Table 1.4 8Gb Address Cycle Map

Bus Cycle	I/O[15:8]	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	-	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	-	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	A12(CA12)	Low	Low	Low
3rd	-	A13(PA0)	A14(PA1)	A15(PA2)	A16(PA3)	A17(PA4)	A18(PA5)	A19(BA0)	A20(BA1)
4th	-	A21(BA2)	A22(BA3)	A23(BA4)	A24(BA5)	A25(BA6)	A26(BA7)	A27(BA8)	A28(BA9)
5th	-	A29(BA10)	A30(BA11)	Low	Low	Low	Low	Low	Low
X16									
1st	Low	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	Low	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	Low	Low	Low	Low
3rd	Low	A12(PA0)	A13(PA1)	A14(PA2)	A15(PA3)	A16(PA4)	A17(PA5)	A18(BA0)	A19(BA1)
4th	Low	A20(BA2)	A21(BA3)	A22(BA4)	A23(BA5)	A24(BA6)	A25(BA7)	A26(BA8)	A27(BA9)
5th	Low	A28(BA10)	A29(BA11)	Low	Low	Low	Low	Low	Low

Notes 1:
1. CAx = Column Address bit.
2. PAx = Page Address bit.
3. PA0 = Plane Address bit zero.
3. BAx = Block Address bit.
4. Block address concatenated with page address = actual page address.
5. I/O[15:8] are not used during the addressing sequence and should be driven Low.
6. A30 for 8Gb(4Gb x2 – DDP, 1CE)

For the x8 address bits, the following rules apply:
A0 - A12: column address in the page
A13 - A18: page address in the block
A19 - A29: block address
A30 for 8Gb DDP(1CE)

Notes 2:
1. Low must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

Table 1.4 16Gb Address Cycle Map

Bus Cycle	I/O[15:8]	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	-	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	-	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	A12(CA12)	Low	Low	Low
3rd	-	A13(PA0)	A14(PA1)	A15(PA2)	A16(PA3)	A17(PA4)	A18(PA5)	A19(BA0)	A20(BA1)
4th	-	A21(BA2)	A22(BA3)	A23(BA4)	A24(BA5)	A25(BA6)	A26(BA7)	A27(BA8)	A28(BA9)
5th	-	A29(BA10)	A30(BA11)	A31(BA12)	Low	Low	Low	Low	Low
X16									
1st	Low	A0(CA0)	A1(CA1)	A2(CA2)	A3(CA3)	A4(CA4)	A5(CA5)	A6(CA6)	A7(CA7)
2nd	Low	A8(CA8)	A0(CA9)	A10(CA10)	A11(CA11)	Low	Low	Low	Low
3rd	Low	A12(PA0)	A13(PA1)	A14(PA2)	A15(PA3)	A16(PA4)	A17(PA5)	A18(BA0)	A19(BA1)
4th	Low	A20(BA2)	A21(BA3)	A22(BA4)	A23(BA5)	A24(BA6)	A25(BA7)	A26(BA8)	A27(BA9)
5th	Low	A28(BA10)	A29(BA11)	A30(BA12)	Low	Low	Low	Low	Low

Notes 1:
1. CAx = Column Address bit.
2. PAx = Page Address bit.
3. PA0 = Plane Address bit zero.
3. BAx = Block Address bit.
4. Block address concatenated with page address = actual page address.
5. I/O[15:8] are not used during the addressing sequence and should be driven Low.
6. A30, A31 for 16Gb(4Gb x4 – QDP, 1CE)

For the x8 address bits, the following rules apply:
A0 - A12: column address in the page
A13 - A18: page address in the block
A19 - A29: block address
A30, A31 for 16Gb QDP(1CE)

Notes 2:
1. Low must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

1.6 Mode Selection

Table 1.5 Mode Selection

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read Mode	Command Input	High	Low	Low	Rising	High	X
	Address Input	Low	High	Low	Rising	High	X
Program or Erase Mode	Command Input	High	Low	Low	Rising	High	High
	Address Input	Low	High	Low	Rising	High	High
Data Input		Low	Low	Low	Rising	High	High
Data Output (ongoing)		Low	Low	Low	High	Falling	X
Data Output (suspended)		X	X	X	High	High	X
Busy Time in Read		X	X	X	High	High *3	X
Busy Time in Program		X	X	X	X	X	High
Busy Time in Erase		X	X	X	X	X	High
Write Protect		X	X	X	X	X	Low
Stand By		X	X	High	X	X	0V / Vcc *2

Notes:
1. X can be V_{IL} or V_{IH}. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. During Busy Time in Read, RE# must be held high to prevent unintended data out.

2. Bus Operation

There are six standard bus operations that control the device: Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. (See Table 1.5)

Typically, glitches less than 5 ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

The Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable high, Address Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 6.1 and Table 5.4 for details of the timing requirements. Command codes are always applied on I/O7:0 regardless of the bus configuration.

2.2 Address Input

The Address Input bus operation allows the insertion of the memory address. For the 4Gb device, five write cycles are needed to input the addresses.

Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 6.2 and Table 5.4 for details of the timing requirements. Addresses are always applied on I/O7:0 regardless of the bus configuration. Refer to Table 1.3 for more detailed information.

2.3 Data Input

The Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable high, and Write Protect high and latched on the rising edge of Write Enable. See Figure 6.3 and Table 5.4 for details of the timing requirements.

2.4 Data Output

The Data Output bus operation allows data to be read from the memory array and to check the Status Register content, and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low. See Figure 6.4 and Table 5.4 for details of the timing's requirements.

2.5 Write Protect

The Hardware Write Protection is activated when the Write Protect pin is low. In this condition, modify operations do not start and the content of the memory is not altered. The Write Protect pin is not latched by Write Enable to ensure the protection even during power up.

2.6 Standby

In Standby, the device is deselected, outputs are disabled, and power consumption is reduced.

3. Command Set

Table 3.1 Command Set

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable Command During Busy	Supported On
Page Read	00h	30h			NO	Yes
Page Program	80h	10h			NO	Yes
Random Data Input	85h				NO	Yes
Random Data Output	05h	E0h			NO	Yes
Multiplane Program	80h	11h	81h	10h	NO	Yes
ONFI Multiplane Program	80h	11h	80h	10h	NO	Yes
Page Reprogram	8Bh	10h			NO	Yes
Multiplane Page Reprogram	8Bh	11h	8Bh	10h	NO	Yes
Block Erase	60h	D0h			NO	Yes
Multiplane Block Erase	60h	60h	D0h		NO	Yes
ONFI Multiplane Block Erase	60h	D1h	60h	D0h	NO	Yes
Copy Back Read	00h	35h			NO	Yes
Copy Back Program	85h	10h			NO	Yes
Multiplane Copy Back Program	85h	11h	81h	10h	NO	Yes
ONFI Multiplane Copy Program	85h	11h	85h	10h	NO	Yes
Special Read For Copy Back	00h	36h			NO	Yes
Read Status Register	70h				Yes	Yes
Read Status Enhanced	78h				Yes	Yes
Reset	FFh				Yes	Yes
Read Cache	31h				NO	Yes
Read Cache Enhanced	00h	31h			NO	Yes
Read Cache End	3Fh				NO	Yes
Cache Program (End)	80h	10h			NO	Yes
Cache Program (Start)/(Continue)	80h	15h			NO	Yes
Multiplane Cache Program (Start/Continue)	80h	11h	81h	15h	NO	Yes
ONFI Multiplane Cache Program (Start/Continue)	80h	11h	80h	15h	NO	Yes
Multiplane Cache Program(End)	80h	11h	81h	10h	NO	Yes
ONFI Multiplane Cache Program(End)	80h	11h	80h	10h	NO	Yes
Read ID	90h				NO	Yes
Read ONFI Signature	90h				NO	Yes
Read Parameter Page	ECh				NO	Yes
Read Unique ID	EDh				NO	Yes

3.1 Page Read

Page Read is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read and serial page read.
Random read mode is enabled when the page address is changed. All data within the selected page are transferred to the data registers. The system controller may detect the completion of this data transfer (tR) by analyzing the output of the R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45 ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# signal makes the device output the data, starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing Random Data Output command. The column address of next data, which is going to be out, may be changed to the address that follows Random Data Output command. Random Data Output can be performed as many times as needed.
After power up, the device is in read mode, so 00h command cycle is not necessary to start a read operation.
Any operation other than read or Random Data Output causes the device to exit read mode.
See Figure 6.6 and Figure 6.12 as references.

3.2 Page Program

2K and 4K devices contain 2,048 and 4,096 erasable blocks, divided into 64 programmable pages.
Each page can be divided into several cases according to the size of the page and spare area.

- Case: (Page Size + Spare Area)

	1Gb	2Gb		4Gb	
Page	2k	2k		2k	4k
Spare	64	64	128	128	256
Byte (x8)	2,112	2,112	2,176	2,176	4,352
Word (x16)	1,056	1,056	1,088	1,088	2,176

A page program cycle consists of a serial data loading period in which up to 4,352 of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs (four cycles for 1Gb) and then serial data. The words other than those to be programmed do not need to be loaded. The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address that follows the Random Data Input command (85h). Random Data Input may be performed as many times as needed.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks.

Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 6.9 and Figure 6.11 detail the sequence.

The device is programmable by page, but it also allows multiple partial page programming of a word or consecutive bytes up to the full page in a single page program cycle.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 5.7. In addition, pages must be sequentially programmed within a block.

If a Page Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.3 Multiplane Program

The 4Gb devices support Multiplane Program, making it possible to program two pages in parallel, one page per plane.
A Multiplane Program cycle consists of a double serial data loading period in which up to 4,352 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. The address for this page must be in the 1st plane (PLA0 = 0). The device supports Random Data Input exactly the same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, the '81h' command must be issued, followed by 2nd page address (5 cycles) and its serial data input. The address for this page must be in the 2nd plane (PLA0 = 1). The Program Confirm command (10h) starts parallel programming of both pages.

Figure 6.13 describes the sequences using the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes.
Figure 6.14 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (tDBSY). In case of failure in either page program, the failure bit of the Status Register will be set. Refer to Section 3.8 for further info.

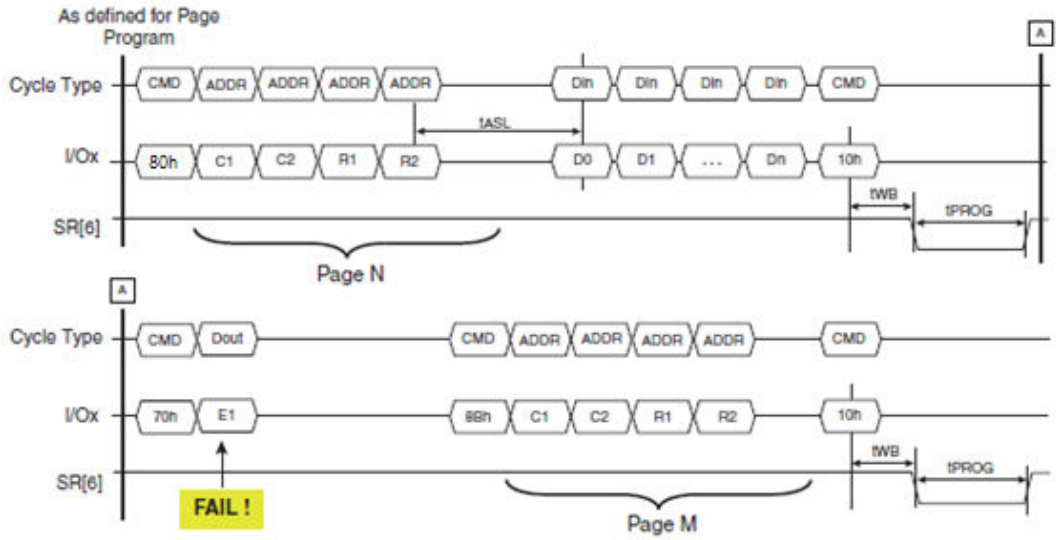
The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 5.7. Pages may be programmed in any order within a block.

If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.4 Page Reprogram

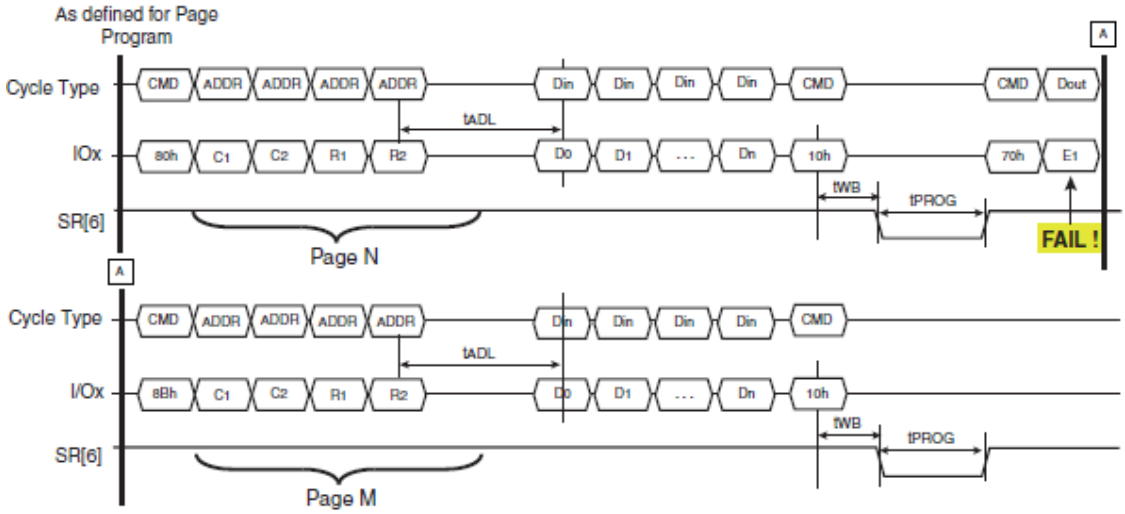
Page Program may result in a failure, which can be detected by Read Status Register. In this event, the host may call Page Reprogram. This command allows the reprogramming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with reprogram setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle, as described in Figure 3.1.

Figure 3.1 Page Reprogram



On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm '10h', as described in Figure 3.2.

Figure 3.2 Page Reprogram with Data Manipulation



The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address which follows the Random Data Input command (85h). Random Data Input may be operated multiple times regardless of how many times it is done in a page.

The Program Confirm command (10h) initiates the re-programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register.
Only the Read Status command and Reset command are valid when programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register.

The Page Reprogram must be issued in the same plane as the Page Program that failed. In order to program the data to a different plane, use the Page Program operation instead. The Multiplane Page Reprogram can re-program two pages in parallel, one per plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The command sequence is very similar to Figure 6.13, except that it requires the Page Reprogram Command (8Bh) instead of 80h and 81h.
If a Page Reprogram operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.5 Block Erase
The Block Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only the block address bits are valid while the page address bits are ignored.

The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process.
This two-step sequence of setup followed by the execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase, and erase verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register.

The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O0) may be checked. Figure 6.15 details the sequence.

If a Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted block is erased under continuous power conditions before that block can be trusted for further programming and reading operations.

3.6 Multiplane Block Erase
Multiplane Block Erase allows the erase of two blocks in parallel, one block per memory plane.
The Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See Table for performance information.
For the Multiplane Block Erase operation, the address of the first block must be within the first plane (PLA0 = 0) and the address of the second block in the second plane (PLA0 = 1). See Figure 6.16 for a description of the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure 6.17 51 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (tDBSY). In case of failure in either erase, the failure bit of the Status Register will be set. Refer to Section 3.8 for further info.
If a Multiplane Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted blocks are erased under continuous power conditions before those block can be trusted for further programming and reading operations.

3.7 Copy Back Program
The copy back feature is intended to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also needs to be copied to the newly assigned free block. The operation for performing a copy back is a sequential execution of page-read (without mandatory serial access) and Copy Back Program with the address of destination page.

A read operation with the '35h' command and the address of the source page moves the whole 4,352-byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE# (see Figure 6.18), or Copy Back Program command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation.

Source and Destination page in the Copy Back Program sequence must belong to the same device plane. Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (tPROG) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).

The data input cycle for modifying a portion or multiple distinct portions of the source page is allowed as shown in Figure 6.19.

If a Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete

3.7.1 Multiplane Copy Back Program

The device supports Multiplane Copy Back Program with exactly the same sequence and limitations as the Page Program. Multiplane Copy Back Program must be preceded by two single page Copy Back Read command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multiplane Copy Back cannot cross plane boundaries — the contents of the source page of one device plane can be copied only to a destination page of the same plane.
The Multiplane Copy Back Program sequence represented in Figure 6.20 shows the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure 6.21 describes the sequence using the ONFI protocol.
For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.7.2 Special Read for Copy Back

The device features the "Special Read for Copy Back." If Copy Back Read (described in Section 3.7 and Section 3.7.1) is triggered with confirm command '36h' instead '35h', Copy Back Read from target page(s) will be executed with an increased internal (VPASS) voltage.
This special feature is used in order to minimize the number of read errors due to over-program or read disturb — it shall be used only if ECC read errors have occurred in the source page using Page Read or Copy Back Read sequences.
Excluding the Copy Back Read confirm command, all other features described in Section 3.7 and Section 3.7.1 for standard copy back remain valid (including the figures referred to in those sections).

3.8 Read Status Register

The Status Register is used to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. Refer to Section 3.2 for specific Status Register definition, and to Figure 6.22 for timings.

If the Read Status Register command is issued during multiplane operations, then Status Register polling will return the combined status value related to the outcome of the operation in the two planes according to the following table:

Status Register Bit	Composite Status Value
Bit 0, Pass/Fail	OR
Bit1, Cache Pass/Fail	OR

In other words, the Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

The command register remains in Status Read mode until further commands are issued. Therefore, if the Status Register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Note: The Read Status Register command shall not be used for concurrent operations in multi-die stack configurations (single CE#). "Read Status Enhanced" shall be used instead.

3.9 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the case of multiplane operations in the same die.
Figure 6.23 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.
Refer to Table 3.2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued.
The Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

3.10 Read Status Register Field Definition

Table 3.2 below lists the meaning of each bit of the Read Status Register and Read Status Enhanced.

Table 3.2 Status Register Coding

ID	Page Program / Page Reprogram	Block Erase	Read	Read Cache	Cache Program / Cache Reprogram	Coding
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail	N Page Pass : 0 Fail : 1
1	NA	NA	NA	NA	Pass / Fail	N -1 Page Pass : 0 Fail : 1
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Internal Data Operation Active : 0 Idle :1
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy Busy : 0 Ready : 1
7	Write Protect	Write Protect	NA	NA	Write Protect	Protected : 0 Not Protected :1

3.11 Reset

The Reset feature is executed by writing FFh to the command register. If the device is in Busy state during random read, program, or erase mode, the Reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data may be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high or value 60h when WP# is low. If the device is already in reset state a new Reset command will not be accepted by the command register. The R/B# pin transitions to low for tRST after the Reset command is written. Refer to Figure 6.24 for further details. The Status Register can also be read to determine the status of a Reset operation.

3.12 Read Cache

Read Cache can be used to increase the read operation speed, as defined in Section 3.1, and it cannot cross a block boundary. As soon as the user starts to read one page, the device automatically loads the next page into the cache register. Serial data output may be executed while data in the memory is read into the cache register. Read Cache is initiated by the Page Read sequence (00-30h) on a page M.

After random access to the first page is complete (R/B# returned to high, or Read Status Register I/O6 switches to high), two command sequences can be used to continue read cache:

◆ Read Cache (command '31h' only): once the command is latched into the command register (see Figure 6.26), device goes busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, the cache register data can be output by toggling RE# while the next page (page address M+1) is read from the memory array into the data register.

◆ Read Cache Enhanced (sequence '00h' <page N address> '31'): once the command is latched into the command register (see Figure 6.27), device goes busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, cache register data can be output by toggling RE# while page N is read from the memory array into the data register.

Subsequent pages are read by issuing additional Read Cache or Read Cache Enhanced command sequences. If serial data output time of one page exceeds random access time (tR), the random access time of the next page is hidden by data downloading of the previous page.

On the other hand, if 31h is issued prior to completing the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.

To terminate the Read Cache operation, 3Fh command should be issued (see Figure 6.28). This command transfers data from the data register to the cache register without issuing next page read.

During the Read Cache operation, the device doesn't allow any other command except for 00h, 31h, 3Fh, Read SR, or Reset (FFh). To carry out other operations, Read Cache must be terminated by the Read Cache End command (3Fh) or the device must be reset by issuing FFh.

Read Status command (70h) may be issued to check the status of the different registers and the busy/ready status of the cached read operations.

◆ The Cache-Busy status bit I/O6 indicates when the cache register is ready to output new data.

◆ The status bit I/O5 can be used to determine when the cell reading of the current data register contents is complete.

***Note**:* The Read Cache and Read Cache End commands reset the column counter, thus, when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random Data Output command can be used to switch column address

3.13 Cache Program

Cache Program can be used with 4Gb device to improve the program throughput by programming data using the cache register. The cache program operation cannot cross a block boundary. The cache register allows new data to be input while the previous data that was transferred to the data register is programmed into the memory array.
After the serial data input command (80h) is loaded to the command register, followed by five cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in the Busy state for a short time (tCBSYW). After all data of the cache register is transferred into the data register, the device returns to the Ready state and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data from the cache register to the data register. Cell programming the data of the data register and loading of the next data into the cache register is consequently processed through a pipeline model.
In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tCBSYW).
Read Status commands (70h or 78h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations.
▪ The Cache-Busy status bit I/O6 indicates when the cache register is ready to accept new data.
▪ The status bit I/O5 can be used to determine when the cell programming of the current data register contents is complete.
▪ The cache program error bit I/O1 can be used to identify if the previous page (page N-1) has been successfully programmed or not in a cache program operation. The status bit is valid upon I/O6 status bit changing to 1.
▪ The error bit I/O0 is used to identify if any error has been detected by the program/erase controller while programming page N. The status bit is valid upon I/O5 status bit changing to 1.
I/O1 may be read together with I/O0.

If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. See Table 3.2 and Figure 6.29 for more details.

If a Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.14 Multiplane Cache Program

The Multiplane Cache Program enables high program throughput by programming two pages in parallel, while exploiting the data and cache registers of both planes to implement cache.

The command sequence can be summarized as follows:

◆ Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (PLA0 = 0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports Random Data Input exactly like Page Program operation.
◆ The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

◆ Once device returns to ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (PLA0 = 1). The data of 2nd page other than those to be programmed do not need to be loaded.
◆ Cache Program confirm command (15h). Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in the Busy state for a short time (tCBSYW). After all data from the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence 80h-...- 11h...-...81h...-...15h can be iterated, and each time the device will be busy for the tCBSYW time needed to complete programming the current data register contents, and transferring the new data from the cache registers. The sequence to end Multiplane Cache Program is 80h-...- 11h...-...81h...- ...10h.
The Multiplane Cache Program is available only within two paired blocks in separate planes. Figure 6.30 shows the legacy protocol for the multiplane cache program operation. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes.
Figure 6.31 shows the ONFI protocol for the multiplane cache program operation. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
The user can check operation status by R/B# pin or Read Status Register commands (70h or 78h). If the user opts for 70h, Read Status Register will provide "global" information about the operation in the two planes.
I/O6 indicates when both cache registers are ready to accept new data.
I/O5 indicates when the cell programming of the current data registers is complete.
I/O1 identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not.
This status bit is valid upon I/O6 status bit changing to 1.
I/O0 identifies if any error has been detected by the program/erase controller while programming the two pages N. This status bit is valid upon I/O5 status bit changing to 1.
See Table 3.2 for more details.
If the system monitors the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. Refer to Section 3.8 for further information.
If a Multiplane Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.15 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

***Note**:* If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).

Table 3.3 Read ID for Supported Configurations

Density	Org	Vcc	1st	2nd	3rd	4th	5th
4Gb(4K)	x 8	1.8V	ADh	ACh	80h	16h	20h
8Gb(4K)	x 8	1.8V	ADh	A3h	81h	16h	20h
16Gb(4K)	x 8	1.8V	ADh	A5h	82h	16h	20h

3.17 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 6.33 shows the operation sequence.

3.18 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The command register remains in Parameter Page mode until further commands are issued to it. Figure 6.34 shows the operation sequence, while Table 3.4 explains the parameter fields.

***Note**:* For 32nm JSC NAND, for a particular condition, the Read Parameter Page command does not give the correct values. To over come this issue, the host must issue a Reset command before the Read Parameter Page command. Issuance of Reset before the Read Parameter Page command will provide the correct values

Table 3.4 Parameter Page Description (Sheet 1 of 2)

Byte	O/M	Description
Revision Information and Features Block		
0-3	M	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command
10-31		Reserved (0)
Manufacturer Information Block		
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
Memory Organization Block		
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target

Table 3.4 Parameter Page Description (Sheet 2 of 2)

Byte	O/M	Description
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved(0)
Electrical Parameters Block		
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-140	M	t_{CCS} Minimum Change Column setup time (ns)
141-163		Reserved (0)
Vendor Block		
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
Redundant Parameter Pages		
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Note:

1. *O" Stands for Optional, "M" for Mandatory.*
2. *ONFI Table is not matched with product. If you need ONFI function , please contact JSC sales.*
3. *8Gb, 16Gb SLC NAND page parameter values are configured based on value of 4Gb SLC NAND value*

3.19 Read Unique ID

The device supports the ONFI Read Unique ID function, initiated by writing EDh to the command register, followed by an address input of 00h. The host must monitor the R/B# pin or wait for the maximum data transfer time (tR) before reading the Unique ID data. The first sixteen bytes returned by the flash is a unique value. The next sixteen bytes returned are the bit-wise complement of the unique value. The host can verify the Unique ID was read correctly by performing an XOR of the two values. The result should be all ones. The command register remains in Unique ID mode until further commands are issued to it. Figure 6.36 shows the operation sequence, while Table 3.10 shows the Unique ID data contents.

Table 3.5 Unique ID Data Description

Byte	Description
0 - 15	Unique ID
16 - 31	ID Complement
32 - 47	Unique ID
48 - 63	ID Complement
64 - 79	Unique ID
80 - 95	ID Complement
96 - 111	Unique ID
112 - 127	ID Complement
128 - 143	Unique ID
144 - 159	ID Complement
160 - 175	Unique ID
176 - 191	ID Complement
192 - 207	Unique ID
208 - 223	ID Complement
224 - 239	Unique ID
240 - 255	ID Complement
256 - 271	Unique ID
272 - 287	ID Complement
288 - 303	Unique ID
304 - 319	ID Complement
320 - 335	Unique ID
336 - 351	ID Complement
352 - 367	Unique ID
368 - 383	ID Complement
384 - 399	Unique ID
400 - 415	ID Complement
416 - 431	Unique ID
432 - 447	ID Complement
448 - 463	Unique ID
464 - 479	ID Complement
480 - 495	Unique ID
496 - 511	ID Complement

4. Signal Descriptions

4.1 Data Protection and Power On / Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1V.

The power-up and power-down sequence is shown in Figure 6.36, in this case VCC and VCCQ on the one hand (and VSS and VSSQ on the other hand) are shorted together at all times.

The Ready/Busy signal shall be valid within 100 μs after the power supplies have reached the minimum values (as specified on), and shall return to one within 5 ms (max).
During this busy time, the device executes the initialization process (cam reading), and dissipates a current ICC0 (30 mA max), in addition, it disregards all commands excluding Read Status Register (70h).

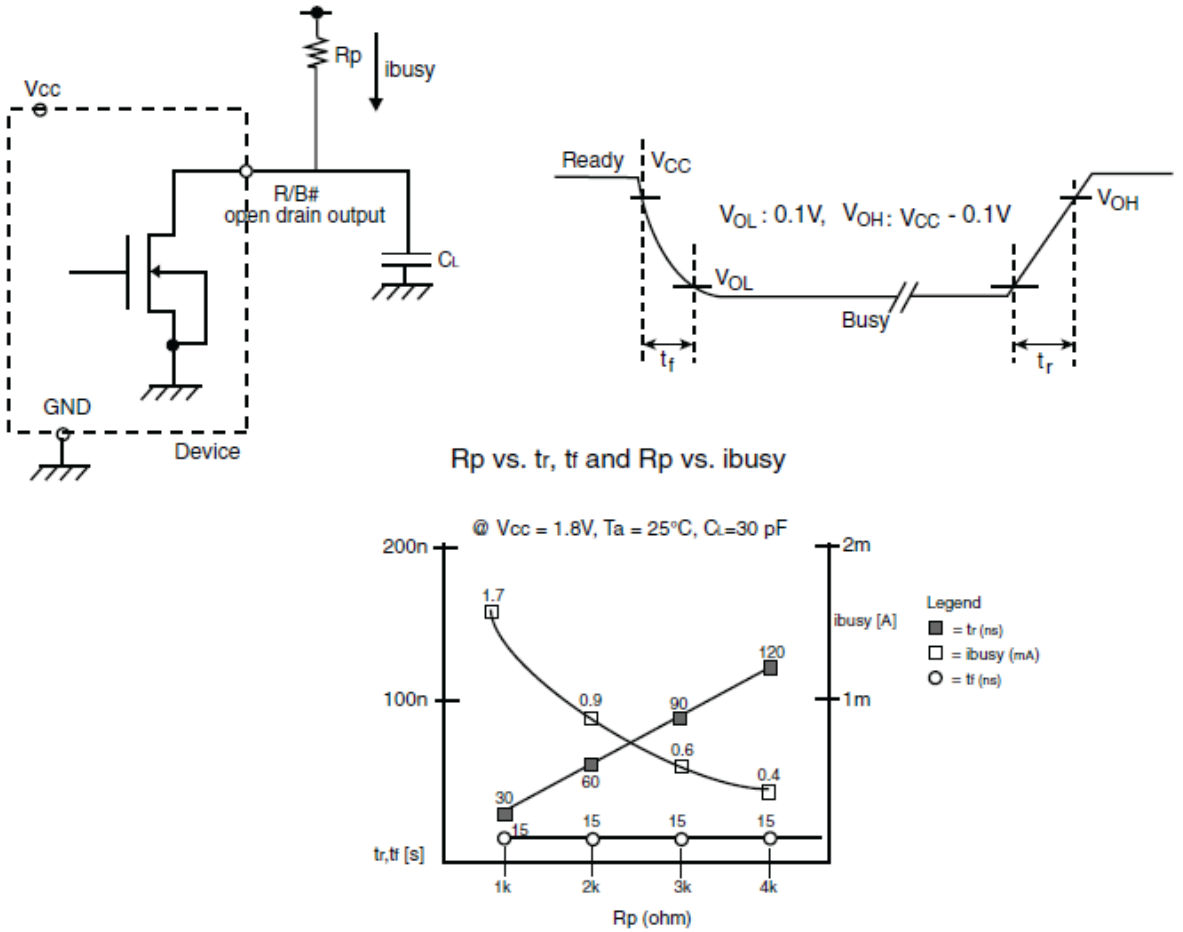
At the end of this busy time, the device defaults into "read setup", thus if the user decides to issue a page read command, the 00h command may be skipped.

The WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 100 μs is required before the internal circuit gets ready for any command sequences as shown in Figure 6.36. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy

The Ready/Busy output provides a method of indicating the completion of a page program, erase, copyback, or read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the reference chart shown in Figure 4.1.

Figure 4.1 Ready/Busy Pin Electrical Application



Rp vs. tr, tf and Rp vs. ibusy

Rp value guidence

$$Rp\ (min.) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \sum I_L} = \frac{1.85V}{3mA + \sum I_L}$$

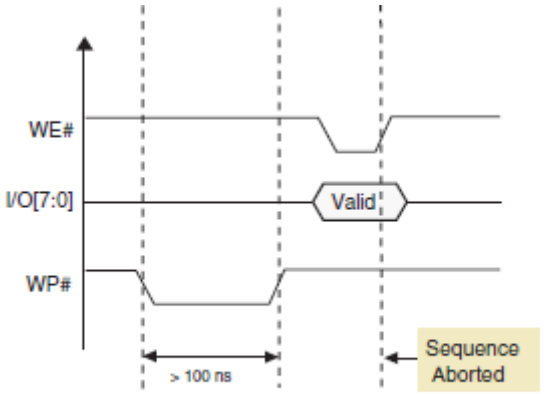
where I_L is the sum of the input currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr.

4.3 Write Protect Operation

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100 ns. Switching WP# low during this time is equivalent to issuing a Reset command (FFh). The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for tRST (similarly to Figure 6.24). At the end of this time, the command register is ready to process the next command, and the Status Register bit I/O6 will be cleared to 1, while I/O7 value will be related to the WP# value. Refer to Table 3.2 for more information on device status.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively, prior to issuing the setup commands (80h or 60h). The level of WP# shall be set tWW ns prior to raising the WE# pin for the set up command, as explained in Figure 6.38 and Figure 6.39.

Figure 4.2 WP# Low Timing Requirements during Program/Erase Command Sequence



5. Electrical Characteristics

5.1 Valid Blocks

Table 5.1 Valid Blocks

NAND	Symbol	Min	Typ	Max	Unit
4Gb Device	N_{VB}	2008	-	2048	Blocks
8Gb Device	N_{VB}	4016	-	4096	Blocks
16Gb Device	N_{VB}	8032	-	8192	Blocks

5.2 Absolute Maximum Ratings

Table 5.2 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Ambient Operating Temperature (Commercial Temperature Range)	T_A	0 to 70	℃
Ambient Operating Temperature (Extended Temperature Range)		-25 to +85	℃
Ambient Operating Temperature (Industrial Temperature Range)		-40 to +85	℃
Temperature under Bias	T_{BIAS}	-50 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Input or Output Voltage	V_{IO} *2	-0.6 to +2.7	V
Supply Voltage	Vcc	-0.6 to +2.7	V

Notes:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the table Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.
3. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions

5.3 AC Test Conditions

Table 5.3 AC Test Conditions

Parameter	Value
Input Pulse Levels	0.0V to Vcc
Input Rise And Fall Times	5 ns
Input And Output Timing Levels	Vcc / 2
Output Load (1.7V - 1.95V)	1 TTL Gate and CL = 30 pF

5.4 AC Characteristics

Table 5.4 AC Characteristics

Parameter	Symbol	Min	Max	Unit
ALE to RE# delay	t_{AR}	10	-	ns
ALE hold time	t_{ALH}	10	-	ns
ALE setup time	t_{ALS}	25	-	ns
Address to data loading time	t_{ADL}	100	-	ns
CE# low to RE# low	t_{CR}	10	-	ns
CE# hold time	t_{CH}	10	-	ns
CE# high to output High-Z	t_{CHZ}	-	30	ns
CLE hold time	t_{CLH}	10	-	ns
CLE to RE# delay	t_{CLR}	10	-	ns
CLE setup time	t_{CLS}	25	-	ns
CE# high to output hold	t_{COH} *3	15	-	ns
CE# high to ALE or CLE don't care	t_{CSD}	10	-	ns
CE# setup time	t_{CS}	35	-	ns
Data hold time	t_{DH}	10	-	ns
Data setup time	t_{DS}	20	-	ns
Data transfer from cell to register	t_{R}	-	30	µs
Output High-Z to RE# low	t_{IR}	0	-	ns
Read cycle time	t_{RC}	45	-	ns
RE# access time	t_{REA}	-	30	ns
RE# high hold time	t_{REH}	15	-	ns
RE# high to output hold	t_{RHOH} *3	15	-	ns
RE# high to WE# low	t_{RHW}	100	-	ns
RE# high to output High-Z	t_{RHZ}	-	100	ns
RE# low to output hold	t_{RLOH}	-	-	ns
RE# pulse width	t_{RP}	25	-	ns
Ready to RE# low	t_{RR}	20	-	ns
Device resetting time (Read/Program/Erase)	t_{RST}	-	5/10/500 *2	µs
WE# high to busy	t_{WB}	-	100	ns
Write cycle time	t_{WC}	45	-	ns
WE# high hold time	t_{WH}	15	-	ns
WE# high to RE# low	t_{WHR}	60	-	ns
WE# high to RE# low for Random data out	t_{WHR2}	200	-	ns
WE# pulse width	t_{WP}	25	-	ns
Write protect time	t_{WW}	100	-	ns

Notes:

1. The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 µs.
3. CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either tCOH or tRHOH will be met.
4. During data output, tCEA depends partly on tCR (CE# low to RE# low). If tCR exceeds the minimum value specified, then the maximum time for tCEA may also be exceeded (tCEA = tCR + tREA).

5.5 DC Characteristics

Table 5.5-1 DC Characteristics and Operating Conditions

Parameter		Symbol	Test Conditions	1.7V ~ 1.95V			Units
				Min	Typ	Max	
Power-On-Reset Current		I_{CC0}	FFh command input after power on	-		50 per device	mA
Operating Current	Read	I_{CC1}	$t_{RC}=t_{RC(min)}$ CE#=V_{IL},I_{OUT}=0mA	-	10	20	mA
	Program	I_{CC2}	Normal	-	-	20	mA
			Cache	-	-	30	mA
	Erase	I_{CC3}	-	-	10	20	mA
Standby Current,(TTL)		I_{CC4}	CE# = V_{IH} WP# = 0V/V_{CC}	-	-	1	mA
Standby Current,(CMOS)		I_{CC5}	CE# = Vcc-0.2 WP# = 0V/V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(Max)	-	-	± 10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(Max)	-	-	± 10	uA
Input High Voltage		V_{IH}	-	Vcc x 0.8	-	Vcc + 0.3	
Input Low Voltage		V_{IL}	-	-0.3	-	Vcc x 0.2	
Output High Voltage		V_{OH}	I_{OH} = -400uA	Vcc-0.1	-	-	
Output Low Voltage		V_{OL}	I_{OL} = -100uA			0.1	
Output Low Currnet (R/B#)		$I_{OL(R/B\#)}$	V_{OL} = 0.1V	3	4	-	mA

Table 5.5-2 AC Test Conditions

Parameter	Value
	1.7V≤Vcc≤1.95V
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	Vcc / 2
Output Load(2.7V-3.6V)	1 TTL GATE and CL=30pF

Notes:
1. These parameters are verified device characterization and are not 100% tested.

5.6 Pin Capacitance

Table 5.6 Pin Capacitance (TA = 25°C, f=1.0 MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input	C_{IN}	V_{IN} = 0V	-	10	pF
Input / Output	C_{IO}	V_{IL} = 0V	-	10	pF

5.7 Program / Erase Characteristics

Table 5.7 Program / Erase Characteristics

Parameter	Description	MIn	Typ	Max	Unit
Program Time	t_{PROG}	-	300	700	us
Dummy Busy Time for Multiplane Program	t_{DBSY}	-	0.5	1	us
Cache Program short busy time	t_{CBSYW}	-	5	t_{PROG}	us
Number of partial Program Cycles in the same page	NOP	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	3.5	10	ms
Read Cache busy time	t_{CBSYR}	-	5	t_R	us

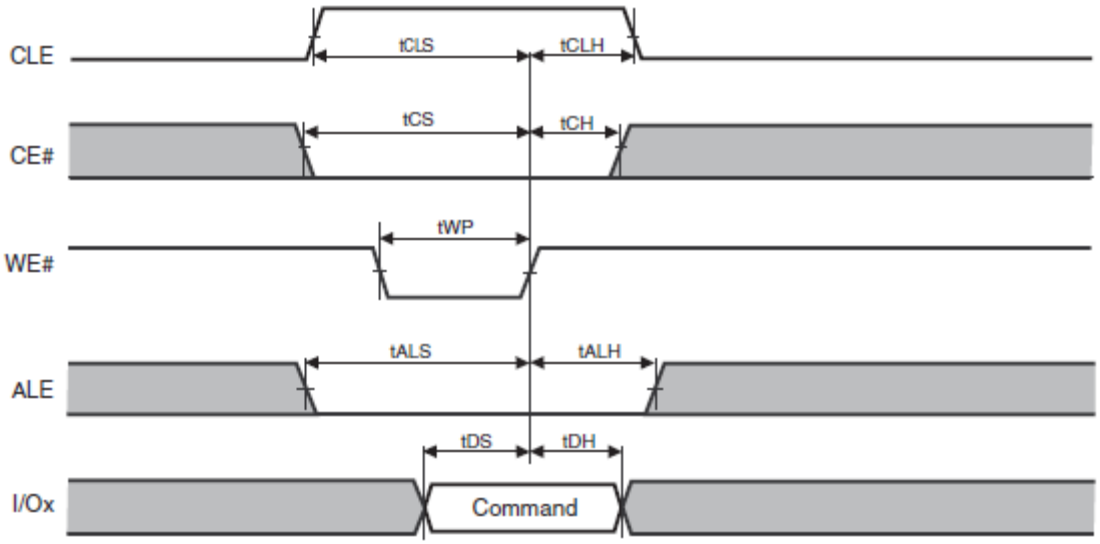
Notes:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed (VCC = 1.8V, 25℃).
2. Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (tPROG) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).

6. Timing Diagrams

6.1 Command Latch Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/ erase) the Write Protect pin must be high.

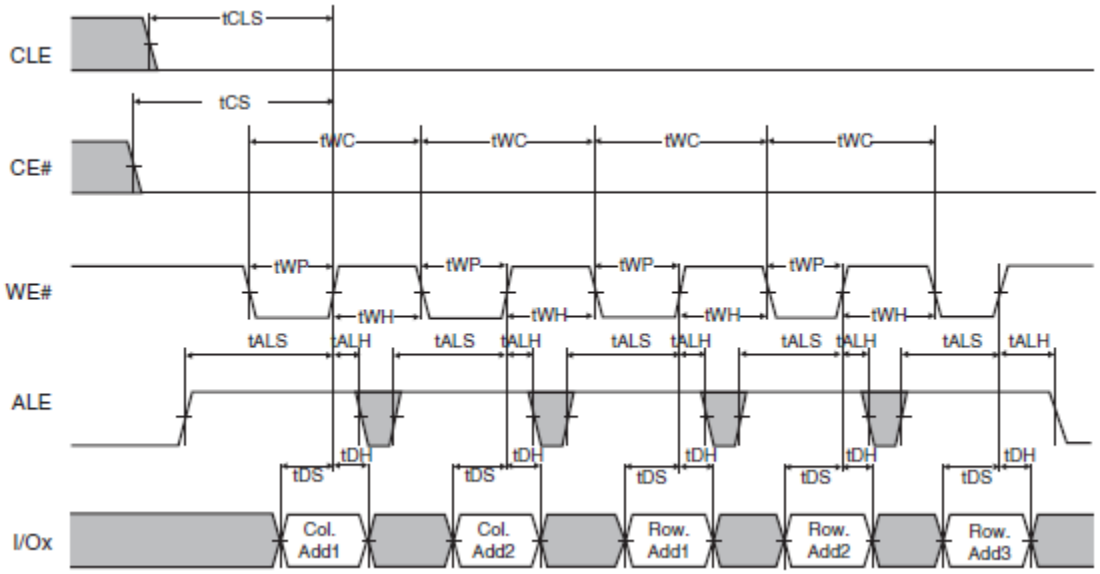
Figure 6.1 Command Latch Cycle



6.2 Address Latch Cycle

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (write/ erase) the Write Protect pin must be high.

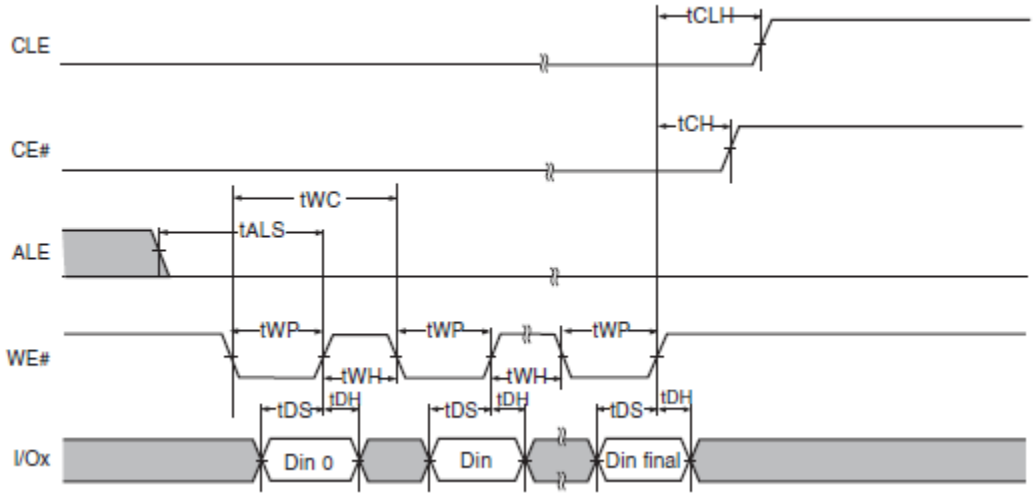
Figure 6.2 Address Latch Cycle



6.3 Data Input Cycle Timing

Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

Figure 6.3 Input Data Latch Cycle

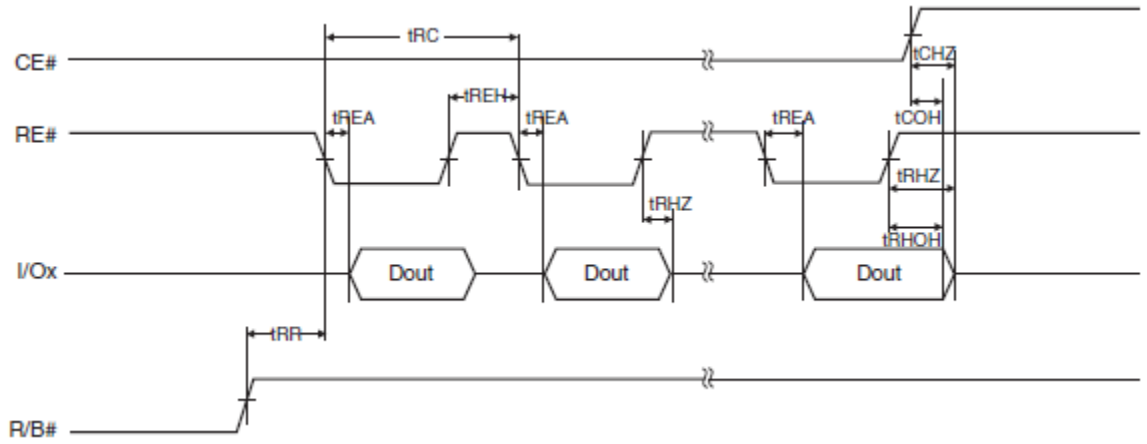


Note:

Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

6.4 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L, WP#=H)

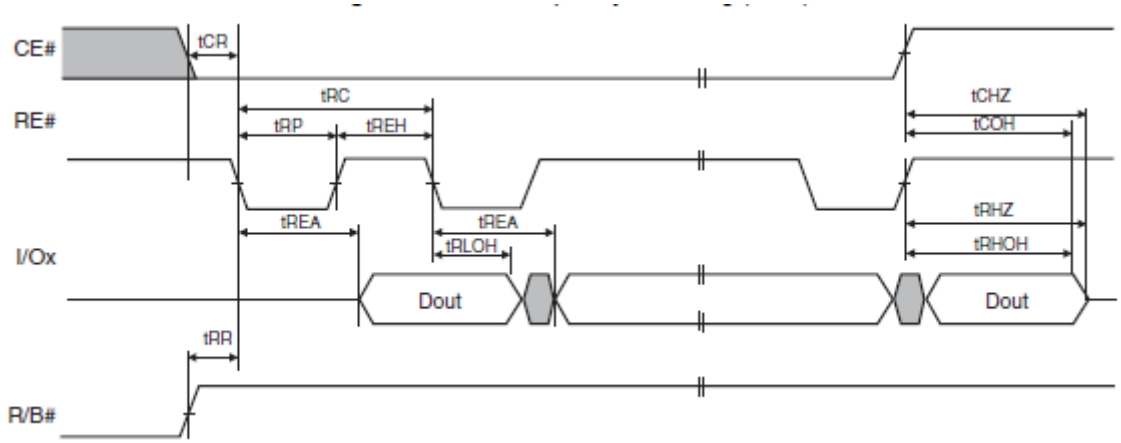
Figure 6.4 Data Output Cycle Timing



Notes:
1. Transition is measured at ± 200 mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. tRLOH is valid when frequency is higher than 33 MHz.
4. tRHOH starts to be valid when frequency is lower than 33 MHz.

6.5 Data Output Cycle Timing (EDO Type, CLE=L, WE#=H, ALE=L)

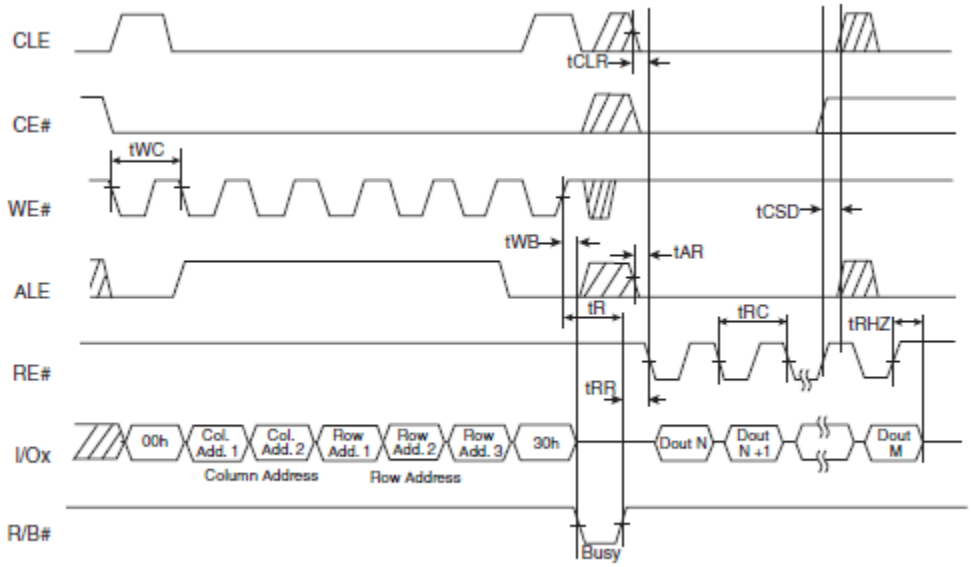
Figure 6.5 Data Output Cycle Timing (EDO)



Notes:
1. Transition is measured at ± 200 mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. tRLOH is valid when frequency is higher than 33 MHz.
4. tRHOH starts to be valid when frequency is lower than 33 MHz.

6.6 Page Read Operation

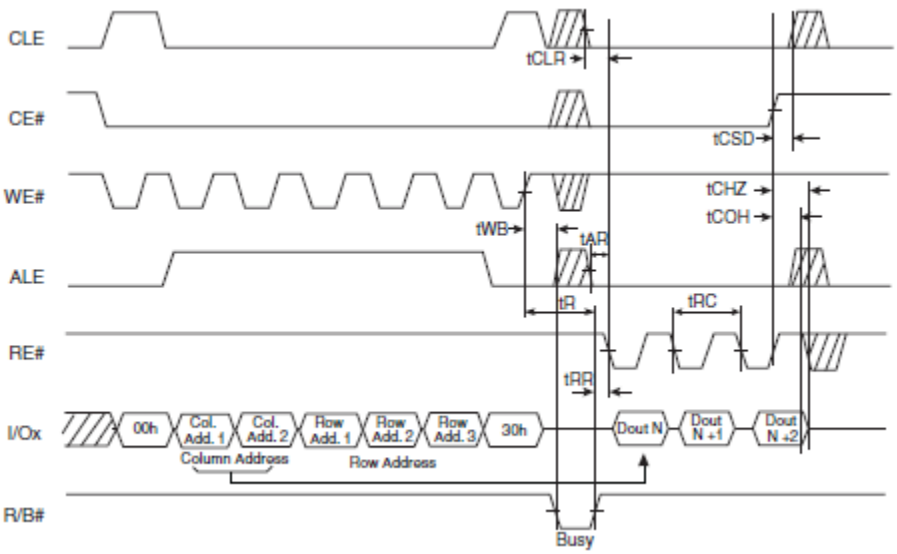
Figure 6.6 Page Read Operation (Read One Page)



Note:
1. If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.

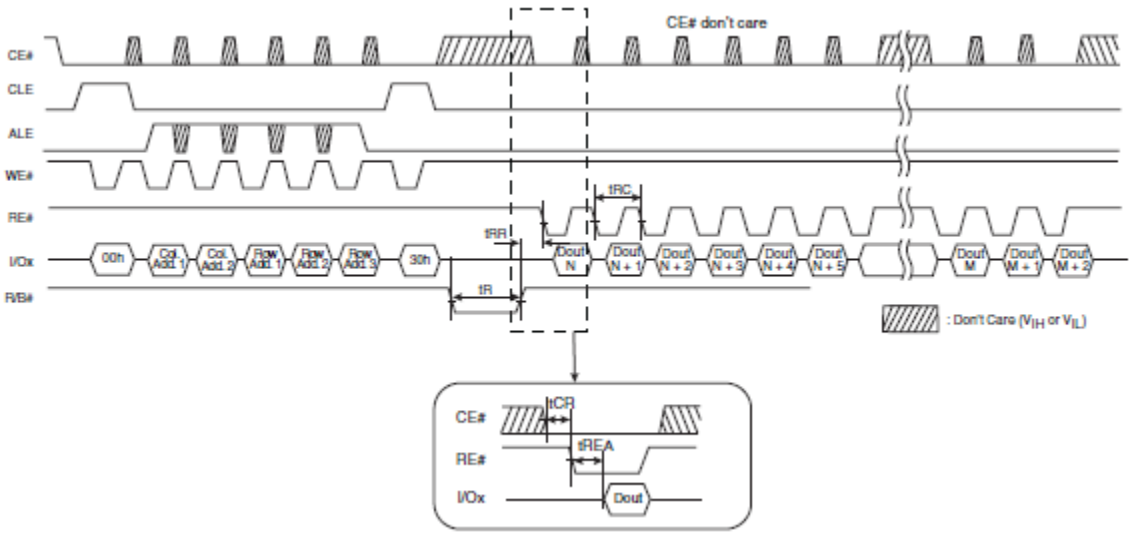
6.7 Page Read Operation (Intercepted by CE#)

Figure 6.7 Page Read Operation Intercepted by CE#



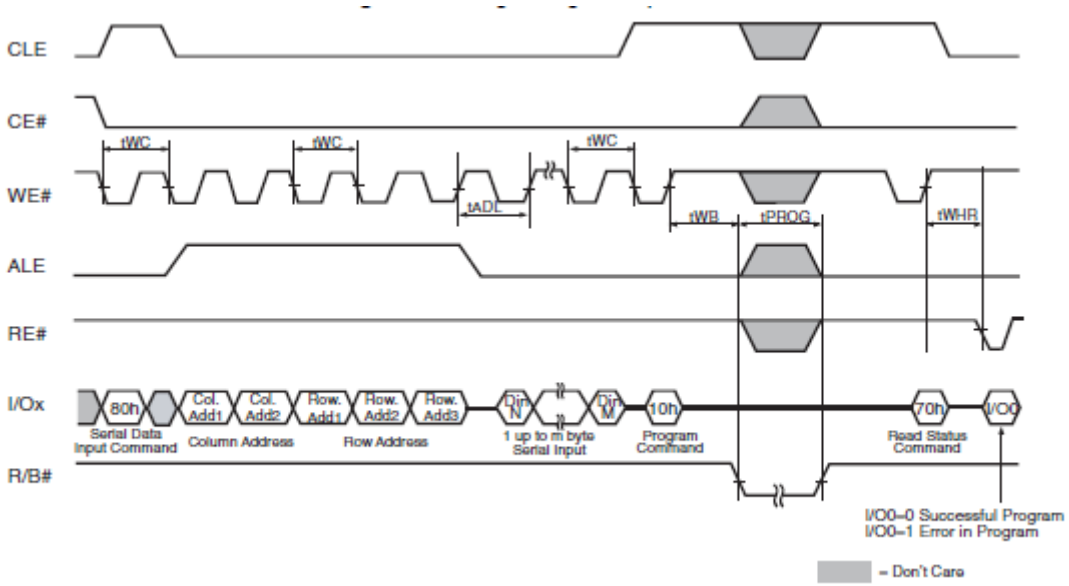
6.8 Page Read Operation Timing with CE# Don't Care

Figure 6.8 Page Read Operation Timing with CE# Don't Care



6.9 Page Program Operation

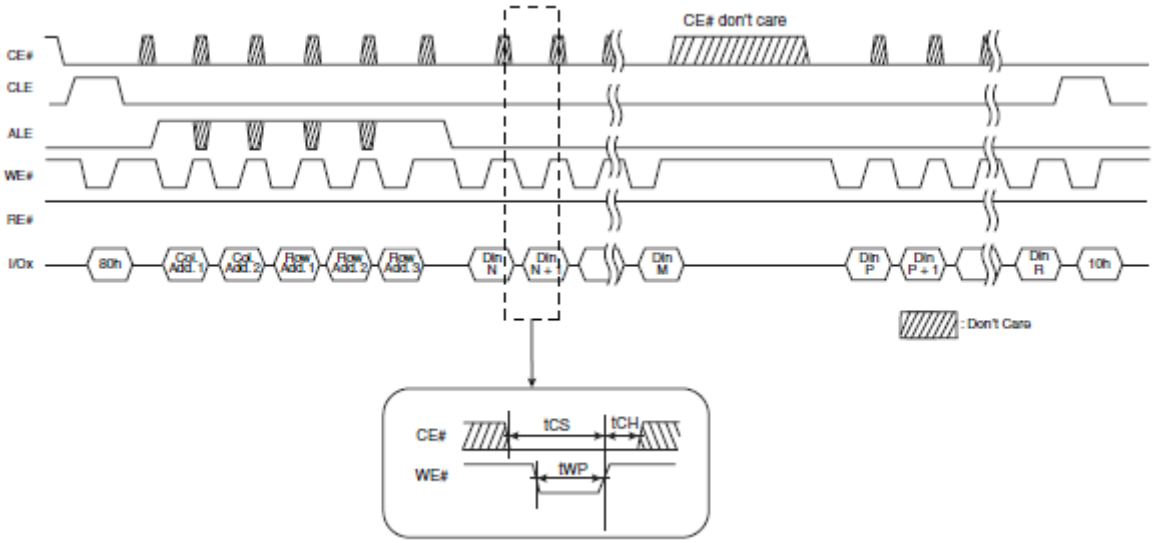
Figure 6.9 Page Program Operation



Note:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

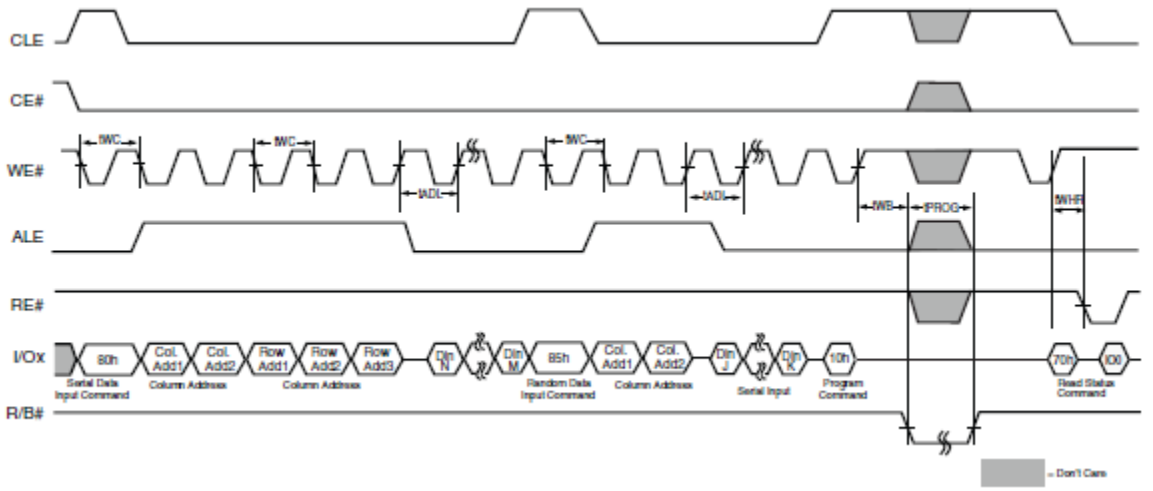
6.10 Page Program Operation Timing with CE# Don't Care

Figure 6.10 Page Program Operation Timing with CE# Don't Care



6.11 Page Program Operation with Random Data Input

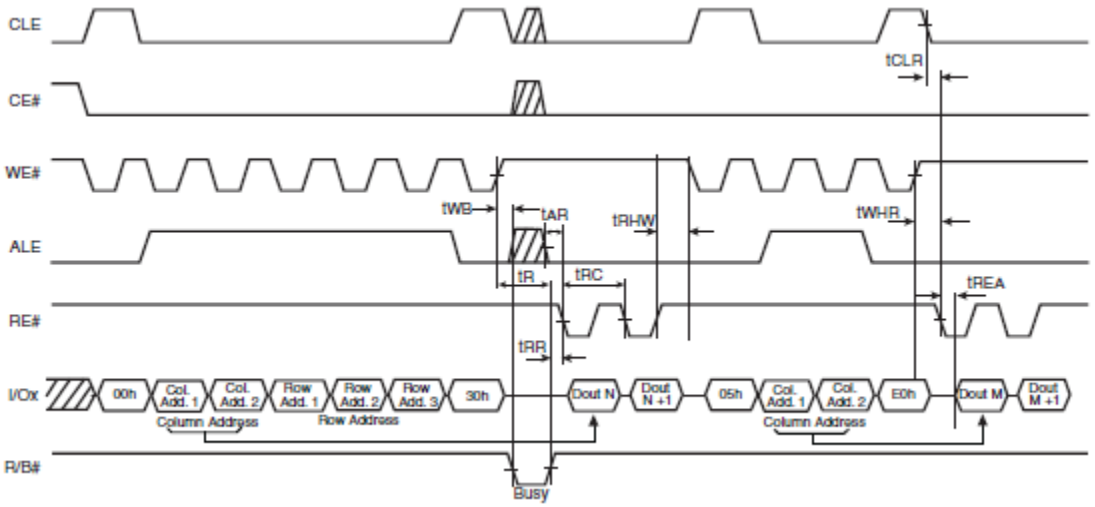
Figure 6.11 Random Data Input



Notes:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

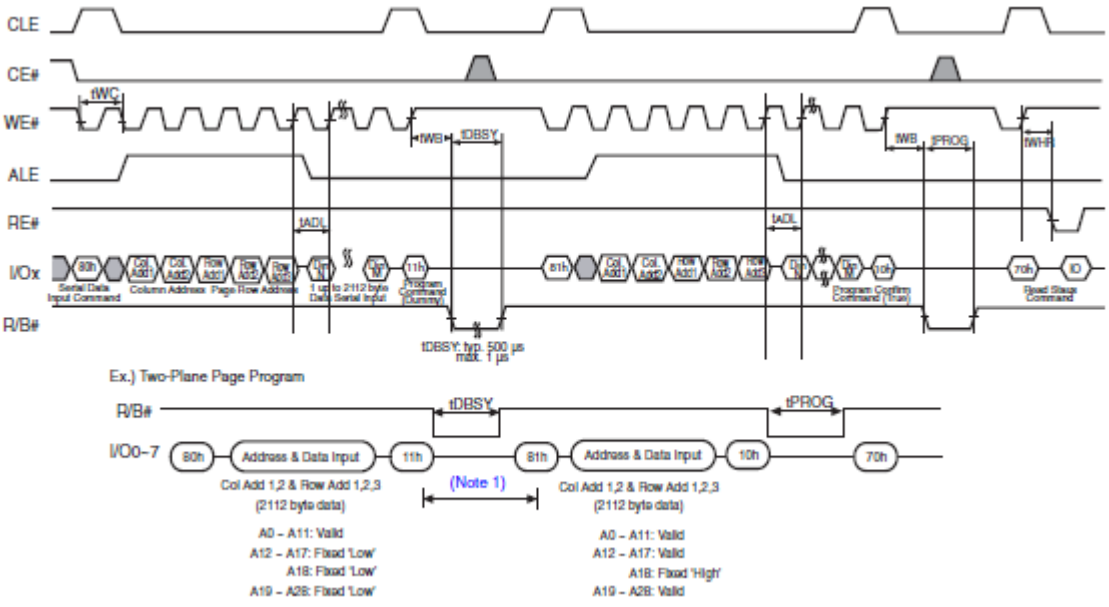
6.12 Random Data Output In a Page

Figure 6.12 Random Data Output



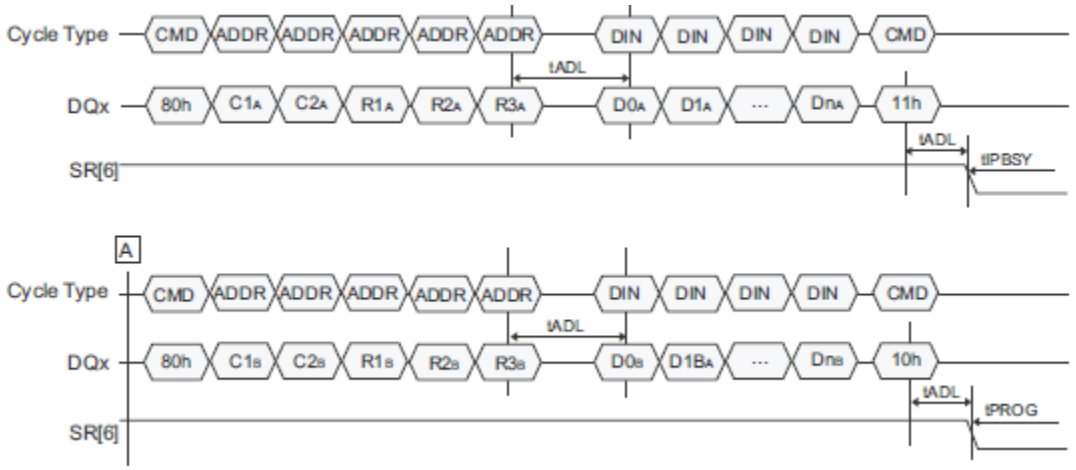
6.13 Multiplane Page Program Operation

Figure 6.13 Multiplane Page Program



Notes:
1. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
2. A18 is the plane address bit for x8 devices.

Figure 6.14 Multiplane Page Program (ONFI 1.0 Protocol)

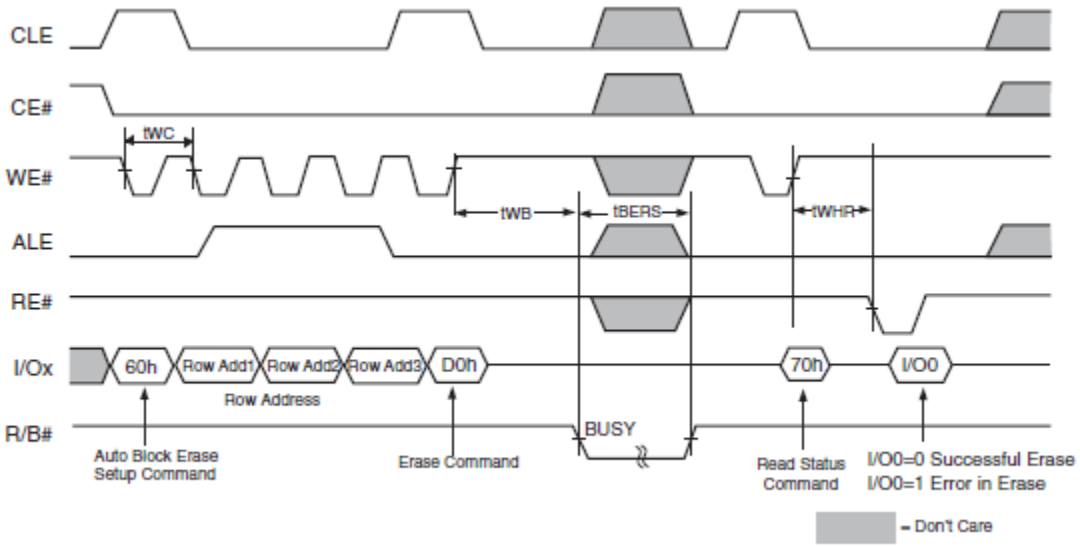


Notes:

1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. D0A-DnA Data to program for page A.
4. C1B-C2B Column address for page B. C1B is the least significant byte.
5. R1B-R3B Row address for page B. R1B is the least significant byte.
6. D0B-DnB Data to program for page B.
7. The block address bits must be the same except for the bit(s) that select the plane.

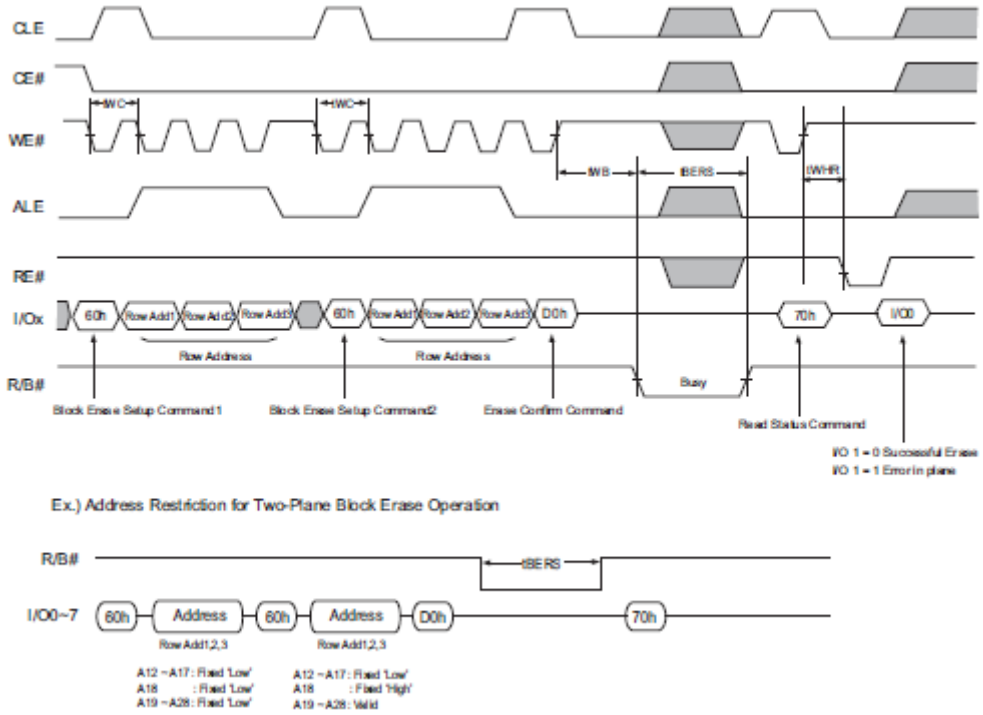
6.14 Block Erase Operation

Figure 6.15 Block Erase Operation (Erase One Block)



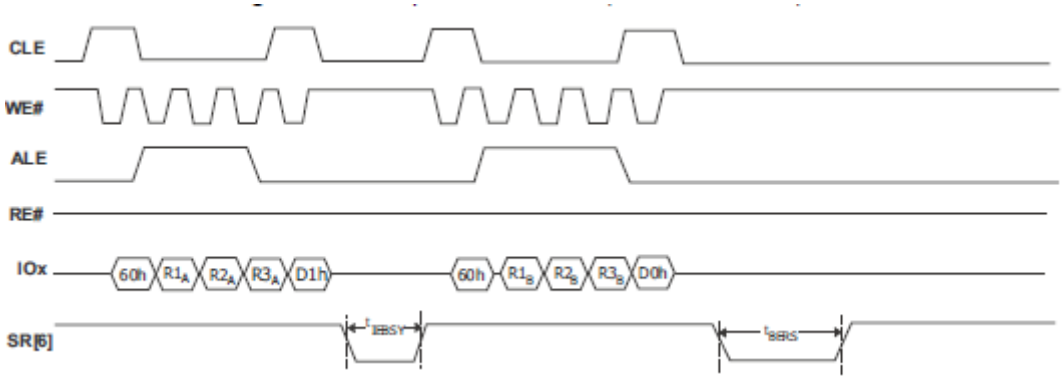
6.15 Multiplane Block Erase

Figure 6.16 Multiplane Block Erase



Note:
1. A18 is the plane address bit for x8 devices.

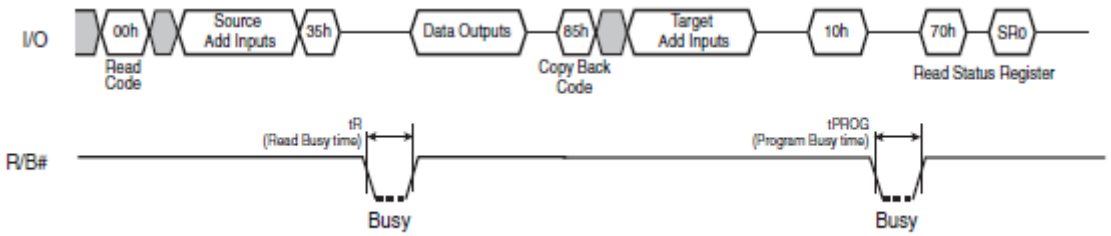
Figure 6.17 Multiplane Block Erase (ONFI 1.0 Protocol)



Notes:
1. R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
2. R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
3. The block address bits must be the same except for the bit(s) that select the plane.

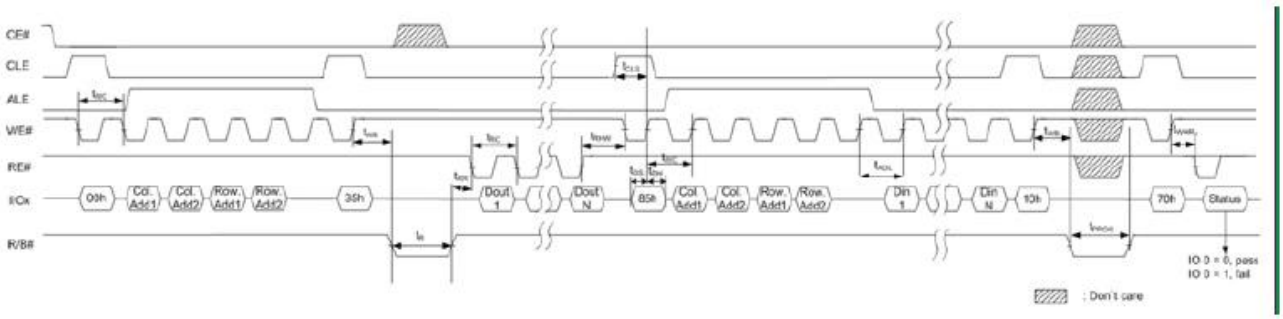
6.16 Copy Back Read with Optional Data Readout

Figure 6.18 Copy Back Read with Optional Data Readout



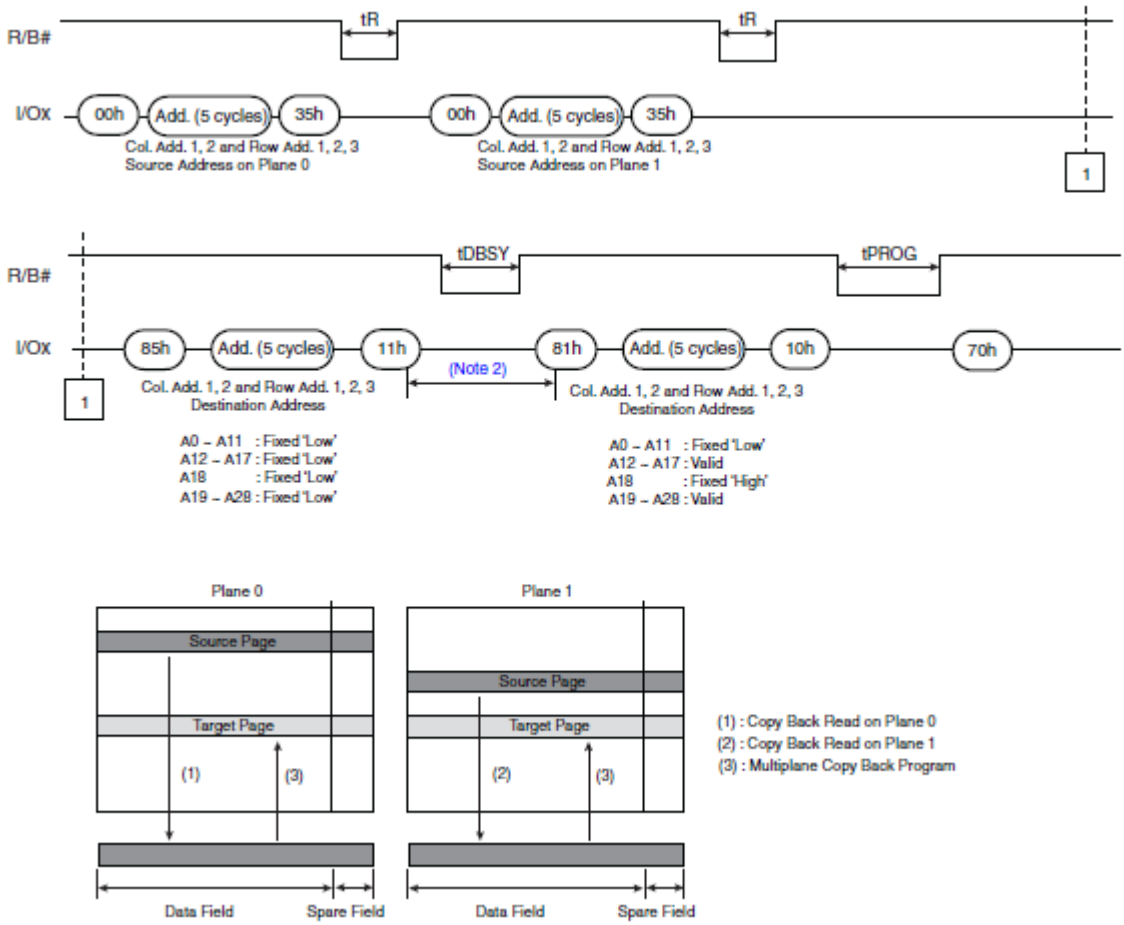
6.17 Copy Back Program Operation With Random Data Input

Figure 6.19 Copy Back Program with Random Data Input



6.18 Multiplane Copy Back Program

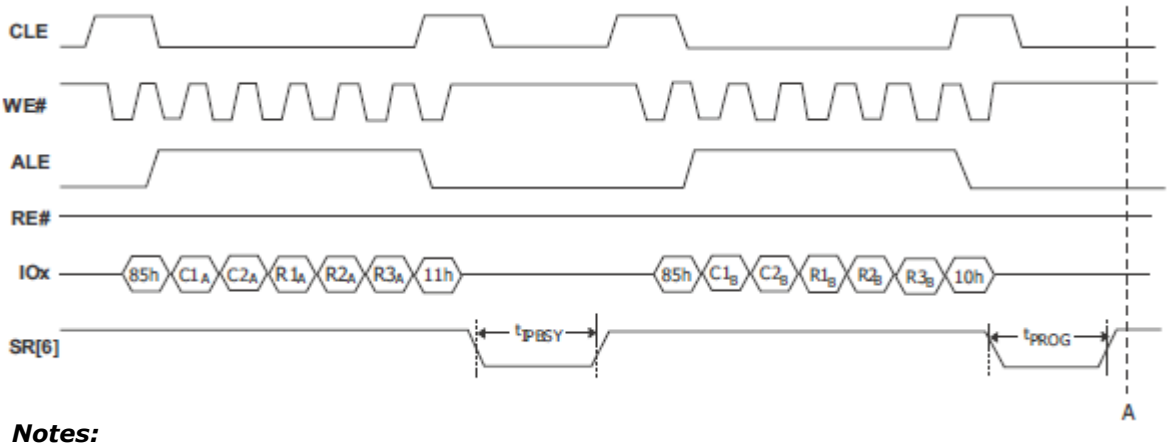
Figure 6.20 Multiplane Copy Back Program



Notes:

1. Copy Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
3. A18 is the plane address bit for x8 devices.

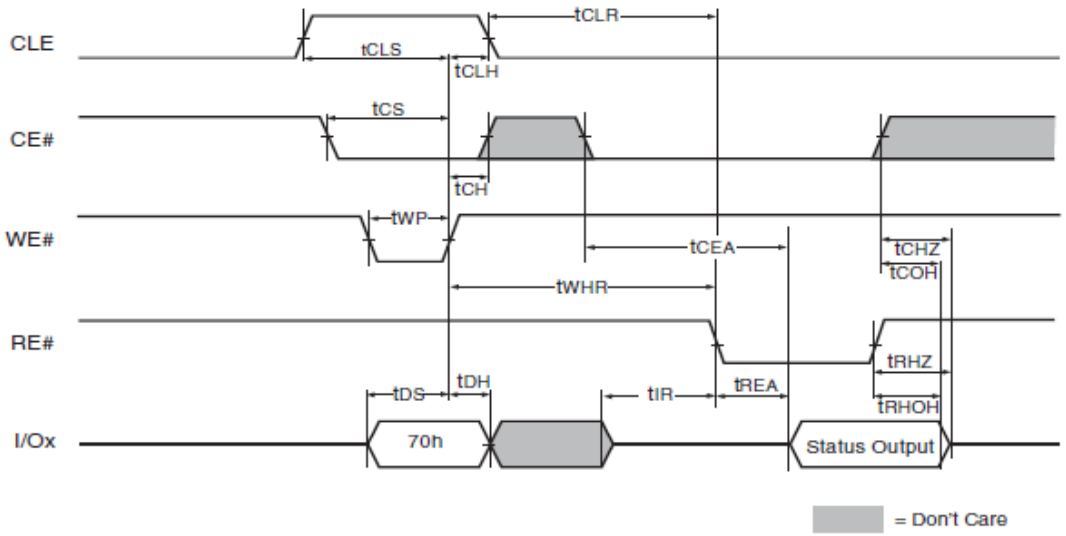
Figure 6.21 Multiplane Copy Back Program (ONFI 1.0 Protocol)



Notes:
1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. C1B-C2B Column address for page B. C1B is the least significant byte.
4. R1B-R3B Row address for page B. R1B is the least significant byte.
5. The block address bits must be the same except for the bit(s) that select the plane.

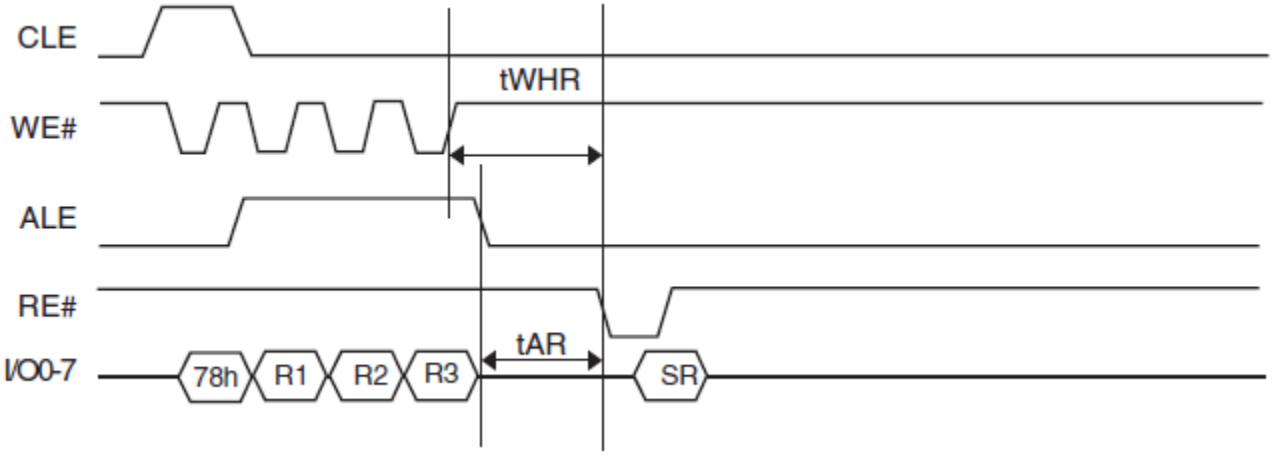
6.19 Read Status Register Timing

Figure 6.22 Status Read Cycle



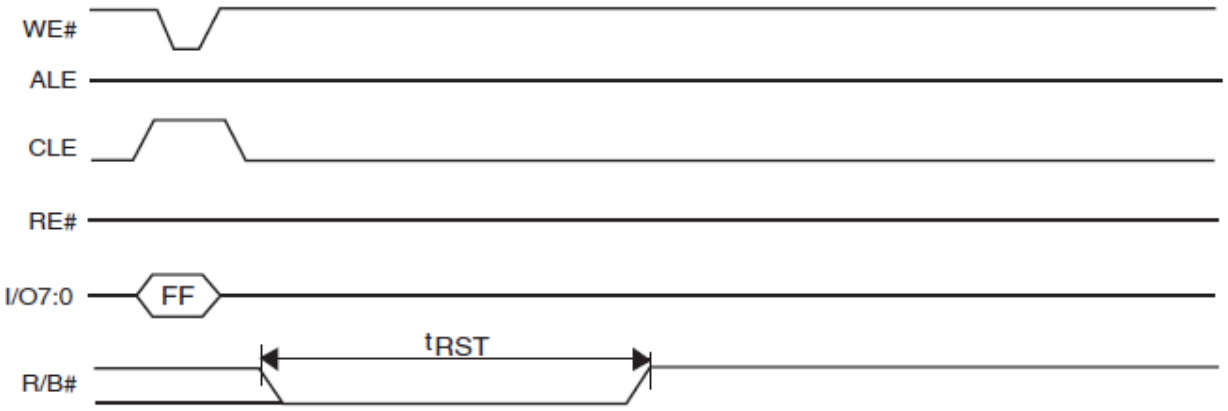
6.20 Read Status Enhanced Timing

Figure 6.23 Read Status Enhanced Cycle



6.21 Reset Operation Timing

Figure 6.24 Reset Operation Timing



6.22 Read Cache

Figure 6.25 Read Cache Operation Timing

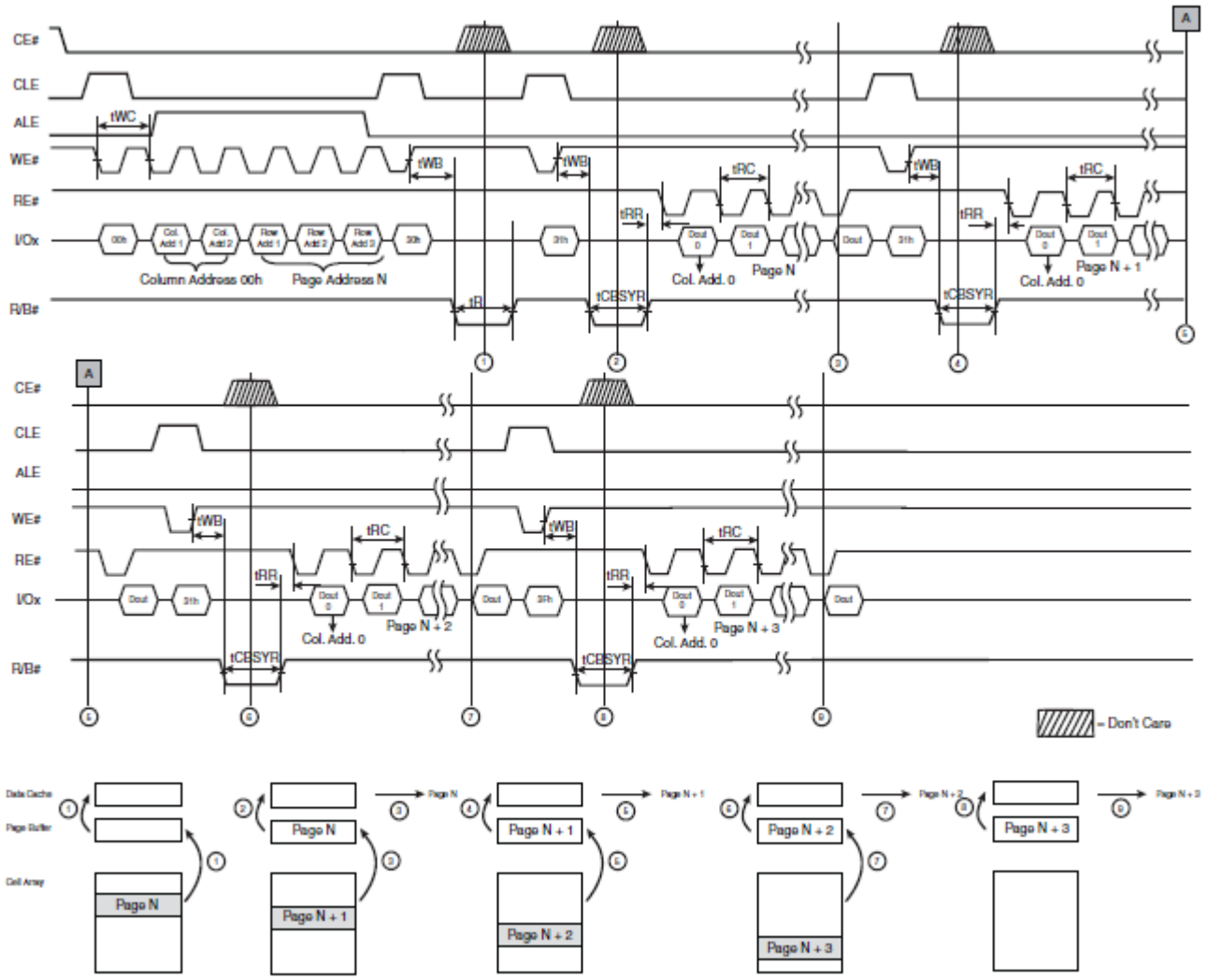


Figure 6.26 "Sequential" Read Cache Timing, Start (and Continuation) of Cache Operation

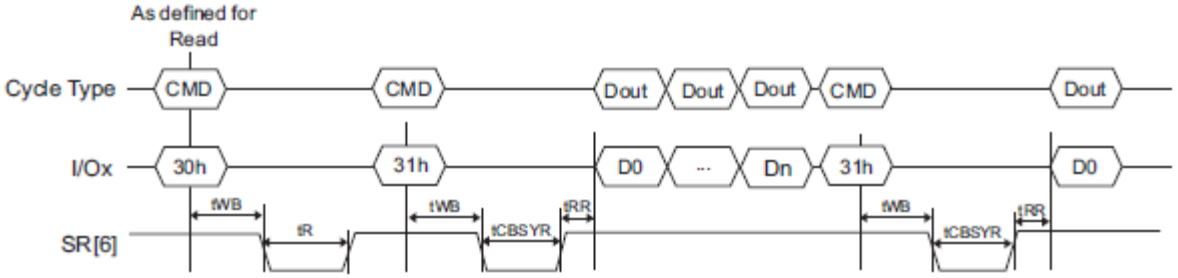


Figure 6.27 "Random" Read Cache Timing, Start (and Continuation) of Cache Operation

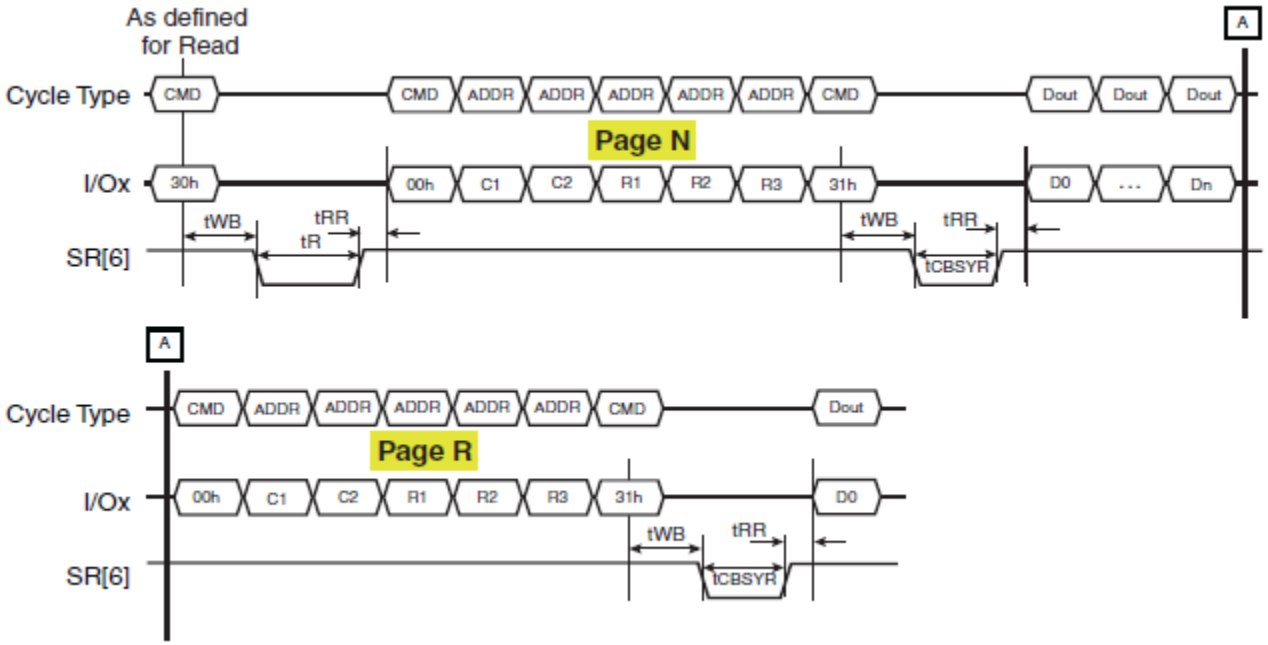
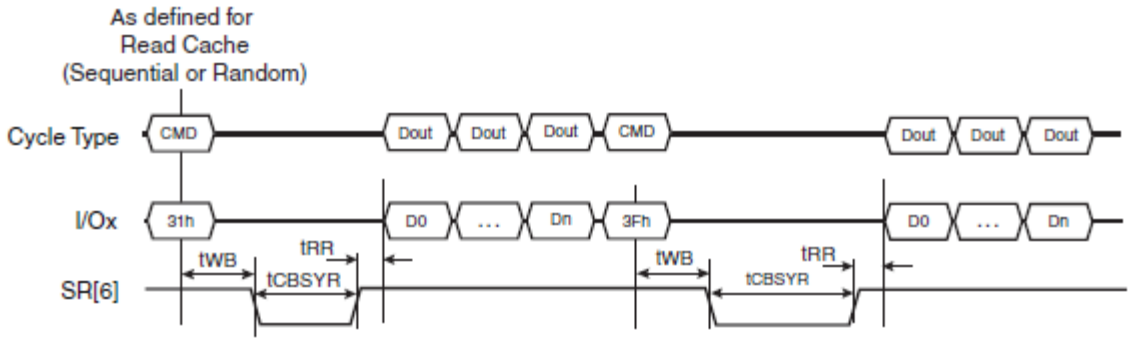
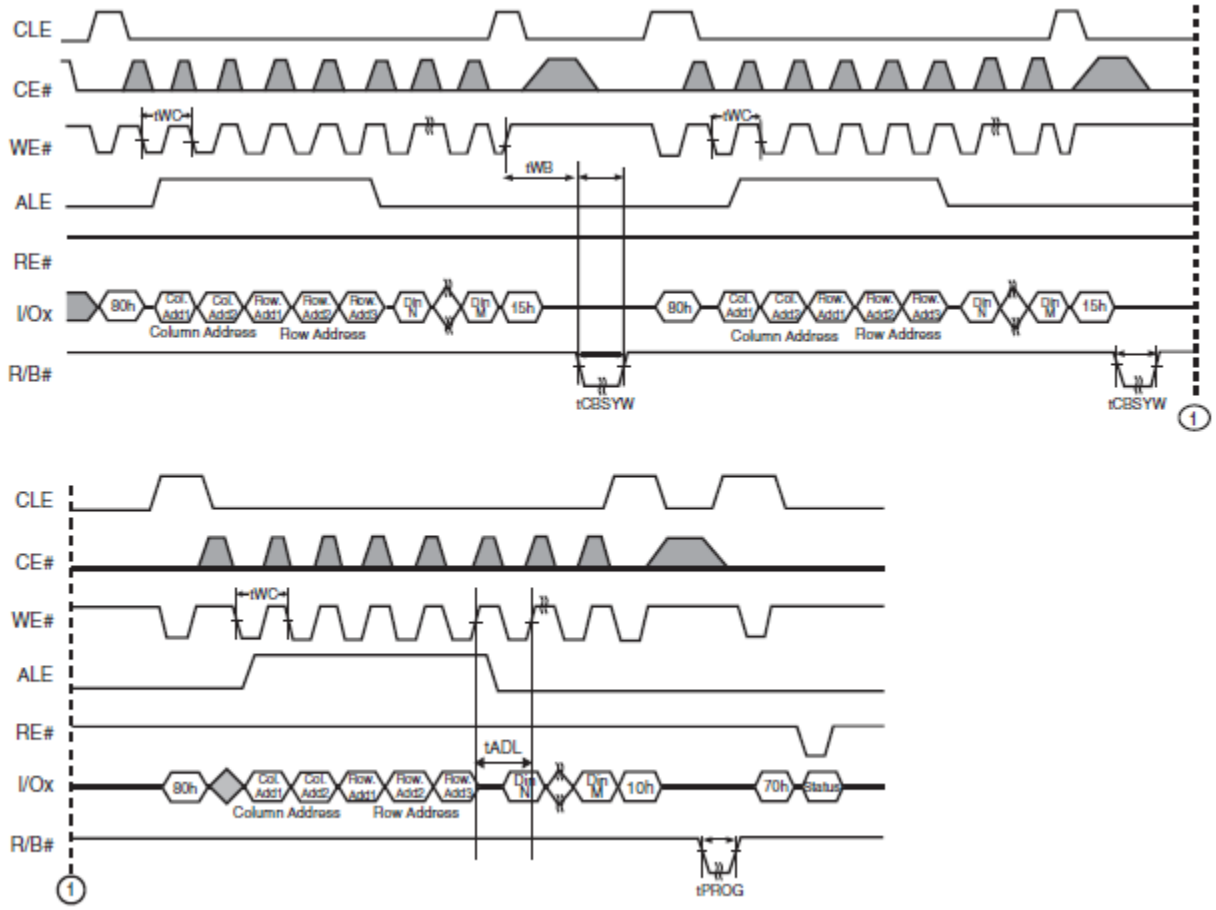


Figure 6.28 Read Cache Timing, End Of Cache Operation



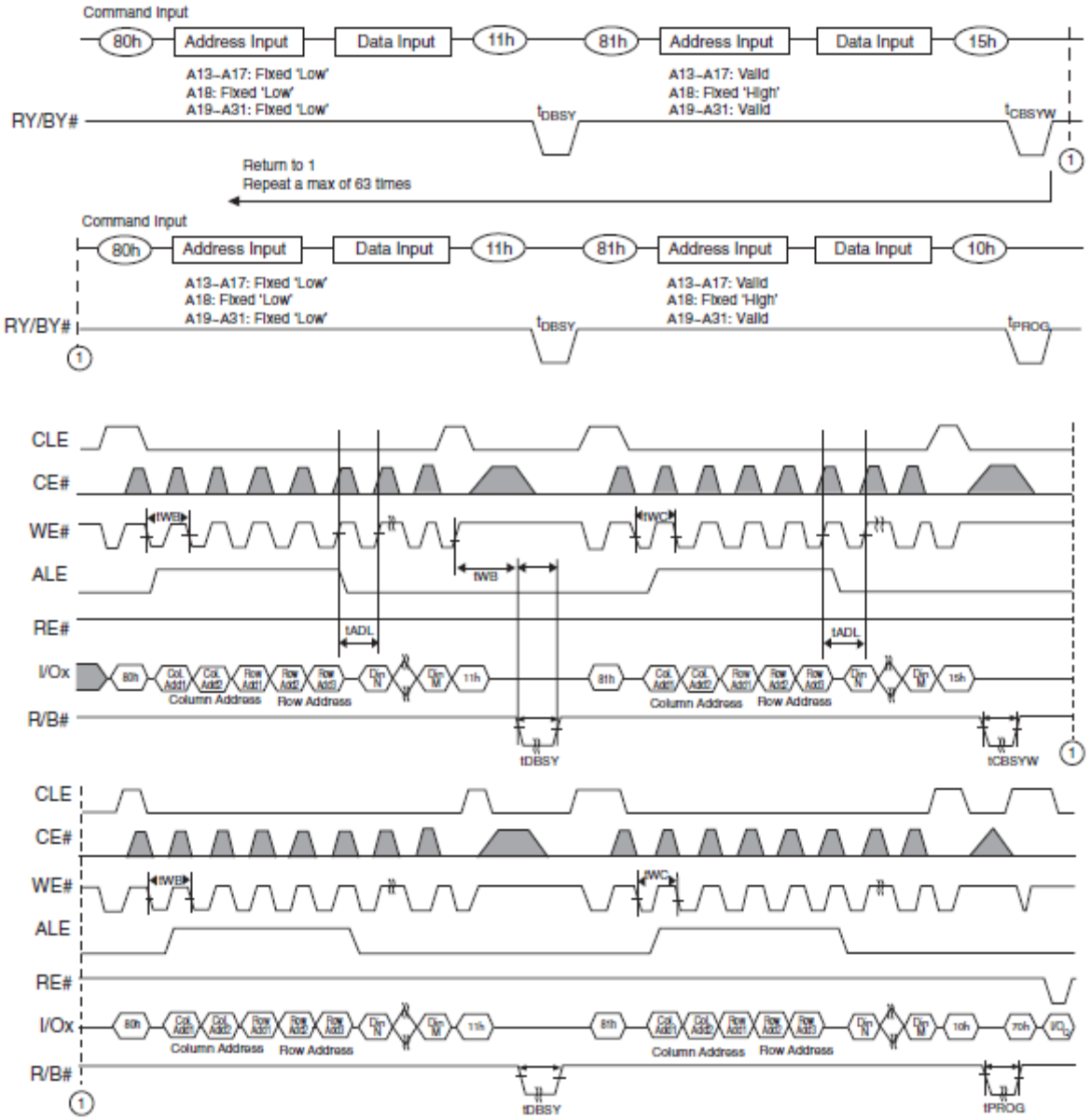
6.23 Cache Program

Figure 6.29 Cache Program



6.24 Multiplane Cache Program

Figure 6.30 Multiplane Cache Program

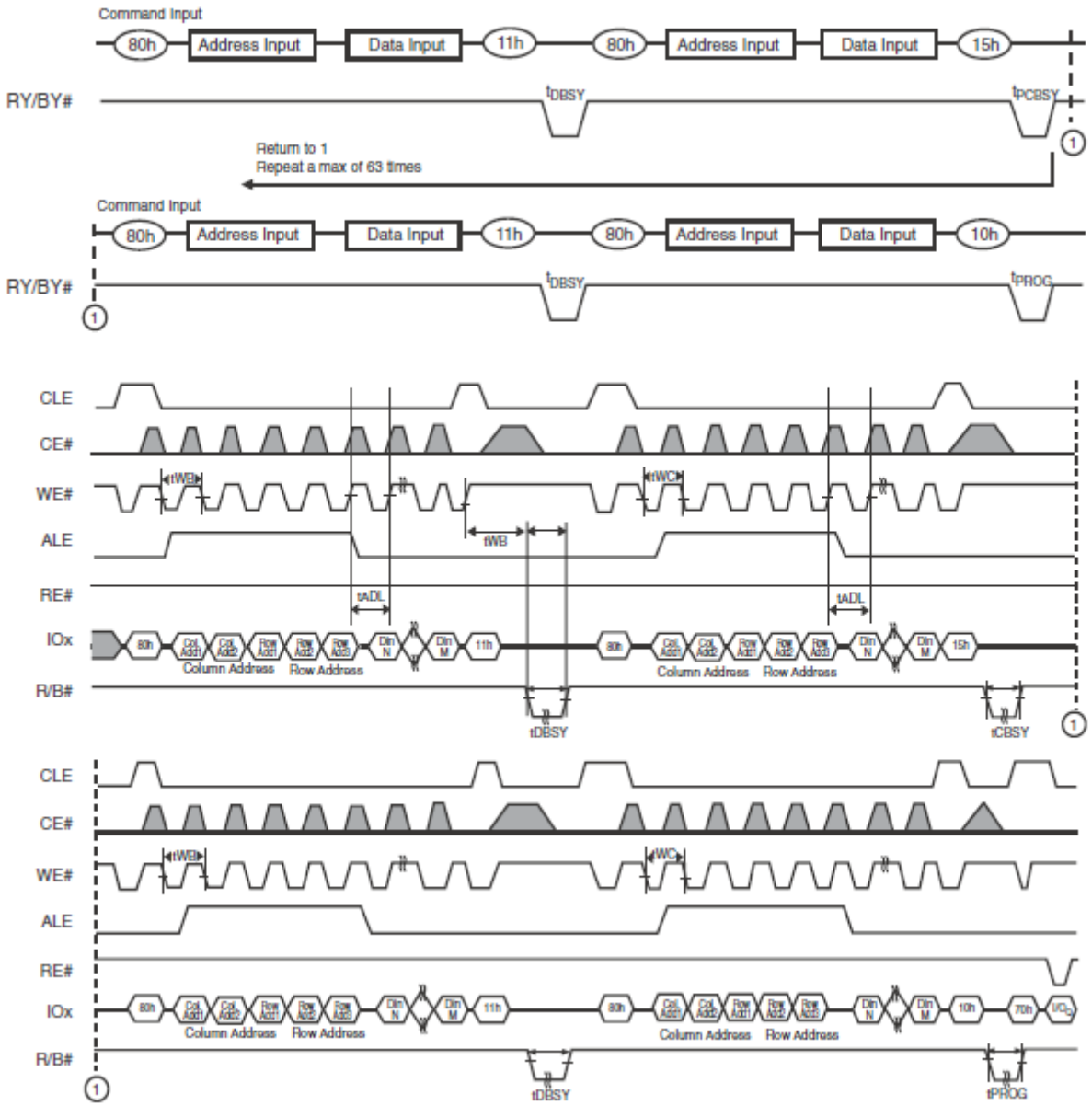


Notes:

1. Read Status Register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

2. A18 is the plane address bit for x8 devices.

Figure 6.31 Multiplane Cache Program (ONFI 1.0 Protocol)



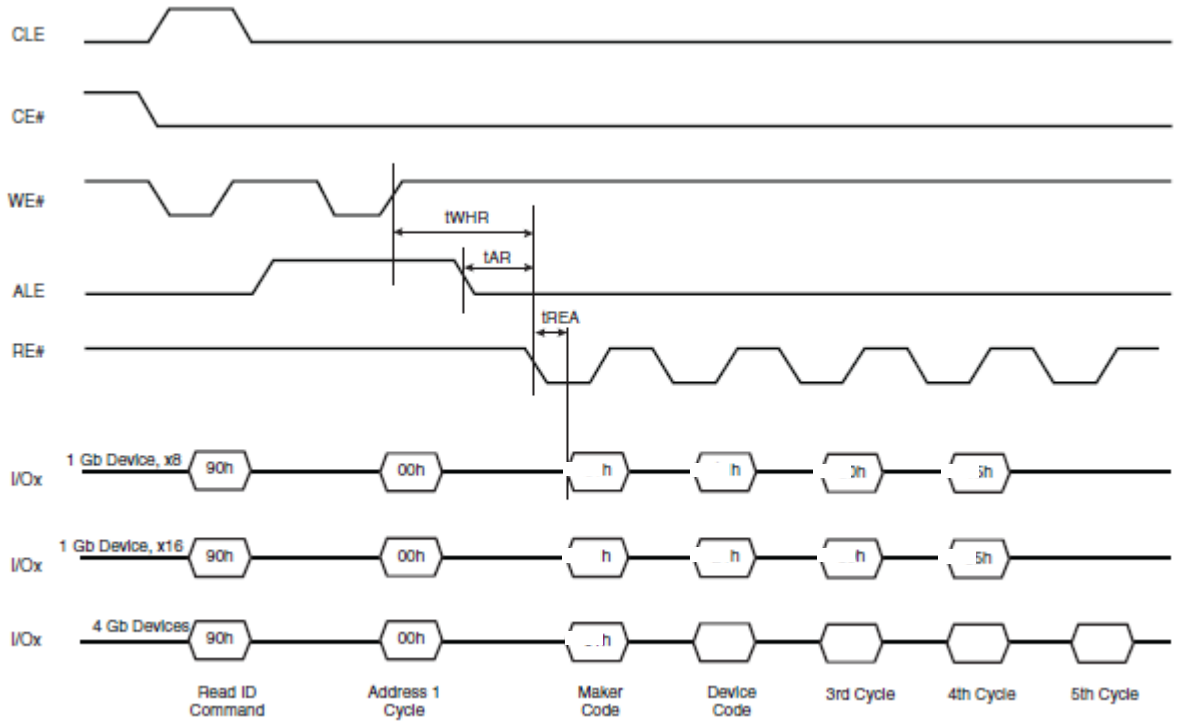
Notes:

1. The block address bits must be the same except for the bit(s) that select the plane.

2. Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

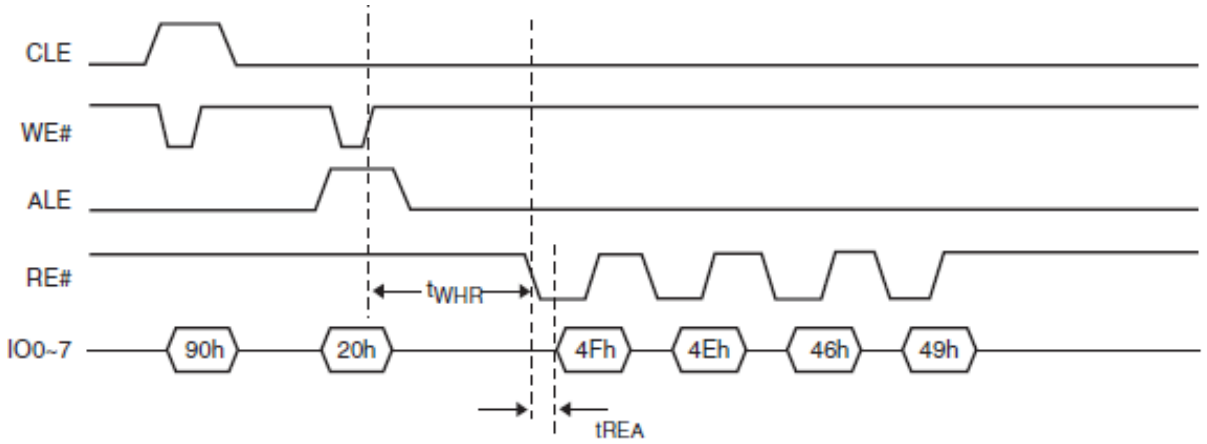
6.25 Read ID Operation Timing

Figure 6.32 Read ID Operation Timing



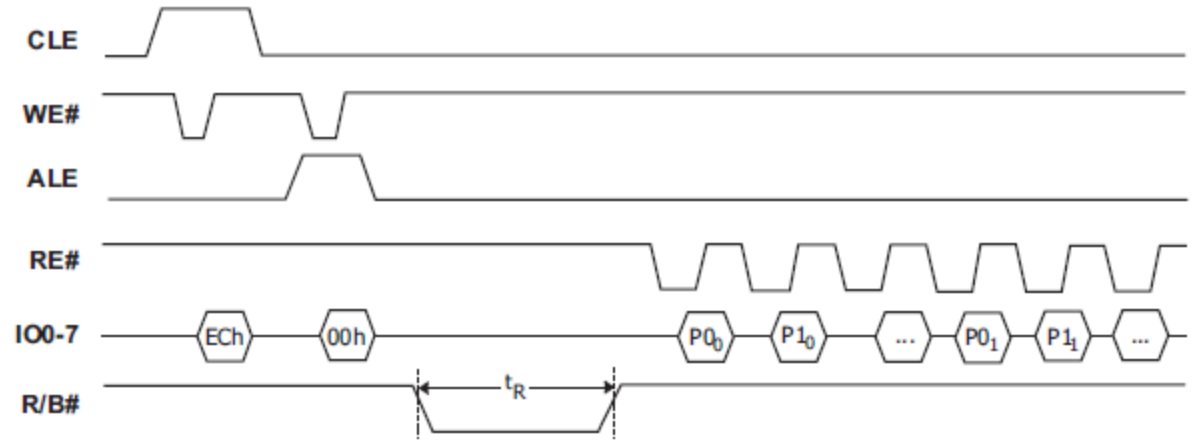
6.26 Read ONFI Signature Timing

Figure 6.33 ONFI Signature Timing



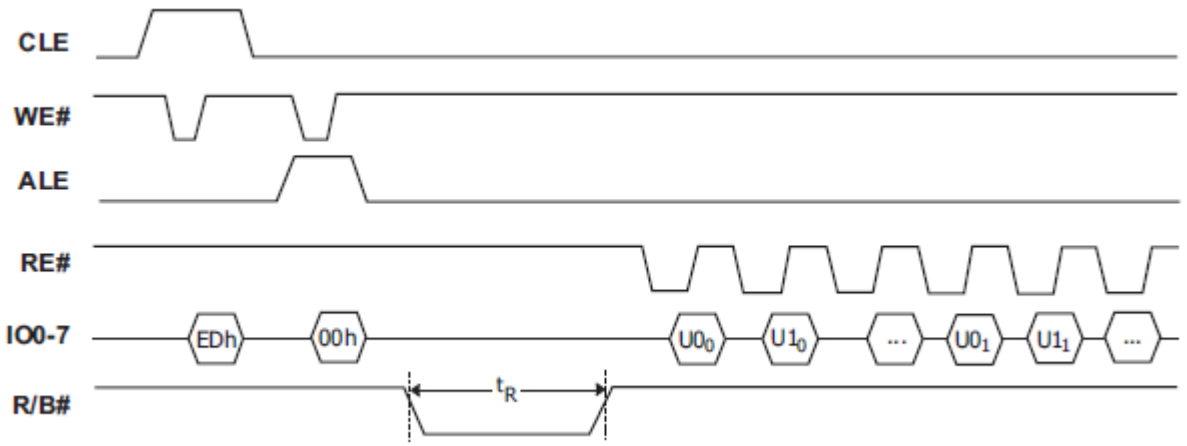
6.27 Read Parameter Page Timing

Figure 6.34 Read Parameter Page Timing



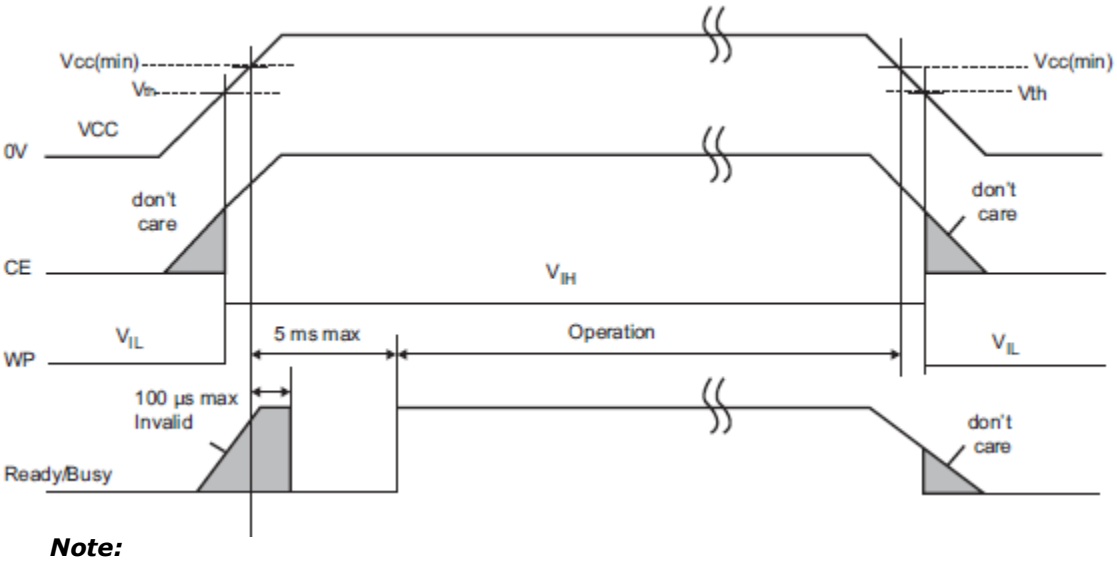
6.28 Read Unique ID Timing

Figure 6.35 Read Unique ID Timing



6.29 Power On and Data Protection Timing

Figure 6.36 Power On and Data Protection Timing



Note:

1. VTH = 1.2 volts.

6.30 WP# Handling

Figure 6.37 Program Enabling / Disabling Through WP# Handling

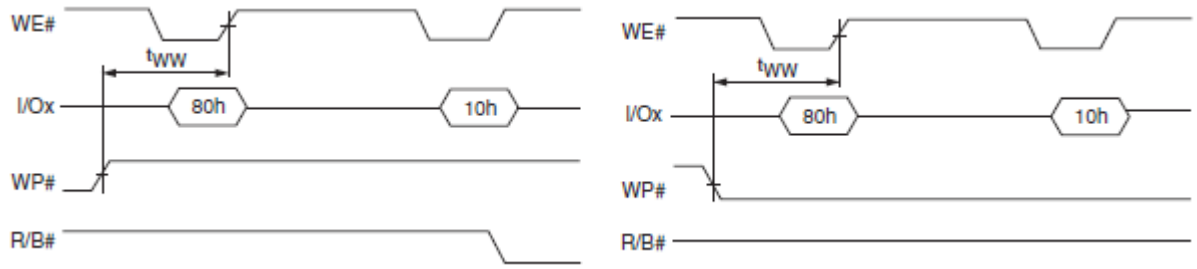
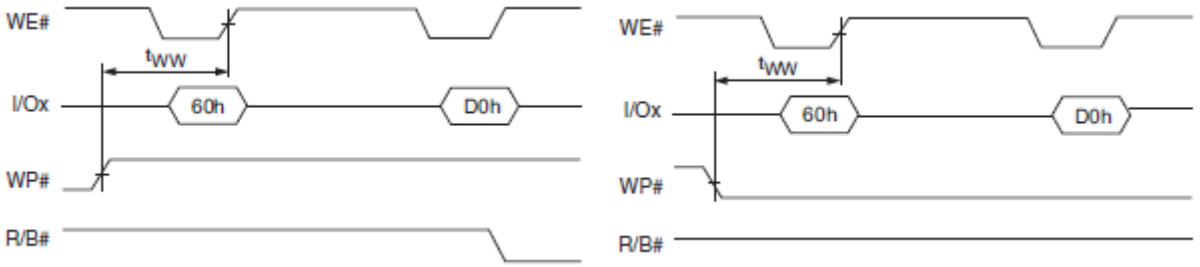


Figure 6.38 Erase Enabling / Disabling Through WP# Handling



7. System Interface

To simplify system interface, CE# may be unasserted during data loading or sequential data reading as shown in Figure 7.1. By operating in this way, it is possible to connect NAND flash to a microprocessor. Contrary to standard NAND, CE# don't care devices do not allow sequential read function.

Figure 7.1 Program Operation with CE# Don't Care

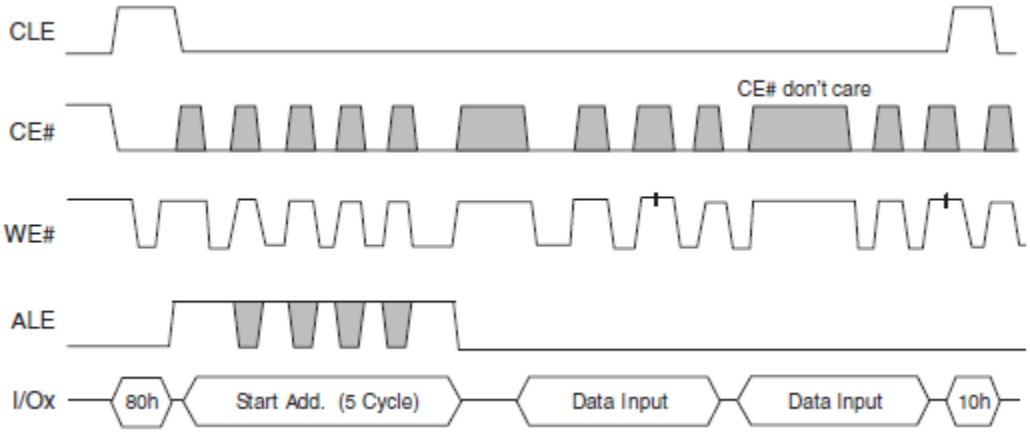


Figure 7.2 Read Operation with CE# Don't Care

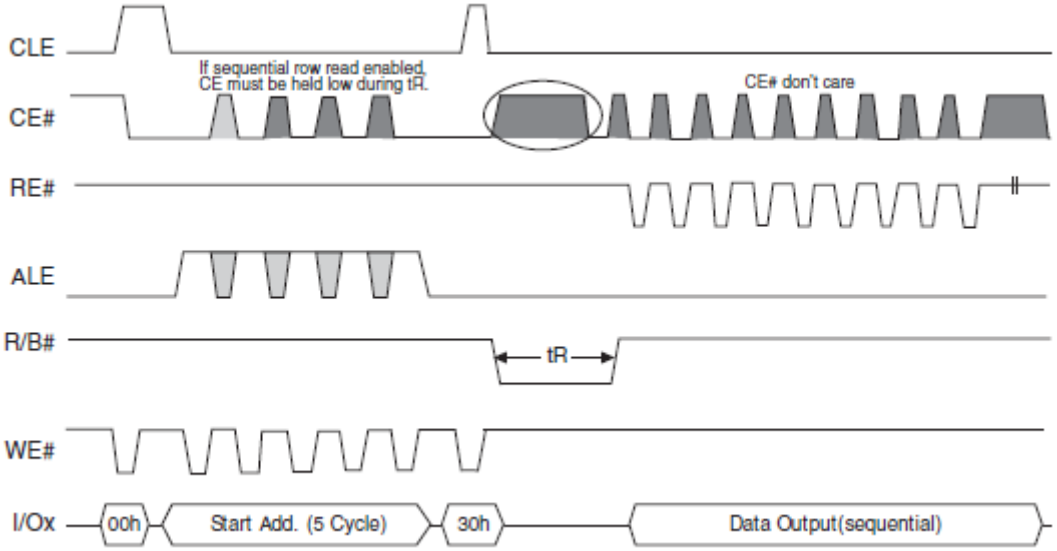
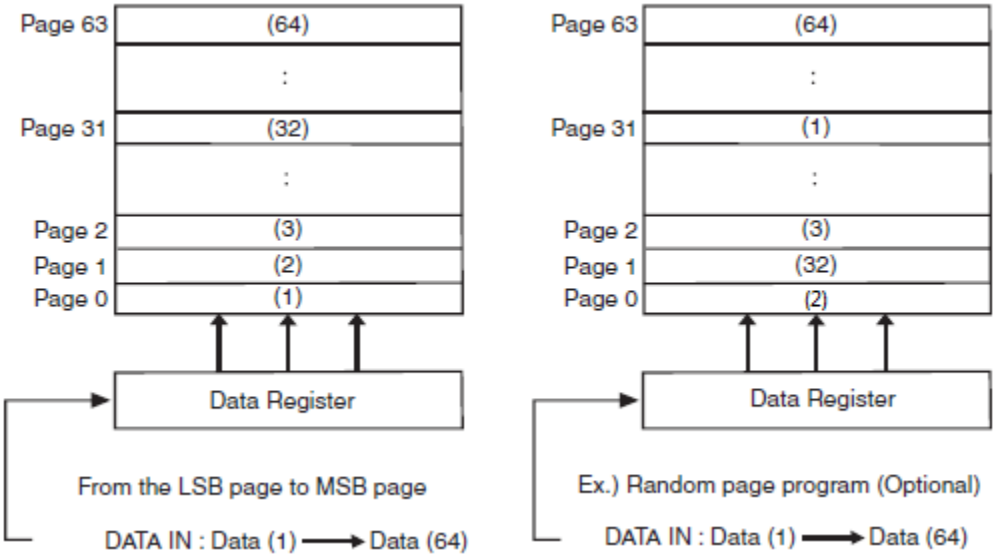


Figure 7.3 Page Programming Within a Block



8. Error Management

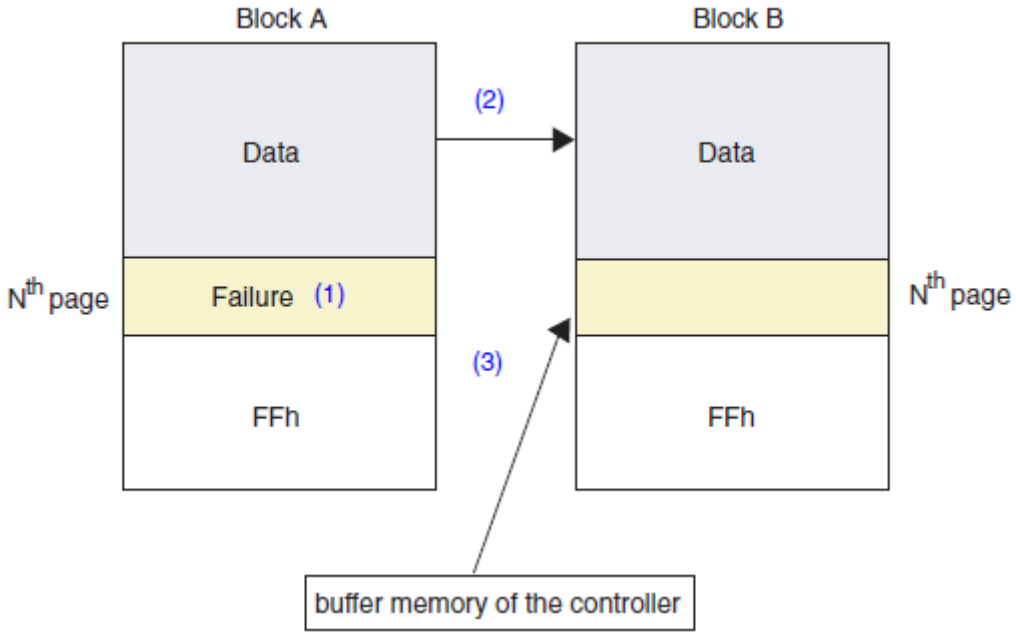
8.1 System Bad Block Replacement

Over the lifetime of the device, additional Bad Blocks may develop. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional Bad Blocks can be identified whenever a program or erase operation reports "Fail" in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 8.1 and Figure 8.1 for the recommended procedure to follow if an error occurs during an operation.

Table 8.1 Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (4bit / 512 + 16 byte)

Figure 8.1 Bad Block Replacement

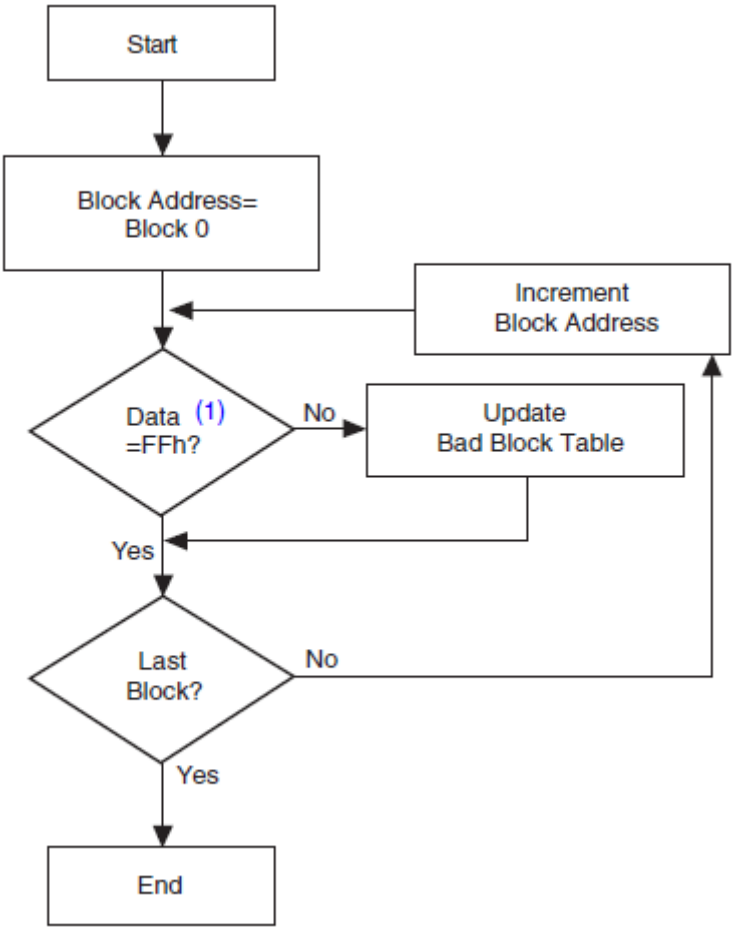


Notes:
1. An error occurs on the Nth page of Block A during a program operation.
2. Data in Block A is copied to the same location in Block B, which is a valid block.
3. The Nth page of block A, which is in controller buffer memory, is copied into the Nth page of Block B.
4. Bad block table should be updated to prevent from erasing or programming Block A.

8.2 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st byte in the spare area of the 1st or 2nd page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page will indicate a bad block. The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure 8.2. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Figure 8.2 Bad Block Management Flowchart



Note:

1. Check for FFh at the 1st byte in the spare area of the 1st, 2nd pages.