JSL24Gxx8WA-SU : 4Gb (x32), 2Gb 2stack LPDDR2 SDRAM

KEY FEATURE

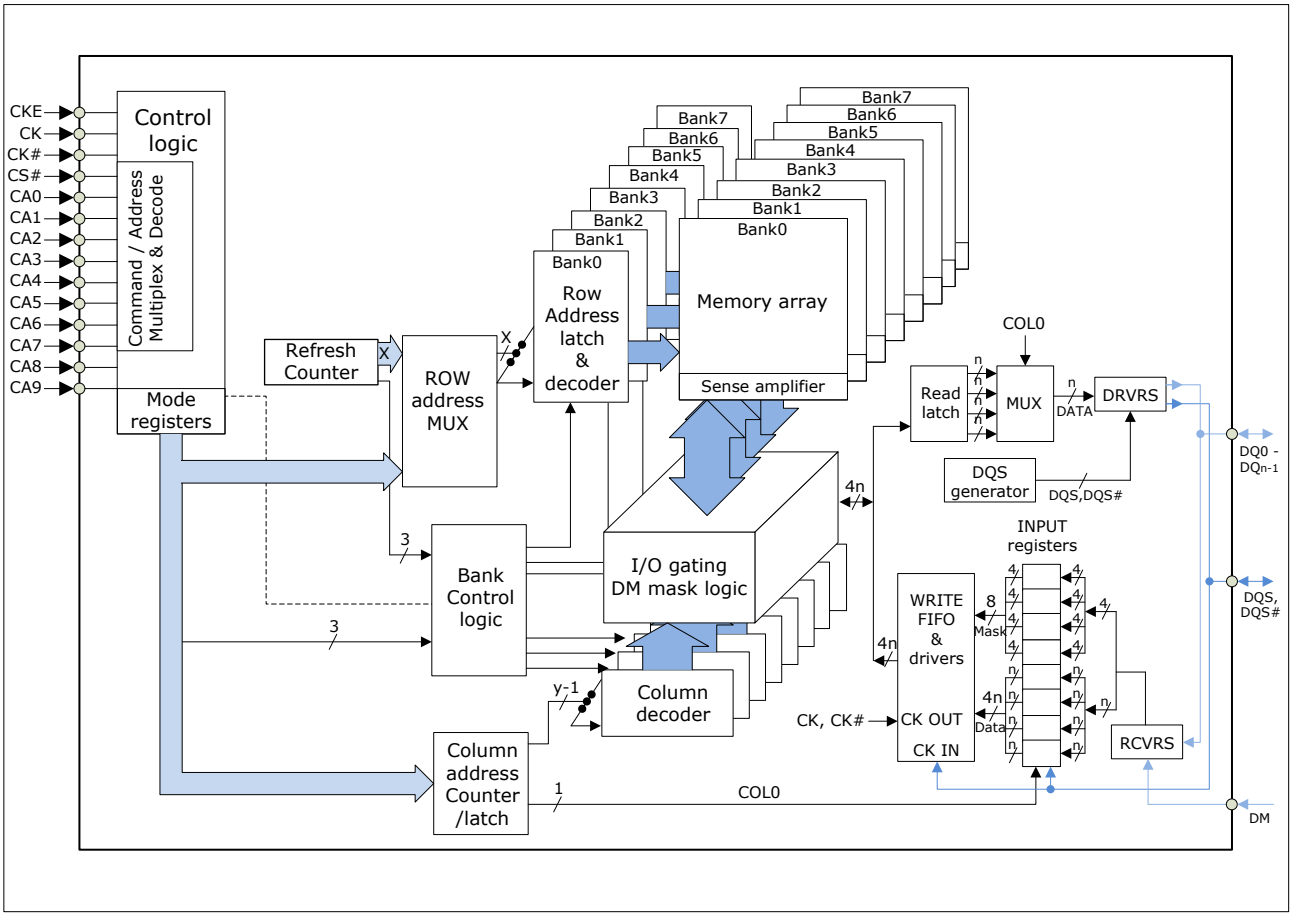
- 4Gb (2Gb 2stack)
- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS / DQS#), these are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK / CK#)
- Differential data strobes (DQS / DQS#)
- Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 4 (default), 8 or 16
- Burst Type: Sequential or Interleave
- Read & Write latency: Refer to Table 51 LPDDR2 AC Timing Table
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- HSUL_12 compatible inputs
- VDD1/VDD2/VDDQ
  : 1.8V/1.2V/1.2V/1.2V
- No DLL: CK to DQS is not synchronized
- Edge aligned data output, center aligned data input
- Operating Temperature: -25 to 85°C (Commercial)
  -40 to 85°C (Industrial)
  85 to 105°C (Extended)
- Auto refresh duty cycle: 3.9us

Speed Grade	Clock Rate [MHz]	Data Rate (Mb/s/pin)	RL	WL
-25A	533	1066	8	4
-25	400	800	6	3

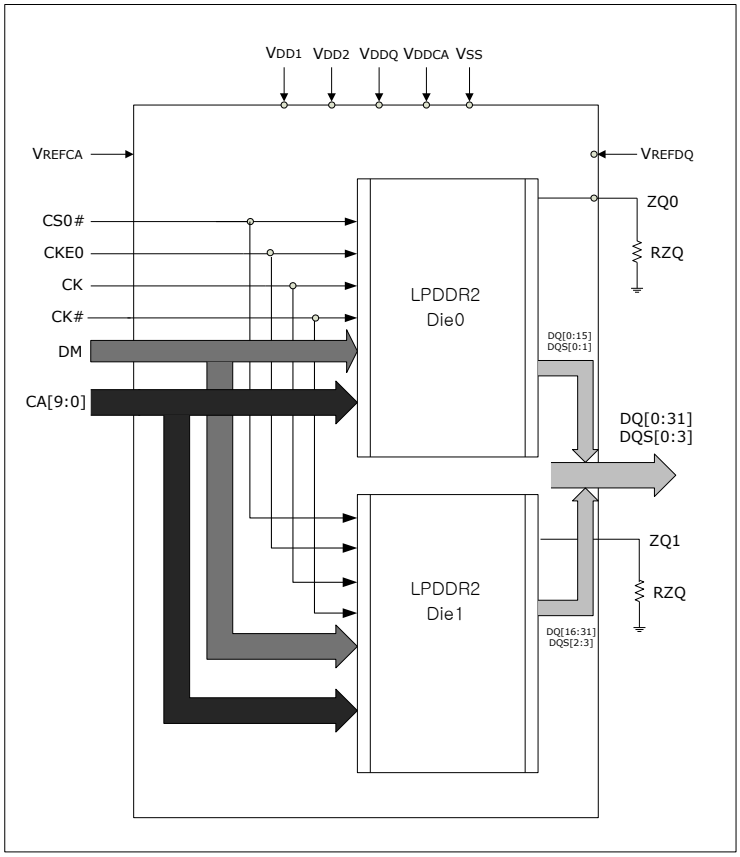
[ORDERING INFORMATION]

PNM	Density	Interface	PKG	Option	Speed	Grade
JSL24G328WABQ-D25-SU	4Gb (2Gb 2stack)	x32	10*11.5* 1.0T	1CS,2ZQ	400MHz	Industrial
JSL24G328WABQ-D25A-SU					533MHz	Industrial
JSL24G328WABQ-D25M-SU					400MHz	AT
JSL24G328WABQ-D25AM-SU					533MHz	AT

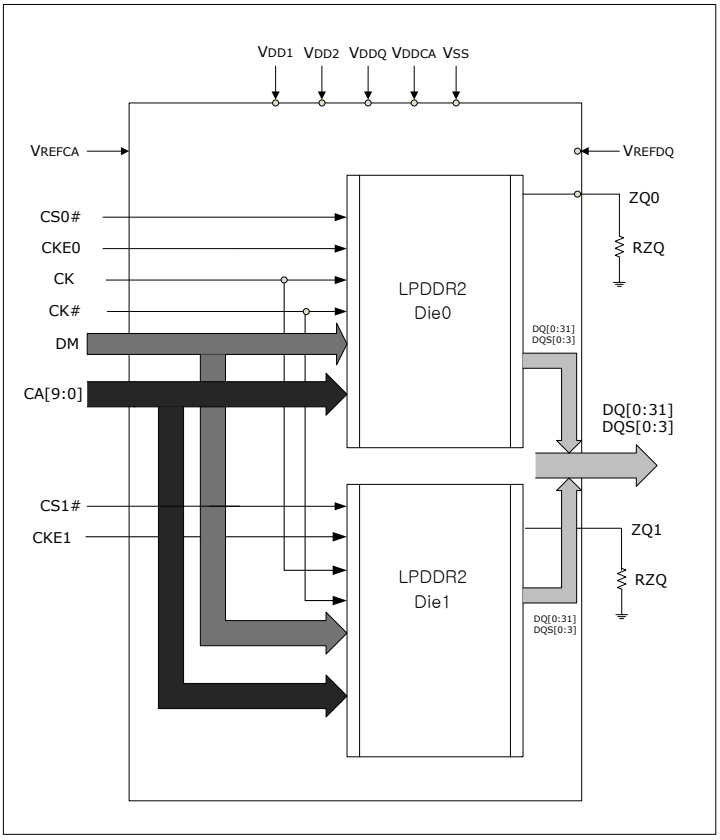
1. Functional Block Diagrams



[2Gb/4Gb Blcok Diagram]



[4Gb (2Gb 2stack,1CS 2ZQ)Block Diagram]



[4Gb (2Gb 2stack, 2CS) BIcok Diagram]

2. Ball Descriptions

2.1 Pad Definition and Description

Name	Type	Description
CK, CK#	Input	**Clock**: CK and CK# are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CS# and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and CK#. The positive Clock edge is defined by the crosspoint of a rising CK and a falling CK#. The negative Clock edge is defined by the crosspoint of a falling CK and a rising CK#.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS#	Input	**Chip Select:** CS# is considered part of the command code. See Command Truth Table for command code descriptions. CS# is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ31 (x32)	I/O	**Data Inputs/Outputs**: Bi-directional data bus
DQS0 - DQS3, DQS0# - DQS3# (x32)	I/O	**Data Strobes (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x32 DQS0 and DQS0# correspond to the data on DQ0 - DQ7, DQS1 and DQS1# to the data on DQ8 - DQ15, DQS2 and DQS2# to the data on DQ16 - DQ23, DQS3 and DQS3# to the data on DQ24 - DQ31.
DM0 - DM3 (x32)	Input	**Input Data Mask:** For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS#). DM0 is the input data mask signal for the data on DQ0-7. For x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1:** Core power supply
VDD2	Supply	**Core Power Supply 2:** Core power supply **Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS#, CK, and CK# input buffers.
VDDQ	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
VREF(CA)	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS#, CK, and CK# input buffers.
VREF(DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE : Data includes DQ and DM

LPDDR2 SDRAM Addressing

ITEM		4Gb(2Gb 2stack)
Number of banks		8
Bank address pins		BA0~BA2
Auto precharge pin		A10/AP
X32	Row addresses	R0-R13
	Column addresses	C0-C9
	tREFI(μs)	3.9

NOTE 1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
NOTE 2. tREFI values for all bank refresh is Tc = -25~85℃, Tc means Operating Case Temperature.
NOTE 3. Row and Column Address values on the CA bus that are not used are “don’t care.”

3. Functional Description

LPDDR2 is a high-speed SDRAM device internally configured as a 8-Bank memory.

These devices contain the following number of bits:

2 Gb has 2,147,483,648 bits (4Gb : 2Gb 2stack)

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access. Prior to normal operation, the LPDDR2 must be initialized.

3.1 Simplified LPDDR2 Bus Interface State Diagram

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see “LPDDR2 Command Definitions and Timing Diagrams”

Simplified LPDDR2 Bus Interface State Diagram

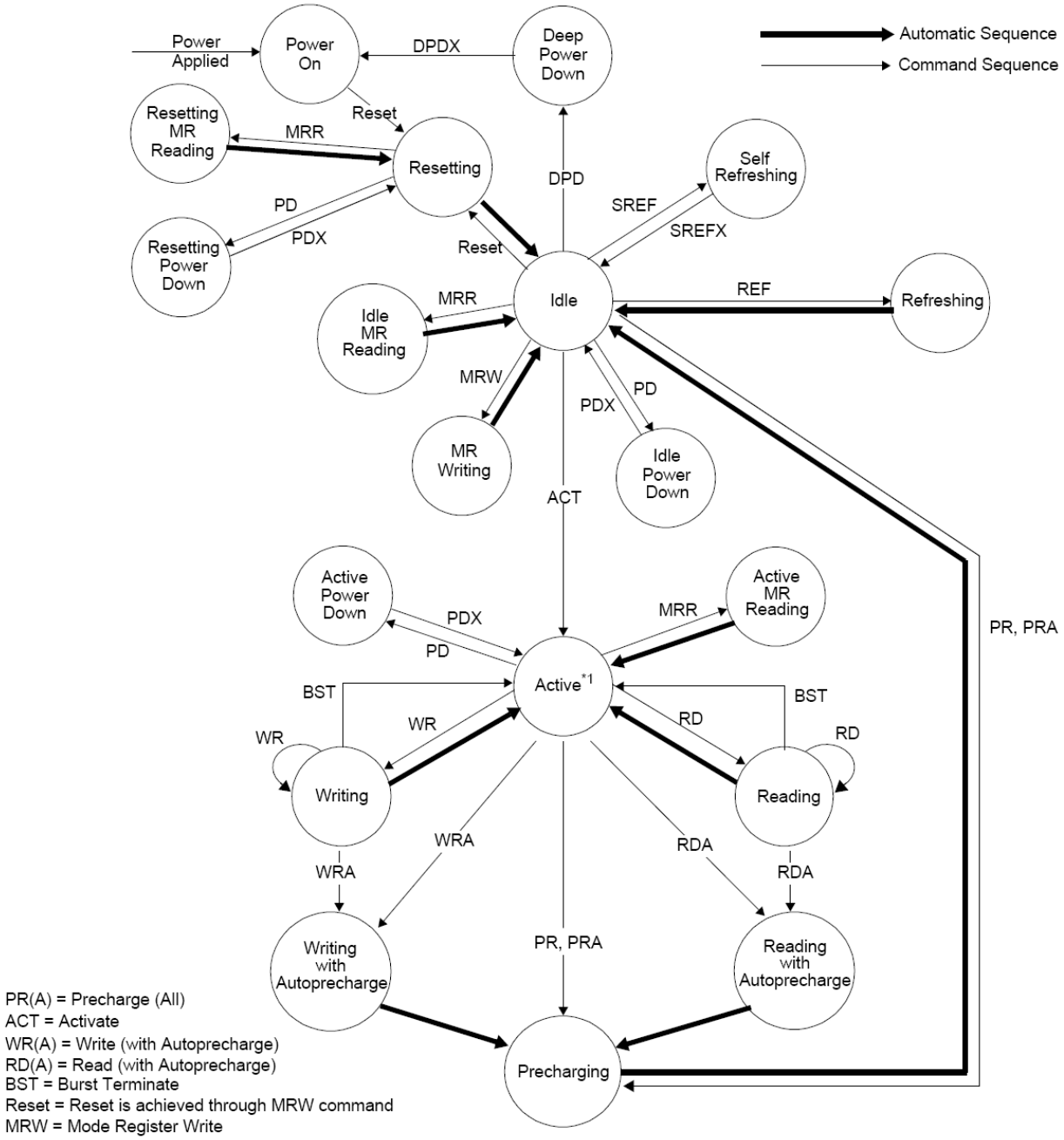


Figure 3.1 LPDDR2 : Simplified Bus Interface State Diagram

NOTE 1. For LPDDR2-SDRAM in the Idle state, all banks are precharged.

3.2 Power-up, Initialization, and Power-Off

LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation

3.2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=< 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.
On or before the completion of the power ramp (Tb) CKE must be held low.
DQ, DM, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDD2 during voltage ramp to avoid latch-up.
The following conditions apply:
Ta is the point where *any* power supply first reaches 300 mV.
After Ta is reached, VDD1 must be greater than VDD2 - 200 mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDD2 - 200 mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
After Ta is reached, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.
The above conditions apply between Ta and power-off (controlled or uncontrolled).
Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.
Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.
NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

2. CKE and clock:

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS# and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 ns to 100 ns), if any Mode Register Reads are performed.
Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 us. (Td).

3. Reset command:

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least t_{INIT4} = 1us while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.
Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see “Powerdown”).
The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.
As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.
After the DAI-bit (MR0, “DAI”) is set to zero “DAI complete” by the memory device, the device is in idle state (**Tf**). The state of the DAI status bit can be determined by an MRR command to MR0.

All SDRAM devices will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.
After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration:
After tINIT5 (**Tf**), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For LPDDR2 devices which do not support the ZQ Calibration command, this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:
After tZQINIT (**Tg**), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.
The LPDDR2 device will now be in IDLE state and ready for any valid command.
After **Tg**, the clock frequency may be changed according to the clock frequency change procedure described in section “Input clock stop and frequency change” of this specification.

Table 1 – Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	ms	Maximum Power Ramp Time
tINIT1	100		ns	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		us	Minimum Idle time after first CKE assertion
tINIT4	1		us	Minimum Idle time after Reset command
tINIT5		10	us	Maximum duration of Device Auto-Initialization
tZQINIT	1		us	ZQ Initial Calibration for LPDDR2-S4 devices
tCKb	18	100	ns	Clock cycle time during boot

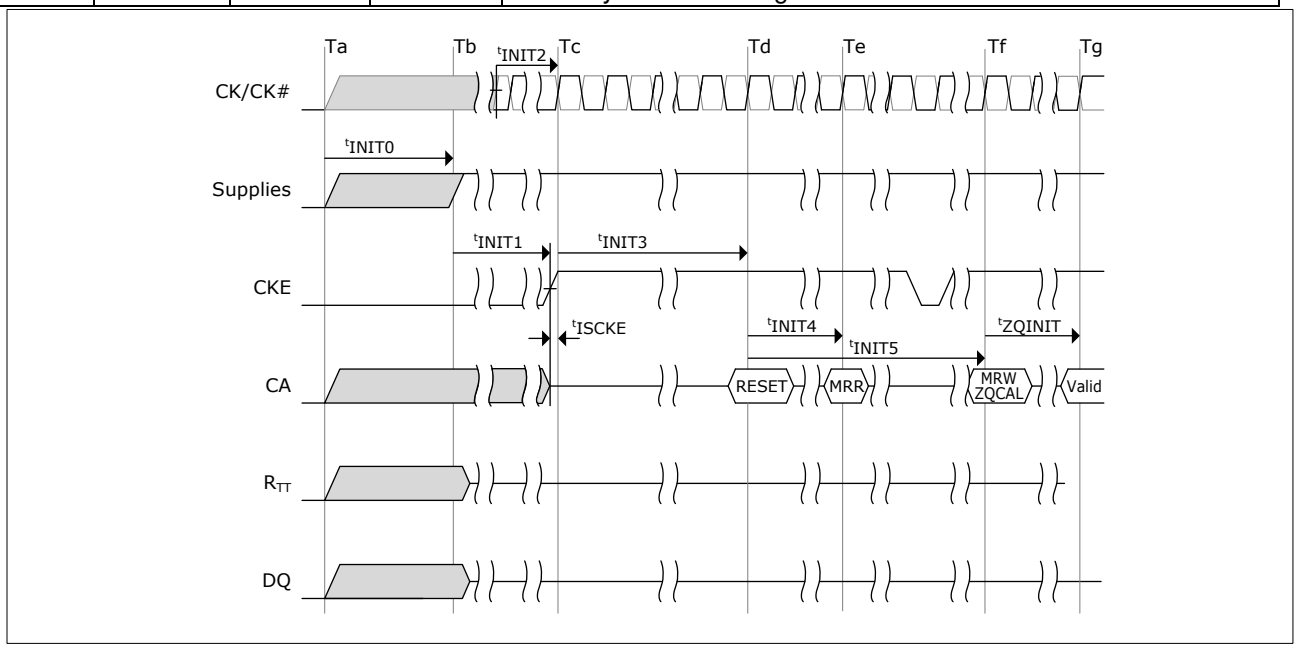


Figure 3.2 Power Ramp and Initialization Sequence

3.2.2 Initialization after Reset (without Power ramp):
If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

3.2.3 Power-off Sequence
The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S4 devices.
While removing power, CKE shall be held at a logic low level (=< 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low. DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDD2 during power off sequence to avoid latch-up.
Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.
Tz is the point where *all* power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.
The following conditions apply:
Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.
Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
Between Tx and Tz, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

Table 2 – Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
tPOFF	-	2	s	Maximum Power-Off ramp time

3.2.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.
Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.
Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.
VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.
Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

3.3 Mode Register Definition

3.3.1 Mode Register Assignment and Definition in LPDDR2 SDRAM

Table 3 shows the 16 common mode registers for LPDDR2 SDRAM **Table 4** shows only LPDDR2 SDRAM mode registers. Additionally **Table 5** shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 3 – Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01h	Device Feature 1	W	nWR(for AP)			WC	BT	BL		
2	02h	Device Feature 2	W	(RFU)				RL & WL			
3	03h	I/O Config-1	W	(RFU)				DS			
4	04h	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05h	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06h	Basic Config-2	R	Revision ID1							
7	07h	Basic Config-3	R	Revision ID2							
8	08h	Basic Config-4	R	I/O width		Density				Type	
9	09h	Test Mode	W	Vendor-Specific Test Mode							
10	0Ah	IO Calibration	W	Calibration Code							
11:15	0Bh~0Fh	(reserved)		(RFU)							

Table 4 — Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10h	PASR_Bank (S4)	W	Bank Mask							
17	11h	PASR_Seg	W	Segment Mask							
18:19	12h:13h	(Reserved)		(RFU)							

Mode Register Assignment in LPDDR2 SDRAM (Reserved for NVM)

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20:31	14h~1Fh	(Do Not Use)									

Table 5 – Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20h	DQ Calibration Pattern A	R	See " DQ Calibration:							
33:39	21h:27h	(Do Not Use)									
40	28h	DQ Calibration Pattern B	R	See " DQ Calibration:							
41:47:00	29h:2Fh	(Do Not Use)									
48:62	30h~3Eh	(Reserved)		(RFU)							
63	3Fh	Reset	W	X							
64:126	40h:7Eh	(Reserved)		(RFU)							
127	7Fh	(Do Not Use)									
128:190	80h: BEh	Reserved for Vendor Use)		(RFU)							
191	BFh	(Do Not Use)									
192:254	C0h:FEh	Reserved for Vendor Use)		(RFU)							
255	FFh	(Do Not Use)									

The following notes apply to Tables 3-5:

NOTE 1. RFU bits shall be set to '0' during Mode Register writes.
NOTE 2. RFU bits shall be read as '0' during Mode Register reads.
NOTE 3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS,DQS# shall be toggled.
NOTE 4. All Mode Registers that are specified as RFU shall not be written.
NOTE 5. Writes to read-only registers shall have no impact on the functionality of the device.

MR0 Device Information (MA <7:0> =00H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI (Optional)		RFU	DI	DAI

DAI(Device Auto-Initialization Status)	Read-only	OP0	**0_B**: DAI complete **1_B**: DAI still in progress	
DI (Device Information)	Read-only	OP1	**0_B**: S4 SDRAM **1_B**: Do Not Use	
RZQI (Built in Self Test for RZQ Information)	Read -only	OP4:OP3	**00_B** : RZQ self test not supported) **01_B** : ZQ-pin may connect to VDD2 or float **10_B** : ZQ-pin may short to GND **11_B** : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD2 or float nor short to GND)	1

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
NOTE 2 If ZQ is connected to VDD2 to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDD2, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per NOTE 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-ohm +/-1%).

MR1 Device Feature 1 (MA <7:0> =01H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	**010_B**: BL4 (default) **011_B**: BL8 **100_B**: BL16 **All others** : reserved	
BT	Write-only	OP<3>	**0_B**: Sequential (default) **1_B**: Interleaved	1
WC	Write-only	OP<4>	**0_B**: Wrap (default) **1_B**: Reserved	
nWR	Write-only	OP<7:5>	**001_B**: nWR =3(default) **010_B**: nWR =4 **011_B**: nWR =5 **100_B**: nWR =6 **101_B**: nWR =7 **110_B** :nWR =8 All others : reserved	2

NOTE 1 BL 16, interleaved is not an official combination to be supported.
NOTE 2 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table 6 - Burst Sequence by BL,BT, and WC

C3	C2	C1	C0	W/C	BT	BL	Burst Cycle Number are Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1B	0_B				6	7	4	5	2	3	0	1								
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		**illegal (not allowed)**															

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.

The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 7 for the respective density and bus width combinations.

Table 7 – LPDDR2 Non Wrap Restrictions

	2Gb	4Gb(2Gb x16 ,2stack x32)
Not across full page boundary		
x16	3FE, 3FF, 000, 001	None
x32	1FE, 1FF, 000, 001	None
Not across sub page boundary		
x16	1FE, 1FF, 200, 201	None
x32	None	None

NOTE 1 Non - wrap BL =4 data-orders shown above are prohibited
2 4Gb device do not support the No Wrap function.

MR2 Device Feature 2 (MA <7:0> =02H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B**: RL =3 /WL=1(default) **0010_B**: RL =4 /WL=2 **0011_B**: RL =5 /WL=2 **0100_B**: RL =6 /WL=3 **0101_B**: RL =7 /WL=4 **0110_B** :RL =8 /WL=4 **All others** : reserved	

MR3 I/O Configuration 1 (MA <7:0> =03H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** reserved **0001_B**: 34.3-ohm typical **0010_B**: 40-ohm typical (default) **0011_B**: 48-ohm typical **0100_B**: 60-ohm typical **0101_B**: reserved **0110_B** :80-ohm typical **0111_B** :120-ohm typical (optional) **All others** : reserved	

MR4 Device Temperature (MA <7:0> =04H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B**: SDRAM Low temperature operating limit exceeded **001_B**: 4X t_{REF}, 4x t_{REFIpb}, 4x t_{REFW} **010_B**: 2X t_{REF}, 2x t_{REFIpb}, 2x t_{REFW} **011_B**: 1X t_{REF}, 1x t_{REFIpb}, 1x t_{REFW} (≤85℃) **100_B**: Reserved **101_B**: 0.25X t_{REF}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B** :0.25X t_{REF}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B** :SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B**: OP<2:0> value has not changed since last read of MR4 **1_B**: OP<2:0> value has changed since last read of MR4

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.
NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.
NOTE 3 If OP2 equals '1', the device temperature is greater than 85℃
NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
NOTE 5 LPDDR2 might not operate properly when OP[2:0] = 000B or 111B.
NOTE 6 LPDDR2 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 52. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
NOTE 7 See "Temperature Sensor" for information on the recommended frequency of reading MR4.

MR5 Basic Configuration 1 (MA <7:0> =05H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacture ID							

LPDDR2 Manufacture ID	Read-only	OP<7:0>	**0000 0000$_B$:** Reserved **0000 0001$_B$:** Samsung **0000 0010$_B$:** Qimonda **0000 0011$_B$:** Elpida **0000 0100$_B$:** Etron **0000 0101$_B$:** Nanya **0000 0111$_B$:** Mosel **0000 1000$_B$:** Winbond **0000 1001$_B$:** ESMT **0000 1010$_B$:** Reserved **0000 1011$_B$:** Spansion **0000 1100$_B$:** SST **0000 1101$_B$:** ZMOS **0000 1110$_B$:** Intel **0001 1100$_B$:** JSC **1111 1110$_B$:** Numonyx **1111 1111$_B$:** Micron **All Others :** Reserved	

MR6 Basic Configuration 2 (MA<7:0> = 06H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**0000 0000$_B$**: A-version	

NOTE 1 MR6 is Vendor Specific

MR7 Basic Configuration 3 (MA <7:0> =07H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**0000 0000$_B$**: A-version	

NOTE 1 MR7 is Vendor Specific

MR8_Basic Configuration 4 (MA<7:0> = 08BH):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	
01b		0101b				00h	

NOTE 1 4Gb device consist of 2Gb (2stack)

MR9_Test Mode (MA<7:0> = 09H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = 0AH):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF$_H$**: Calibration command after initialization **0xAB$_H$**: Long calibration **0x56$_H$**: Short calibration **0xC3$_H$**: ZQ Reset **Others** : Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values
NOTE 2 LPDDR2 devices shall ignore calibration command when a "Reserved" value is written into MR10.
NOTE 3 See AC timing table for the calibration latency.
NOTE 4 If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDD2, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
NOTE 5 LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11:15_(Reserved) (MA<7:0> = 0BH-0FH):

MR16_PASR_Bank Mask (MA<7:0> = 010H):

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Bank Mask (4-bank or 8 bank)							

S4 SDRAM :

Bank <7:0> Mask	Write-only	OP<7:0>	**0$_B$**: refresh enable to the bank (=unmasked, default) **1$_B$**: refresh blocked (=masked)	1

1. For 4-bank S4 SDRAM, only<3:0> are used.

OP	Bank Mask	4-Bank S4 SDRAM	8-Bank S4 SDRAM
0	XXXX XXX1	Bank 0	Bank 0
1	XXXX XX1X	Bank 1	Bank 1
2	XXXX X1XX	Bank 2	Bank 2
3	XXXX 1XXX	Bank 3	Bank 3
4	XXX1 XXXX	-	Bank 4
5	XX1X XXXX	-	Bank 5

6	X1XX XXXX	-	Bank 6
7	1XXX XXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011H): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B**: refresh enable to the segment (=unmasked, default) **1_B**: refresh blocked (=masked)

			1Gb	2Gb, 4Gb	8Gb
Segment	**OP**	**Segment Mask**	**R12 : 10**	**R13 : 11**	**R14 : 12**
0	0	XXXX XXX1	**000_B**		
1	1	XXXX XX1X	**001_B**		
2	2	XXXX X1XX	**010_B**		
3	3	XXXX 1XXX	**011_B**		
4	4	XXX1 XXXX	**100_B**		
5	5	XX1X XXXX	**101_B**		
6	6	X1XX XXXX	**110_B**		
7	7	1XXX XXXX	**111_B**		

NOTE This table indicates the range of row addresses in each masked segment X is do not care for a particular segment

MR18-19_Reserved (MA<7:0> = 012H - 013H):
MR20-31_Do Not Use, NVM only

MR32_DQ Calibration Pattern A (MA<7:0> = 20H):
Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration"

MR33:39_(Do Not Use) (MA<7:0> = 21H-27H):
MR40_DQ Calibration Pattern B (MA<7:0> = 28H):
Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration".

MR41:47_(Do Not Use) (MA<7:0> = 29H-2FH):
MR48:62_(Reserved) (MA<7:0> = 30H-3EH):
MR63_Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE1 For additional information on MRW RESET see "Mode Register Write Command "

MR64:126_(Reserved) (MA<7:0> = 40H-7EH):
MR127_(Do Not Use) (MA<7:0> = 7FH):
MR128:190_(Reserved for Vendor Use) (MA<7:0> = 80H-BEH):
MR191_(Do Not Use) (MA<7:0> = BFH):
MR192:254_(Reserved for Vendor Use) (MA<7:0> = C0H-FEH):
MR255_(Do Not Use) (MA<7:0> = FFH):

4. LPDDR2 Command Definitions and Timing Diagrams

4.1 Activate Command

4.1.1 Activate Command

The SDRAM Activate command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

• 8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

• 8-bank device Precharge All Allowance : tRP for a Precharge All command for an 8-bank device shall equal tRPab, which is greater than tRPpb.

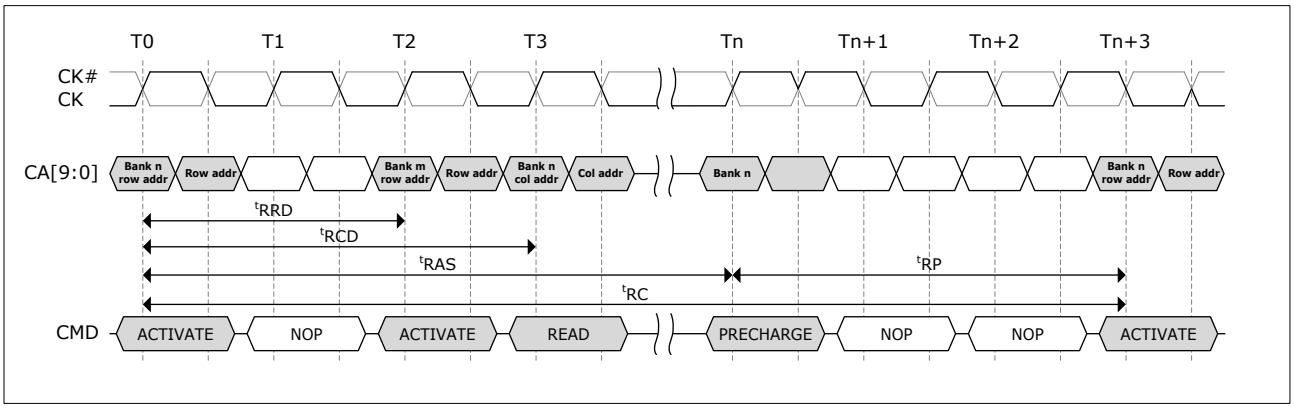


Figure 4.1 — Activate command cycle: tRCD = 3, tRP = 3, tRRD = 2

NOTE 1 A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge.

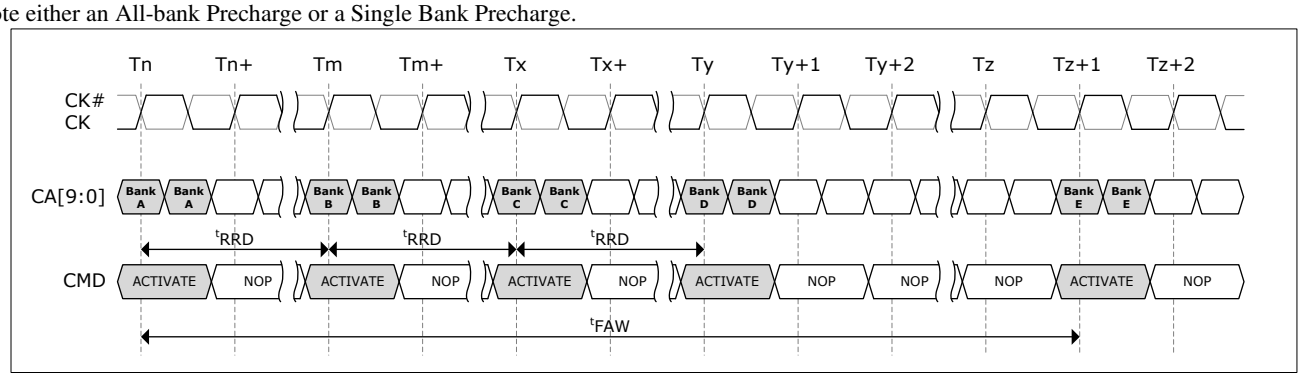
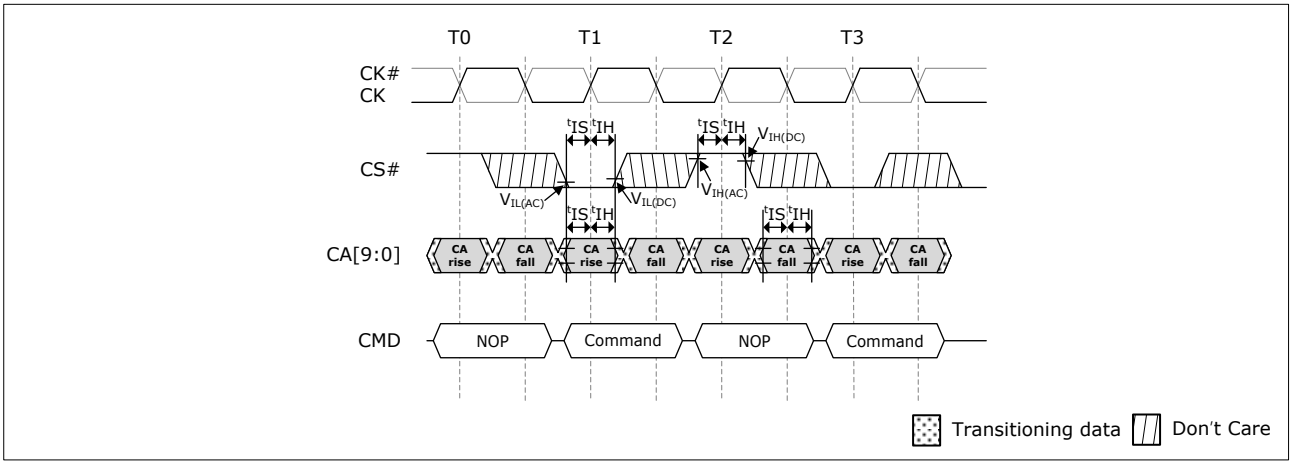


Figure 4.2 — tFAW timing

NOTE 1: For 8-bank devices only.

4.2 LPDDR2 Command Input Signal Timing Definition

4.2.1 LPDDR2 Command Input Setup and Hold Timing



NOTE : Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 4.3 — Command Input Setup and Hold Timing

4.3 Read and Write access modes

4.3.1 Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and tCCD is met.

4.4 Burst Read Command

The Burst Read command is initiated by having CS# LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

Timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

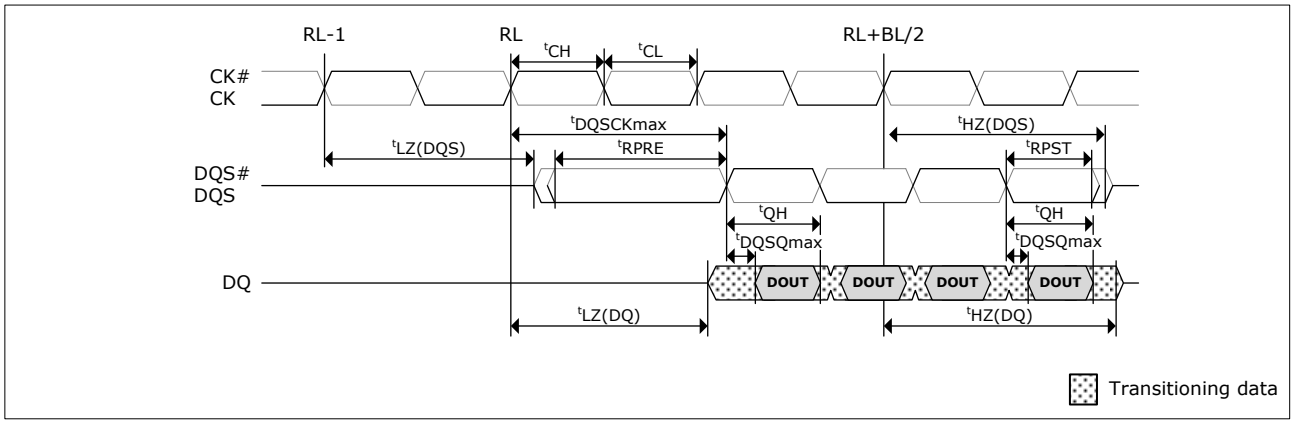


Figure 4.4 — Data output (read) timing ($t_{DQSCKmax}$)

NOTE 1 t_{DQSCK} may span multiple clock periods.
NOTE 2 An effective Burst Length of 4 is shown.

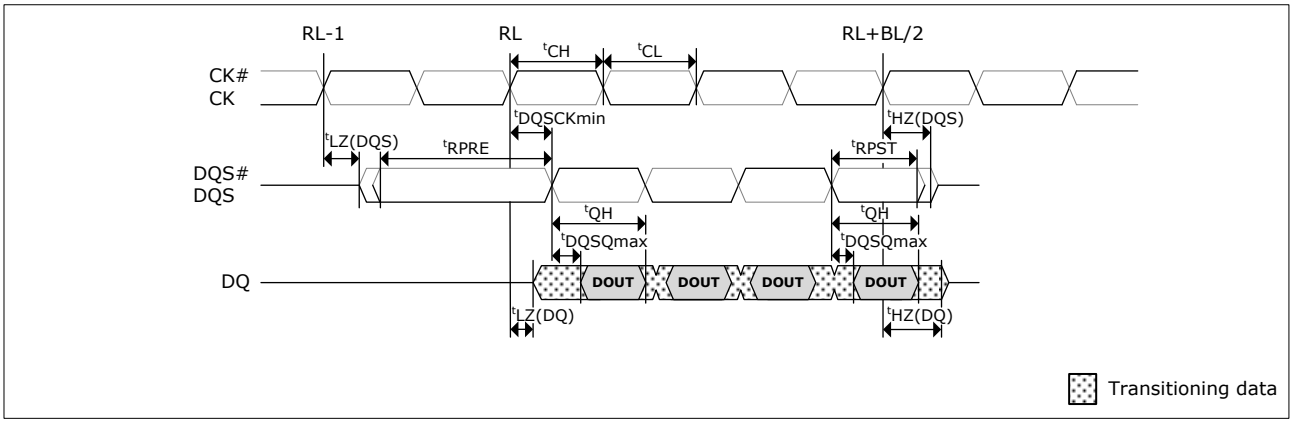


Figure 4.5 — Data output (read) timing ($t_{DQSCKmin}$)

NOTE 1 An effective Burst Length of 4 is shown.

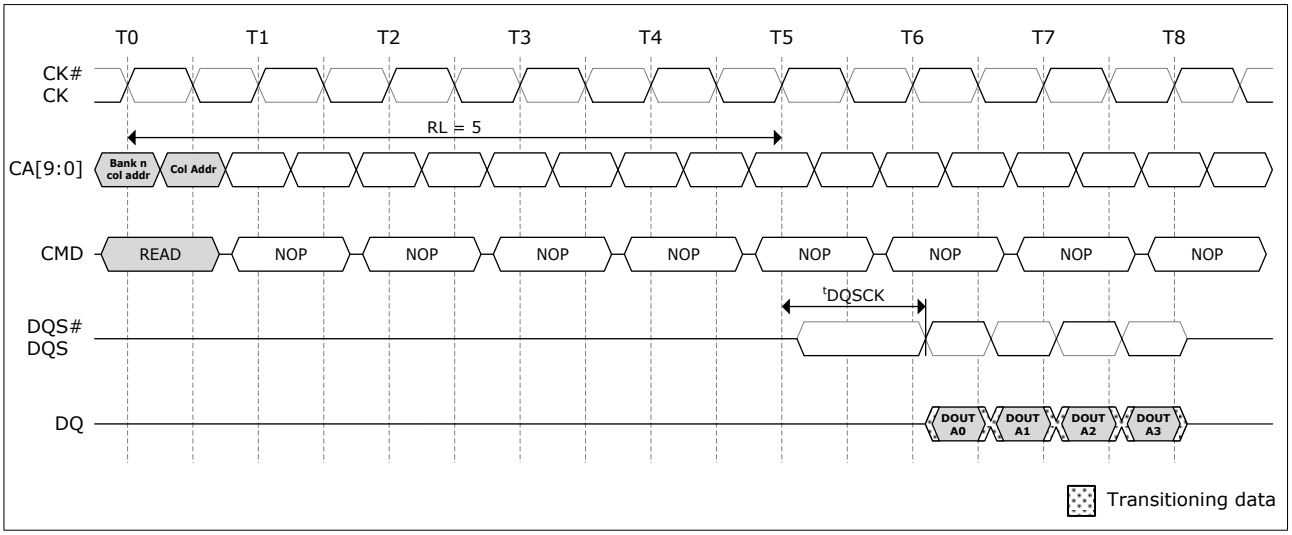


Figure 4.6 — Burst read: RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$

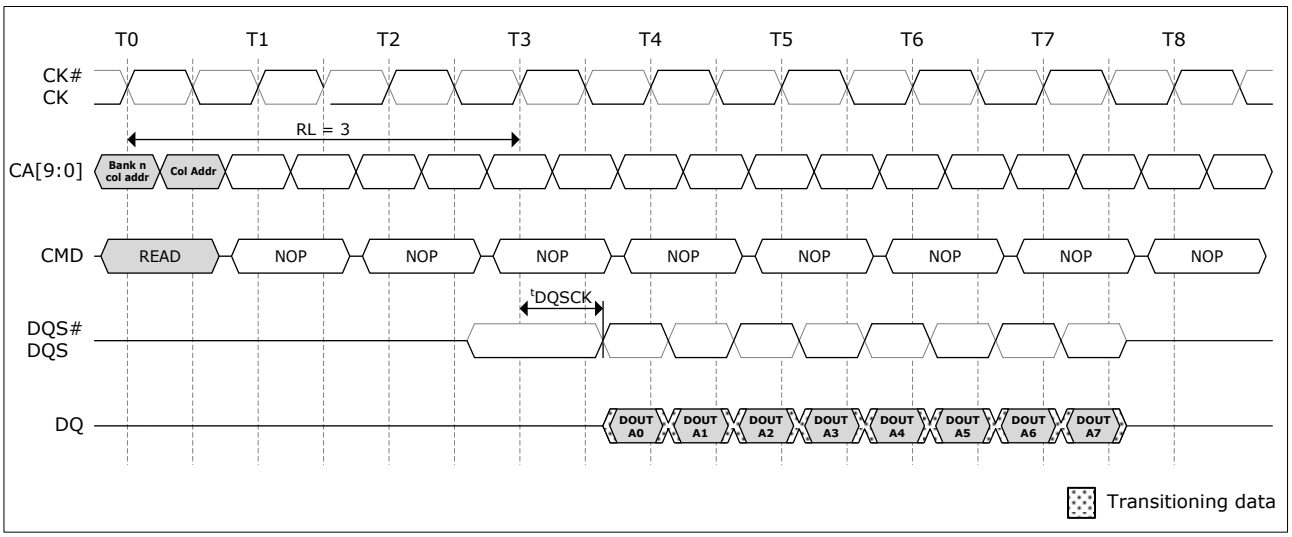


Figure 4.7 — Burst read: RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$

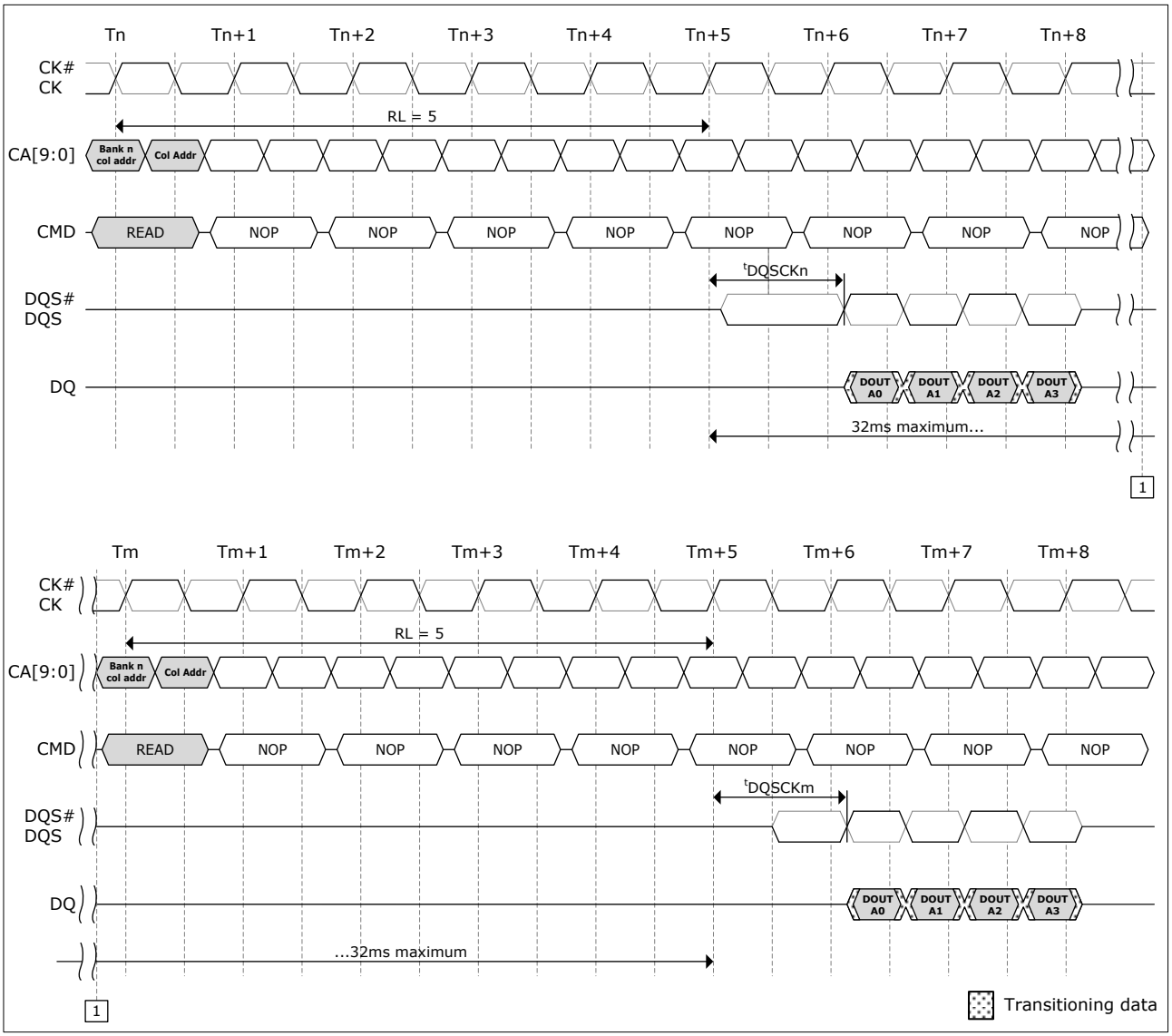


Figure 4.8 — $t_{DQSCKDL}$ timing

NOTE 1 $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair within any 32ms rolling window.

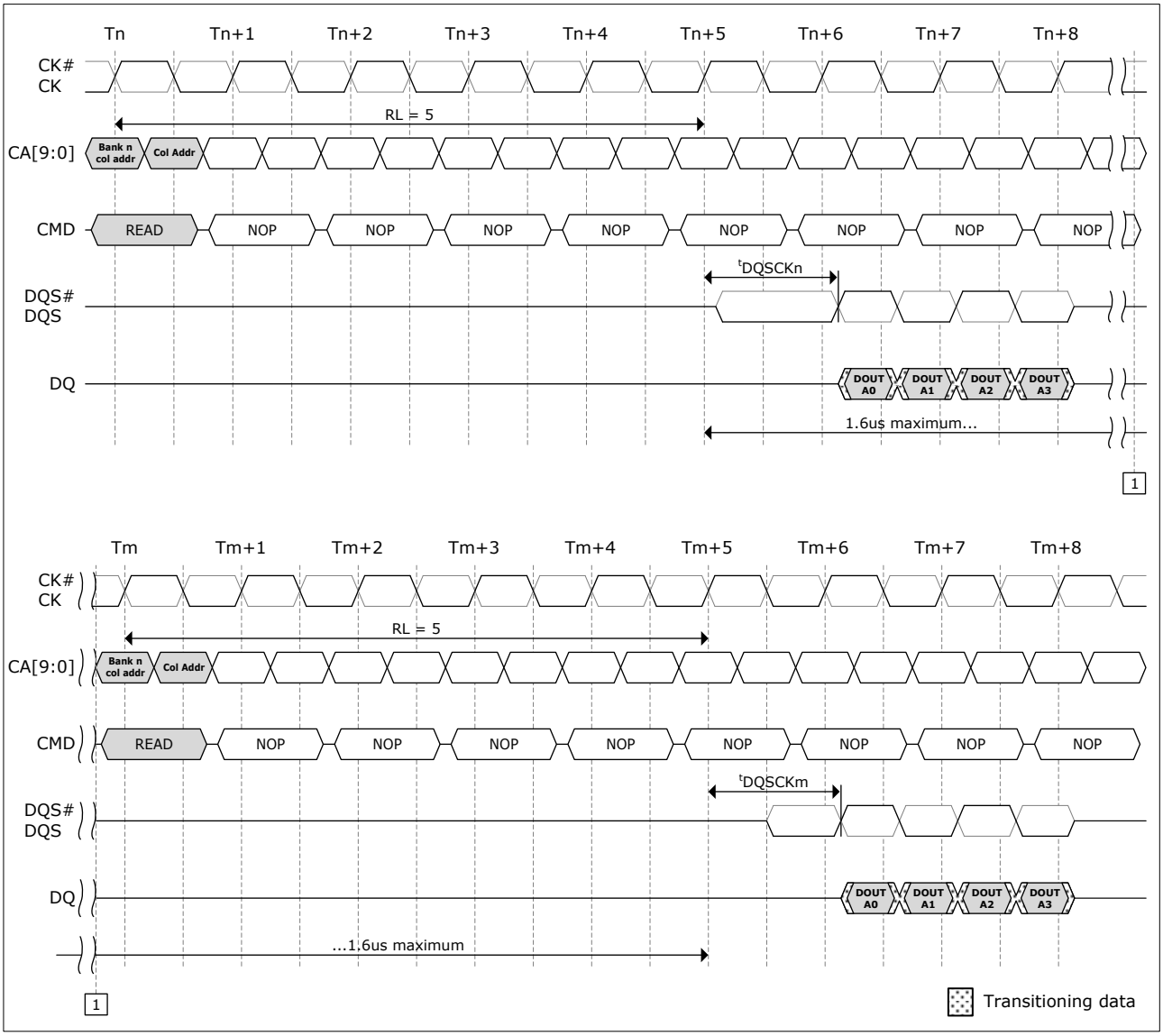


Figure 4.9 — $t_{DQSCKDM}$ timing

NOTE 1 $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window

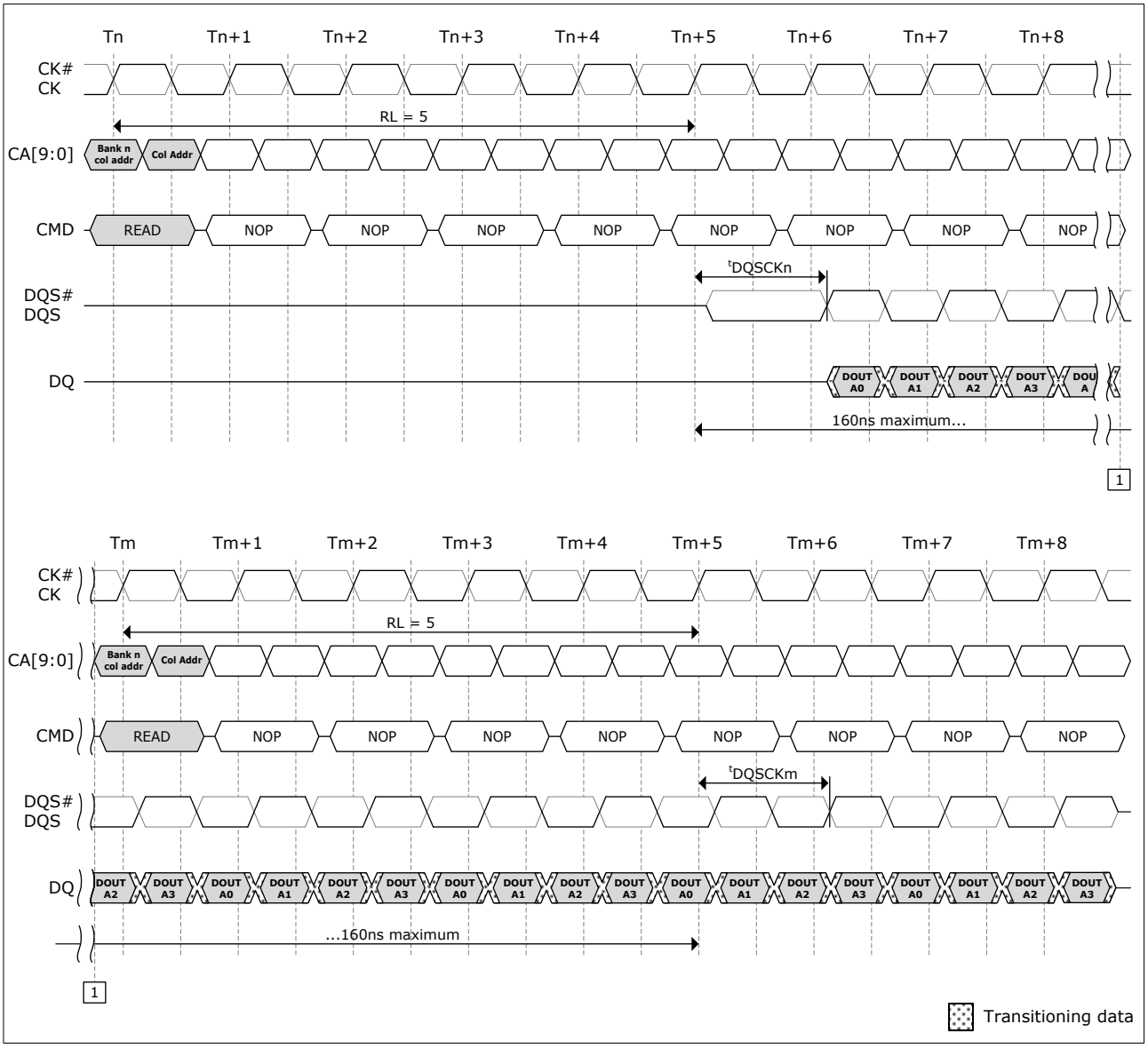


Figure 4.10 — tDQSCKDS timing

NOTE 1 $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair for reads within a consecutive burst within any 160ns rolling window.

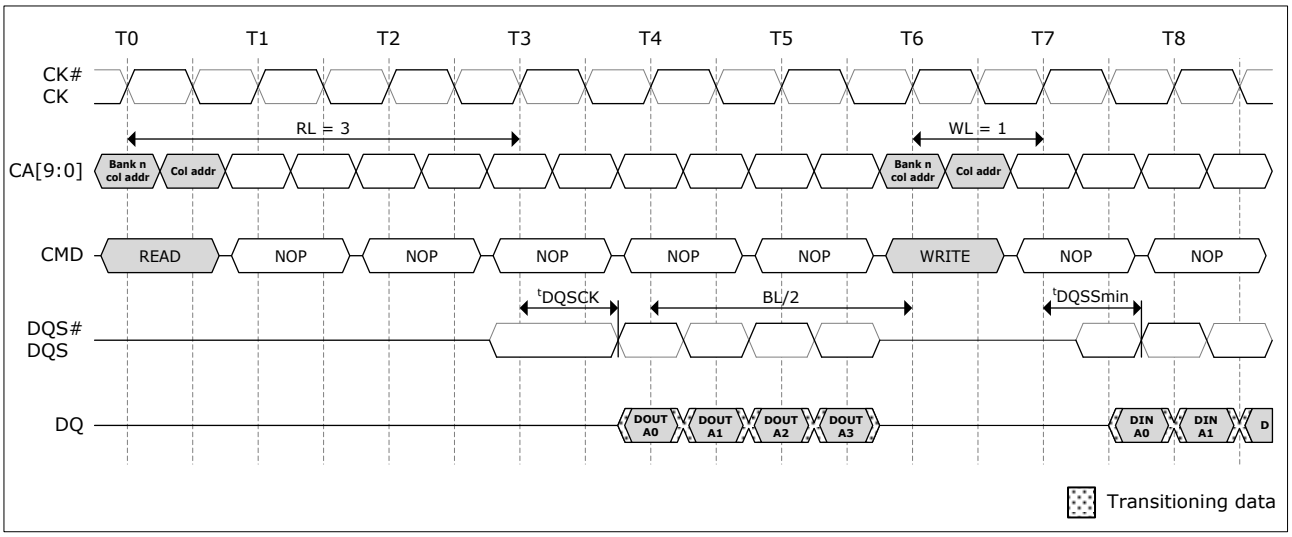


Figure 4.11 — Burst read followed by burst write: RL = 3, WL = 1, BL = 4

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(tDQSCKmax/tCK) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

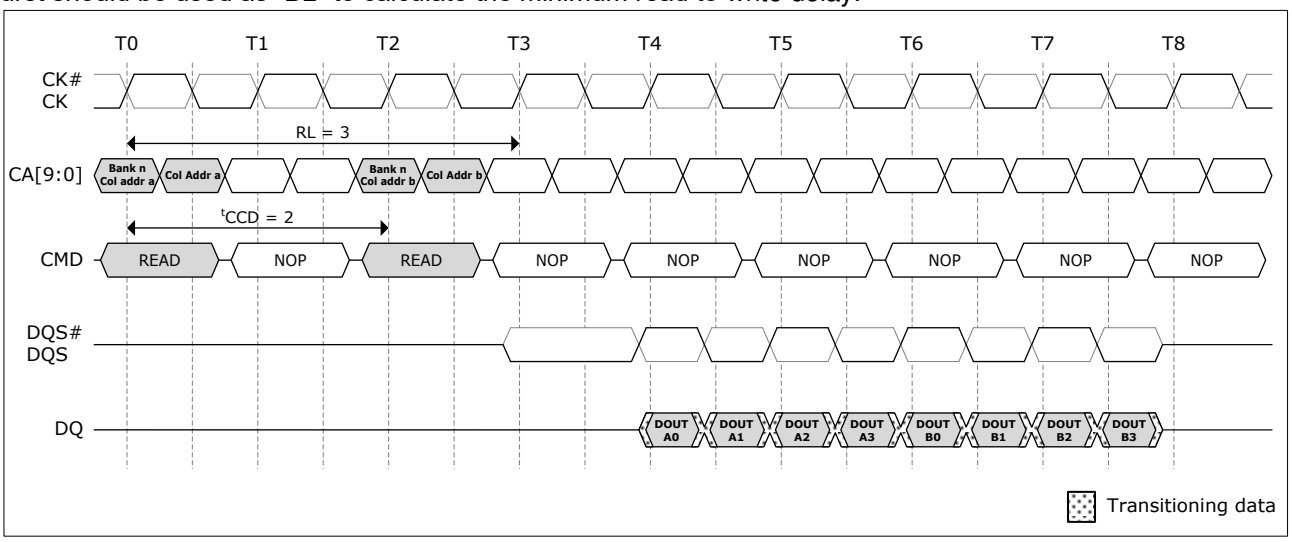


Figure 4.12 — Seamless burst read: RL = 3, BL = 4, tCCD = 2

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

4.4.1 Reads interrupted by a read

For LPDDR2-S4 burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met

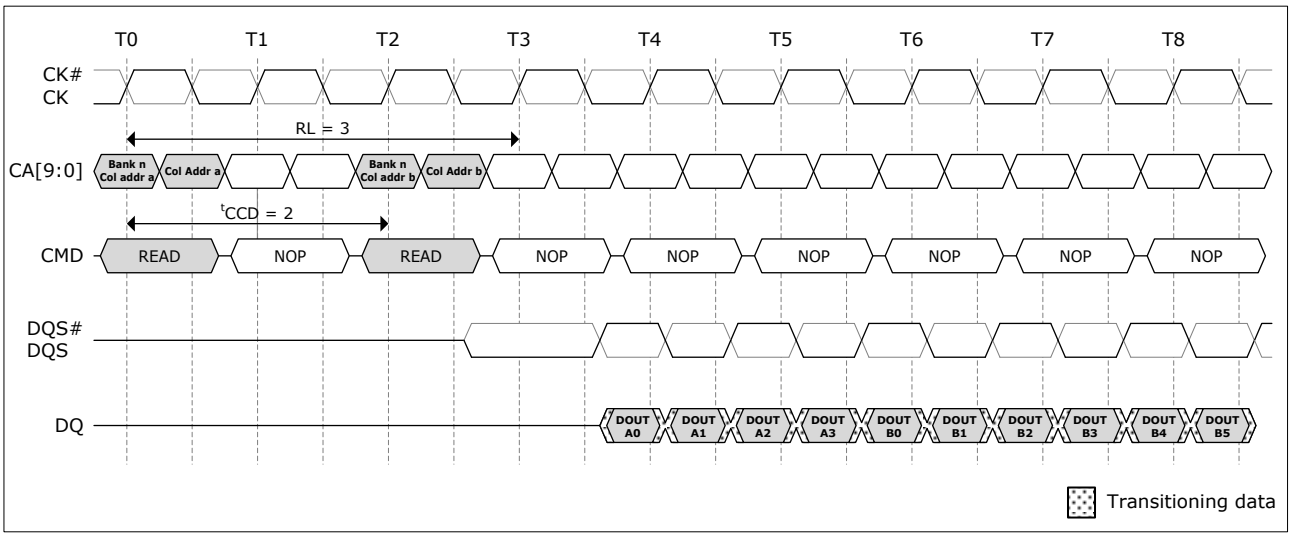


Figure 4.13 — Read burst interrupt example: RL = 3, BL = 8, tCCD = 2

NOTE 1 For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.

NOTE 2 For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous commands, provided that tCCD is met.

NOTE 3 Reads can only be interrupted by other reads or the BST command.

NOTE 4 Read burst interruption is allowed to any bank inside DRAM.

NOTE 5 Read burst with Auto-Precharge is not allowed to be interrupted

NOTE 6 The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

4.5 Burst Write Operation

The Burst Write command is initiated by having CS# LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid datum shall be driven WL * tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW tWPRE prior to the data input. The data bits of the burst cycle must be applied to the DQ pins tDS prior to the respective edge of the DQS, DQS# and held valid until tDH after that edge. The burst data are sampled on successive edges of the DQS, DQS# until the burst length is completed, which is 4, 8, or 16 bit burst.

For LPDDR2-SDRAM devices, tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

Input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

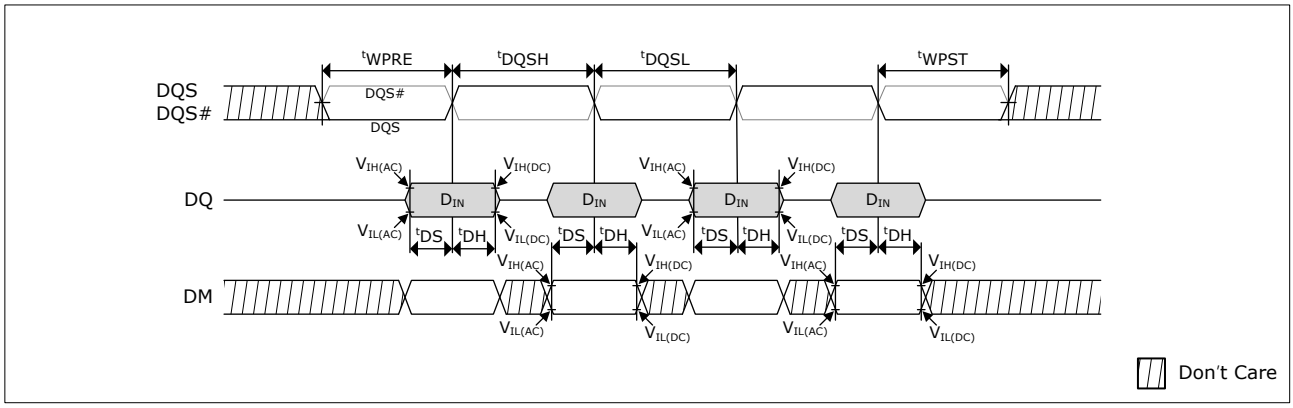


Figure 4.14: Data Input (WRITE) Timing

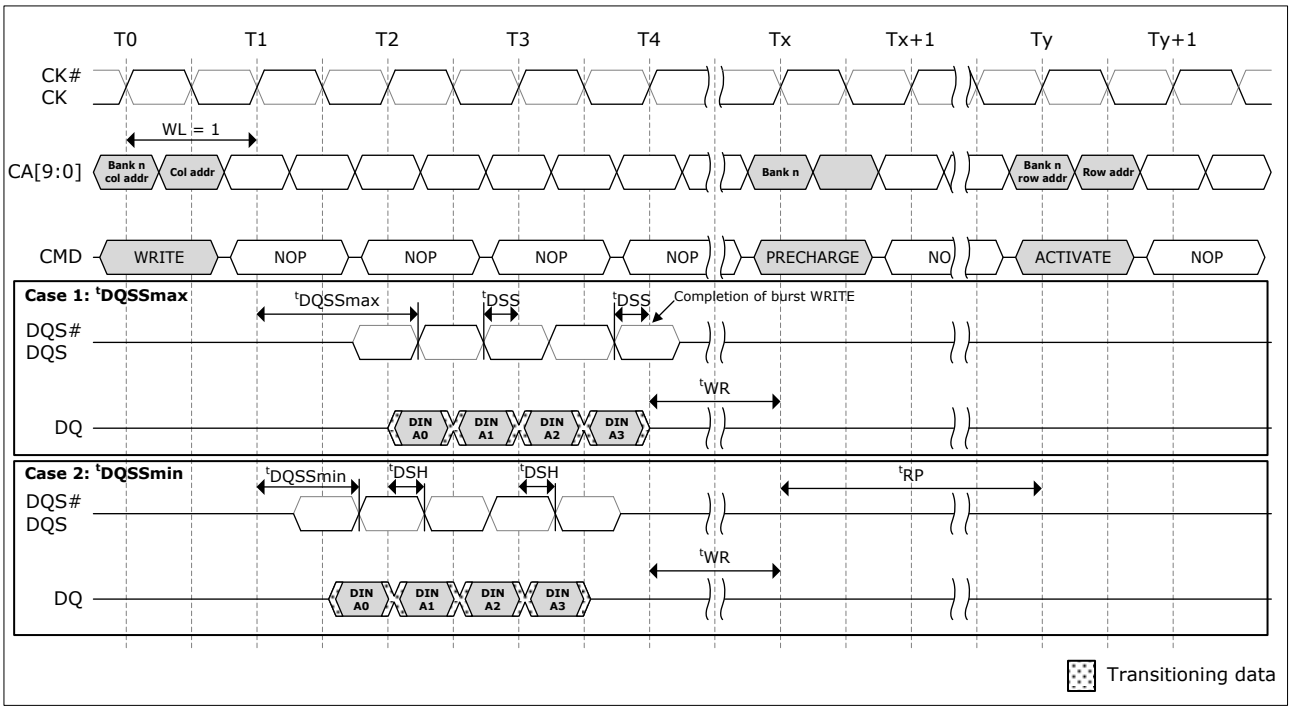


Figure 4.15 — Burst write : WL = 1, BL = 4

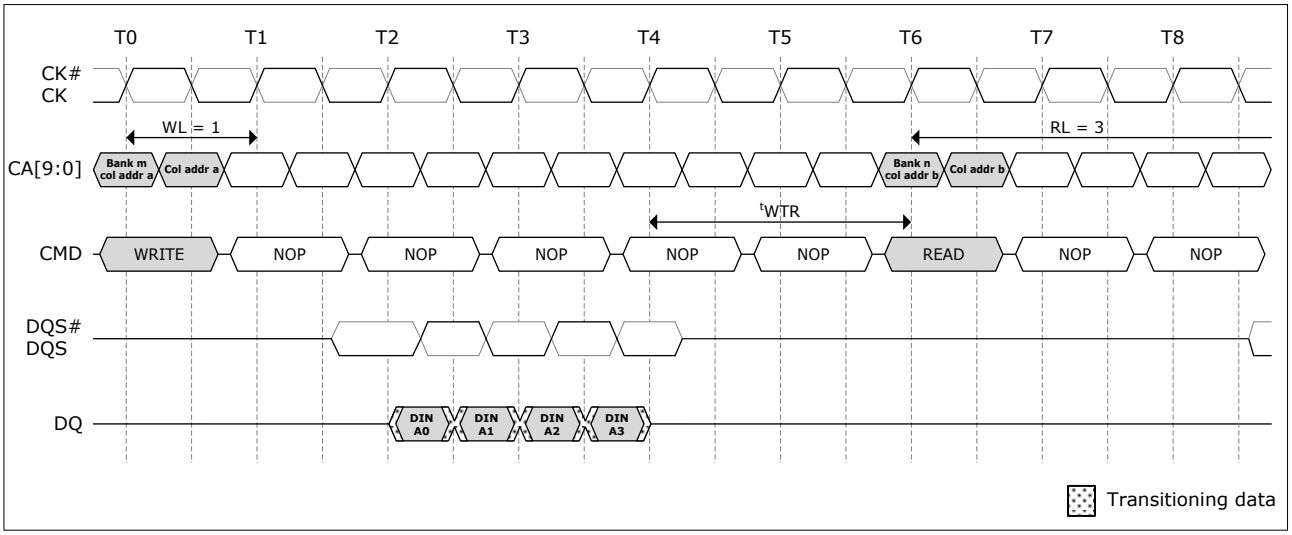


Figure 4.16 — Burst write followed by burst read: RL=3, WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
NOTE 2 tWTR starts at the rising edge of the clock after the last valid input datum.
NOTE 3 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as "BL" to calculate the minimum write to read delay.

4.5.1 Writes interrupted by a write

For LPDDR2-S4 devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that tCCD(min) is met.

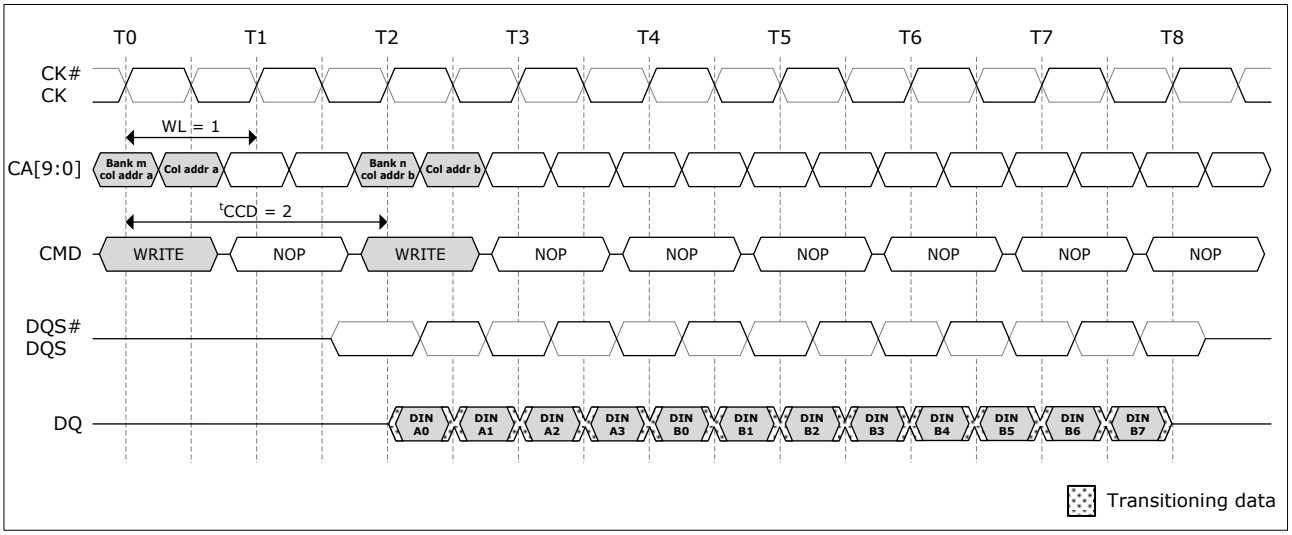


Figure 4.17 — Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2

NOTE 1 For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
NOTE 2 For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.
NOTE 3 Writes can only be interrupted by other writes or the BST command.
NOTE 4 Write burst interruption is allowed to any bank inside DRAM.
NOTE 5 Write burst with Auto-Precharge is not allowed to be interrupted
NOTE 6 The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

4.6 Burst Terminate

The Burst Terminate (BST) command is initiated by having CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows: Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of Read or Write command truncated by a BST command is an integer multiple of 4.

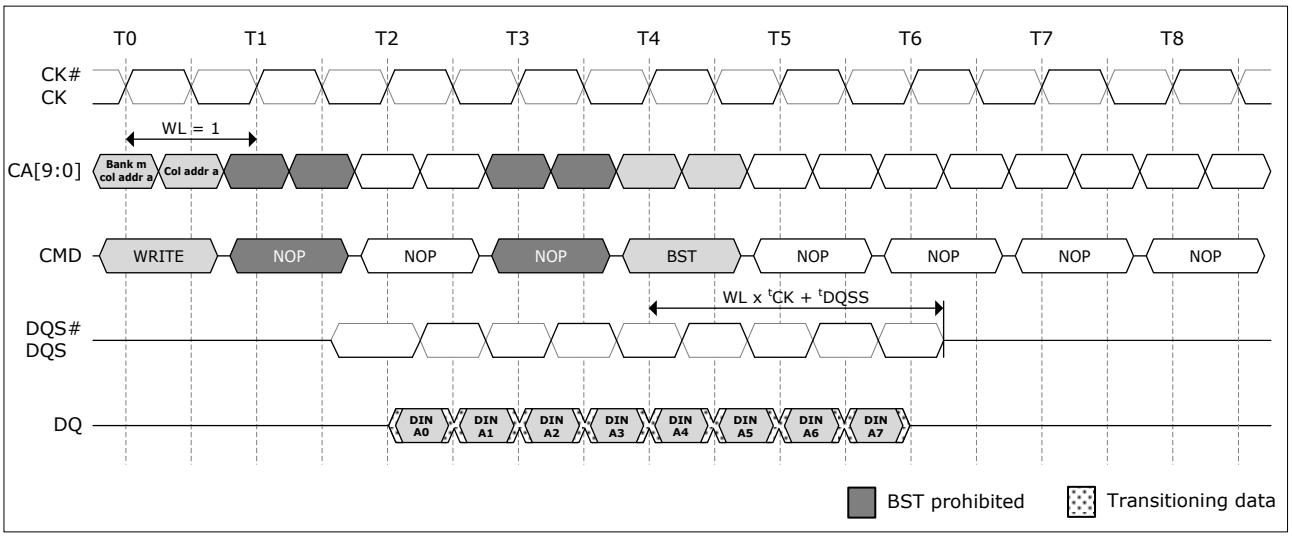


Figure 4.18 — Burst Write truncated by BST: WL = 1, BL = 16

NOTE 1 The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

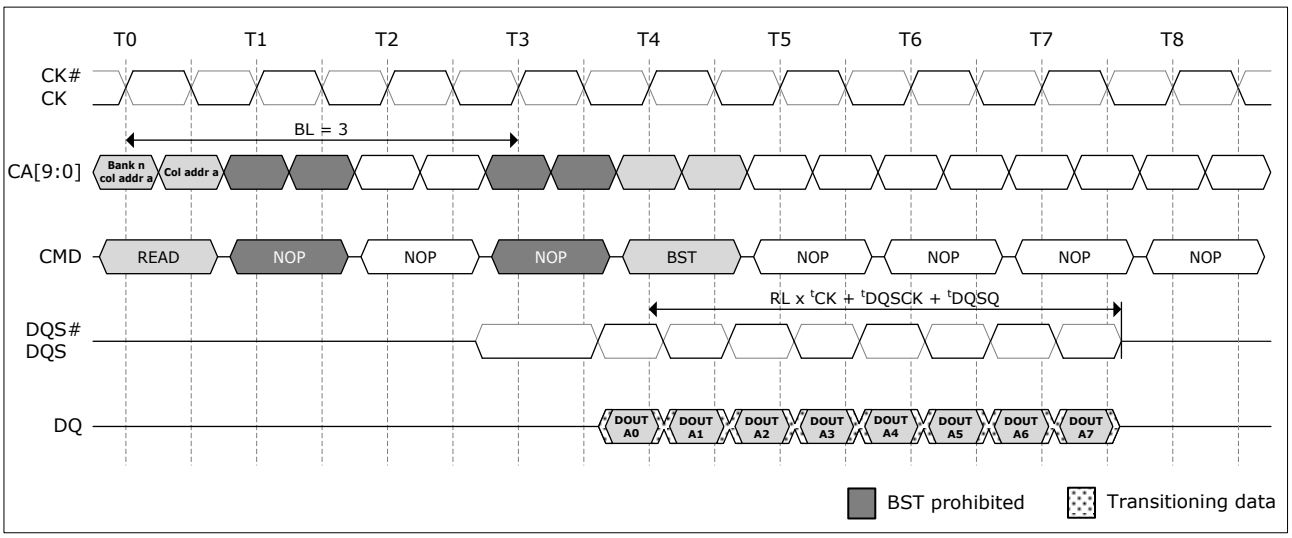


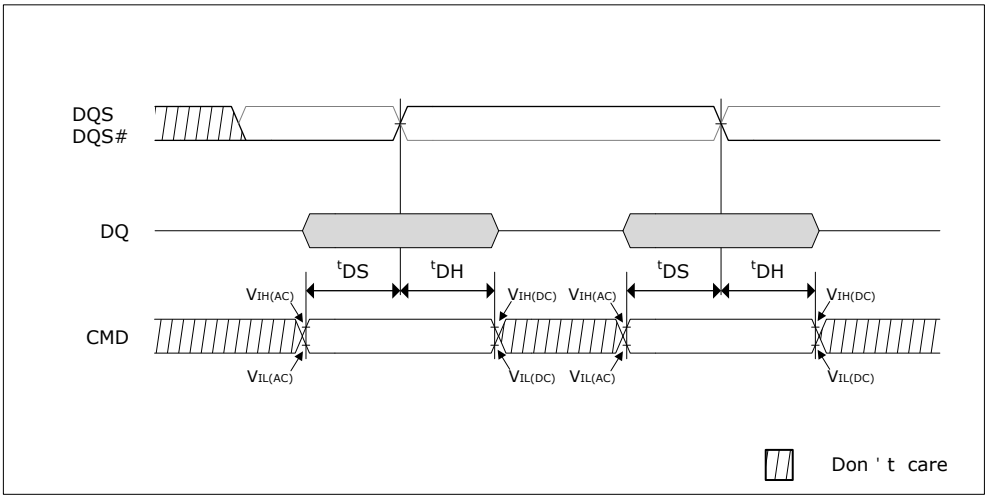
Figure 4.19 — Burst Read truncated by BST: RL=3, BL = 16

NOTE 1 The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.
NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

4.7 Write Data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

Data Mask Timing



Data Mask Function, WL = 2, BL = 4 shown, second DQ masked

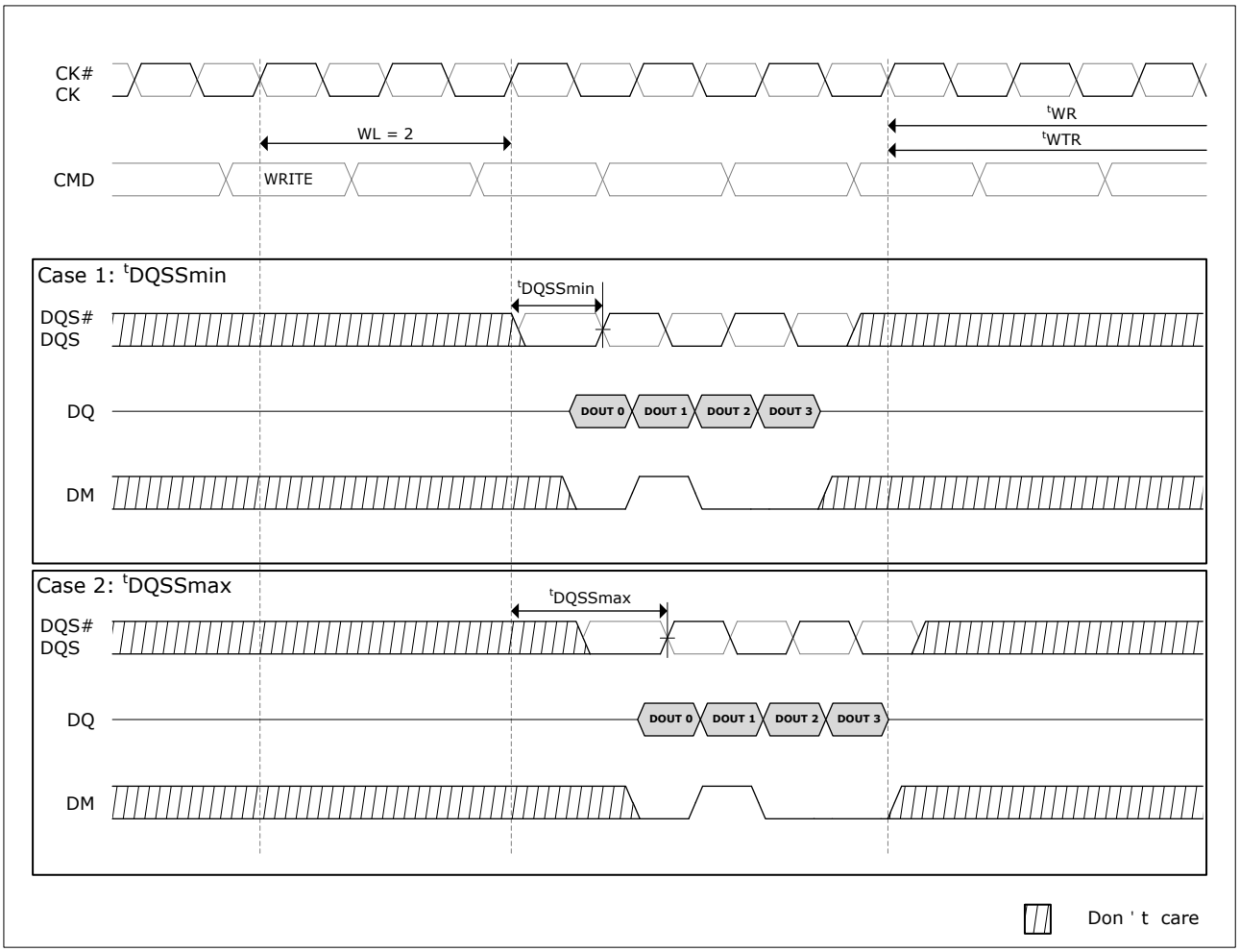


Figure 4.20 — Write data mask

4.8 Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge for 8-bank devices (tRPab) will be longer than the Row Precharge time for a Single-Bank Precharge (tRPpb). For 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge (tRPab) is equal to the Row Precharge time for a Single-Bank Precharge (tRPpb).

Figure 4-1 shows Activate to Precharge timing.

Table 8 – Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don't care	Don't care	Don't care	All Banks	All Banks

4.8.1 Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command cannot be issued until after tRAS is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called tRTP (Read to Precharge).

For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective “BL” shall be used to calculate when tRTP begins.

See Table 9 for Read to Precharge timings for LPDDR2-S4

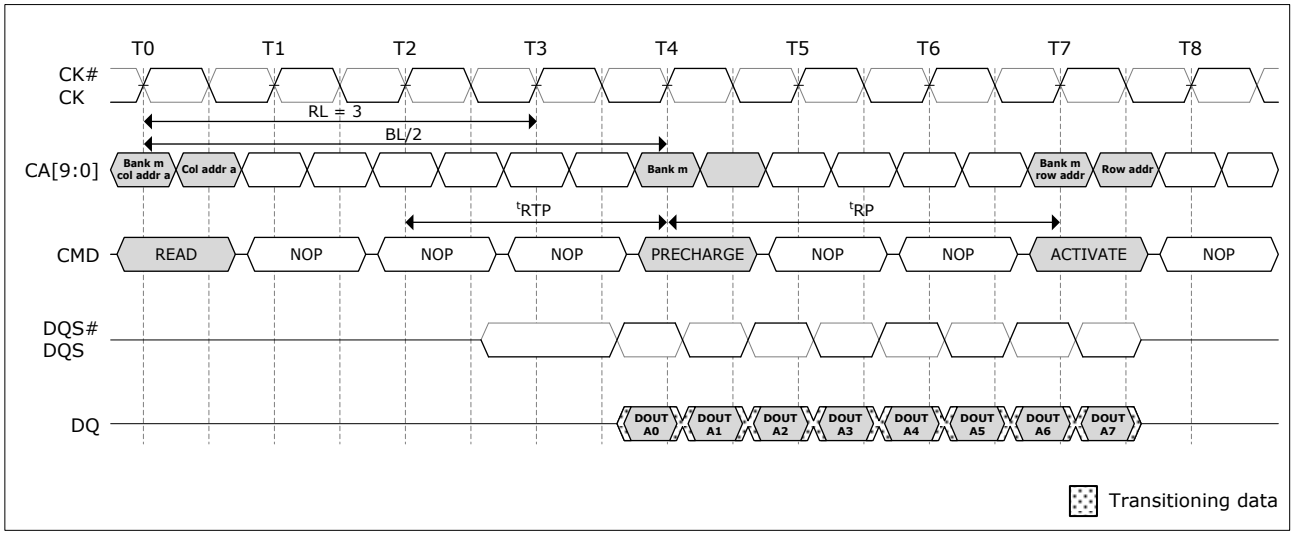


Figure 4.21 — Burst read followed by Precharge:
RL = 3, BL = 8, RU(tRTP(min)/tCK) = 2

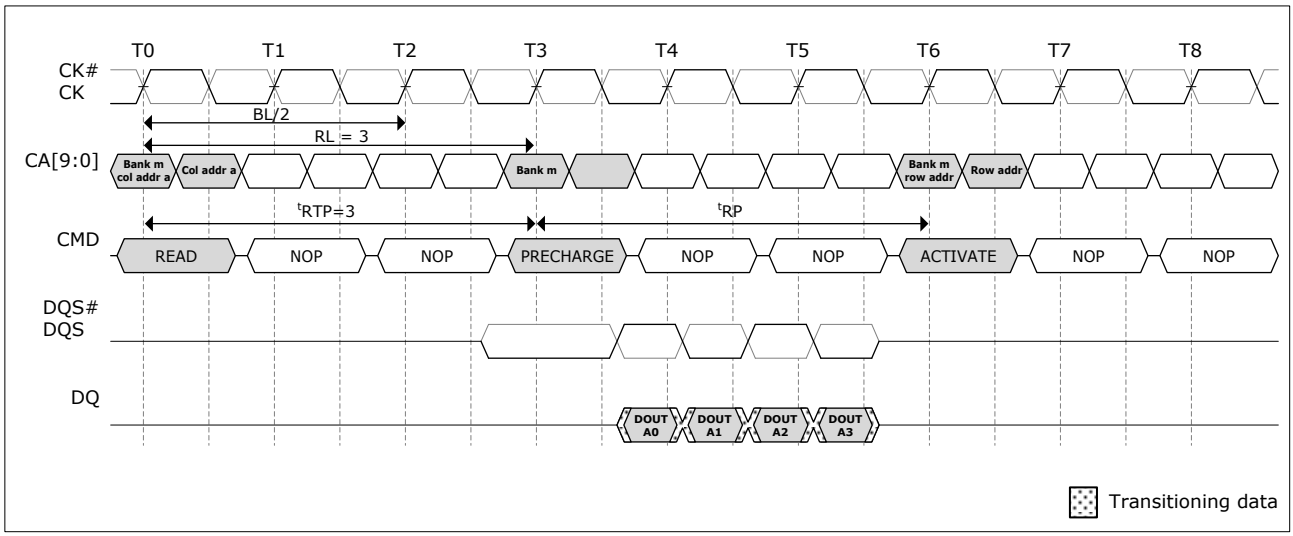


Figure 4.22 — Burst read followed by Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 3

4.8.2 Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the tWR delay.

LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time (tWR) starts at different boundaries for LPDDR2-S4 devices.

For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

See Table 9 for Write to Precharge timings for LPDDR2-S4

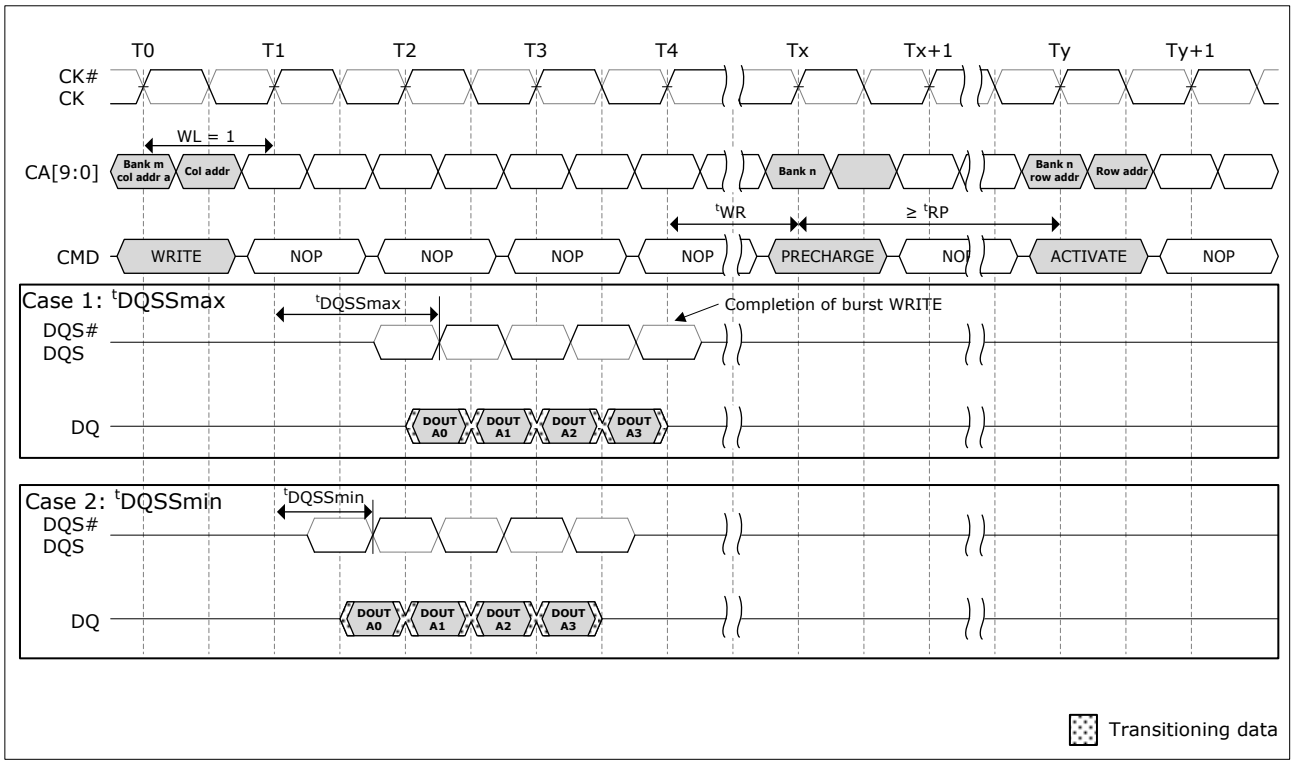


Figure 4.23 — Burst write followed by precharge: WL = 1, BL = 4

4.8.3 Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

4.8.3.1 Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater. Refer to Table 9 for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (tRC) from the previous bank activation has been satisfied.

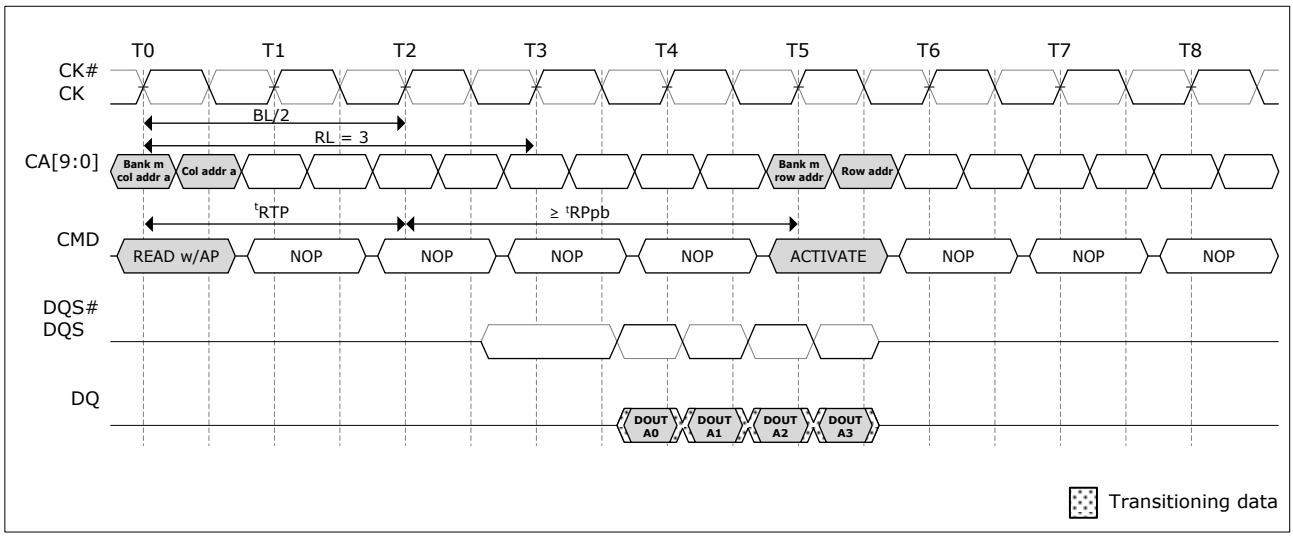


Figure 4.24 — Burst read with Auto-Precharge:
RL = 3, BL = 4, RU(tRTP(min)/tCK) = 2

4.8.3.2 Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (tRC) from the previous bank activation has been satisfied.

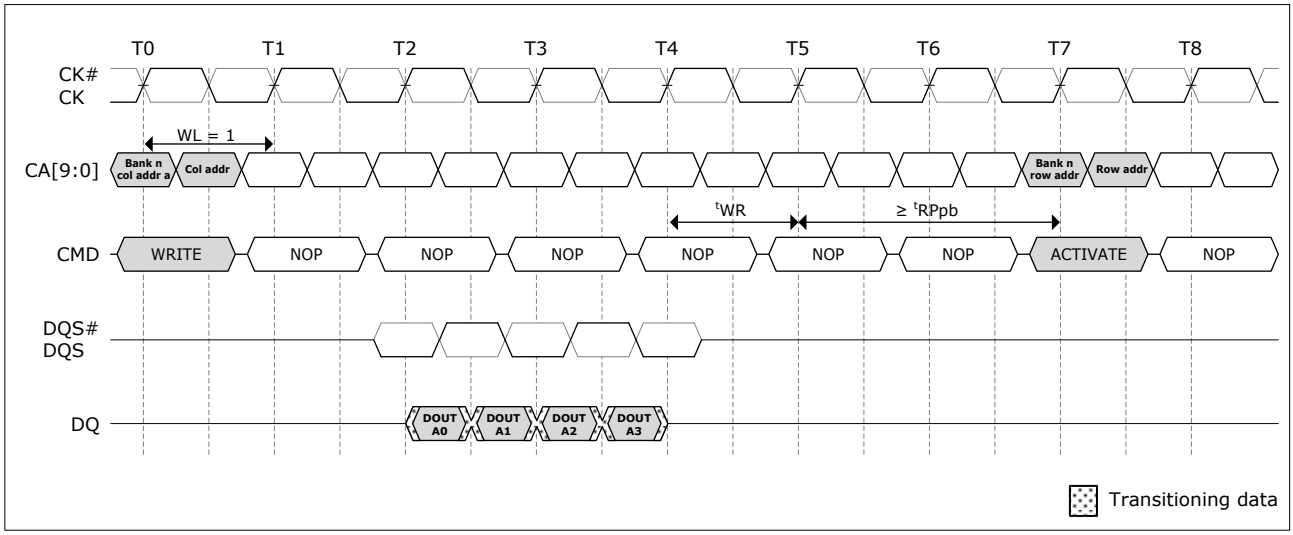


Figure 4.25 — Burst write w/Auto Precharge: WL = 1, BL = 4

Table 9 – Precharge & Auto Precharge Clarification

From command	To command	Minimum Delay between " From Command " to "To Command "	unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2,RU(t_{RTP}/t_{CK})) - 2	clks	1
	Precharge All	BL/2 + max(2,RU(t_{RTP}/t_{CK})) - 2	clks	1
BST (For Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2,RU(t_{RTP}/t_{CK})) - 2	clks	1.2
	Precharge All	BL/2 + max(2,RU(t_{RTP}/t_{CK})) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2,RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL+BL/2+RU(t_{DQSCK}max/t_{CK}) - WL+1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(t_{WR}/t_{CK})+1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK})+1	clks	1
BST (For Writes)	Precharge (to same Bank as Write)	WL + RU(t_{WR}/t_{CK})+1	clks	1
	Precharge All	WL + RU(t_{WR}/t_{CK})+1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK})+1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK})+1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK})+1 +RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	W/L + BL/2 + RU(t_{WTR}/t_{CK})+1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank,
NOTE 2 Any command issued during the minimum delay time as specified in Table 51 is illegal.
NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operation to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

4.9 Refresh command

The Refresh command is initiated by having CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks. A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1- 2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command (see Table 8 , "Bank selection for Precharge by address bits").

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

As shown in Table 10, the REFpb command may not be issued to the memory until the following conditions are met:

a) tRFCab has been satisified after the prior REFab command
b) tRFCpb has been satisfied after the prior REFpb command
c) tRP has been satisified after the prior Precharge command to that given bank
tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessable during the Per Bank Refresh cycle time (tRFCpb), however other banks within the device are accessable and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.

As shown in Table 10, after issuing REFpb:

a) tRFCpb must be satisified before issuing a REFab command
b) tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
c) tRRD must be satisified before issuing an ACTIVATE command to a different bank
d) tRFCpb must be satisified before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in Table 10, the REFab command may not be issued to the memory until the following conditions have been met:

a) tRFCab has been satisified after the prior REFab command
b) tRFCpb has been satisified after the prior REFpb command
c) tRP has been satisified after prior Precharge commands
When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in Table 10, after issuing REFab:

a) the tRFCab latency must be satisfied before issuing an ACTIVATE command
b) the tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table 10 – Command Scheduling Separations related to Refresh

Symbol	Minimum delay from	to	Notes
t_{RFCab}	REFab	REFab	
		Activate cmd to any bank	
		REFpb	
t_{RFCpb}	REFpb	REFab	
		Activate cmd to same bank as REFpb	
		REFpb	
t_{RRD}	REFpb	Activate cmd to different bank than REFpb	
	Activate	REfFpb affecting an idle bank (different bank than Activate)	1
		Activate cmd to different bank than prior Activate	

NOTE 1 A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is now allowed and REFpb is allowed only if it affects a bank which is in the Idle state.

4.9.1 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:
The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within *any* rolling Refresh Window (tREFW = 32 ms @ MR4[2:0] = “011” or Tcase 85 °C). See Table 50 for actual numbers per density.
The resulting average refresh interval (tREFI) is given in Table 50.
See Mode Register 4 for tREFW and tREFI refresh multipliers at different MR4 settings.
For LPDDR2-SDRAM devices supporting Per-Bank-Refresh, a REFab command may be replaced by a full cycle of eight REFpb commands.
(2) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling tREFBW (tREFBW = 4 x 8 x tRFCab). This condition does not apply if REFpb commands are used.
(3) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R* = R - RU{tSRF / tREFI} = R - RU{R * tSRF / tREFW}; where RU stands for the round-up function.

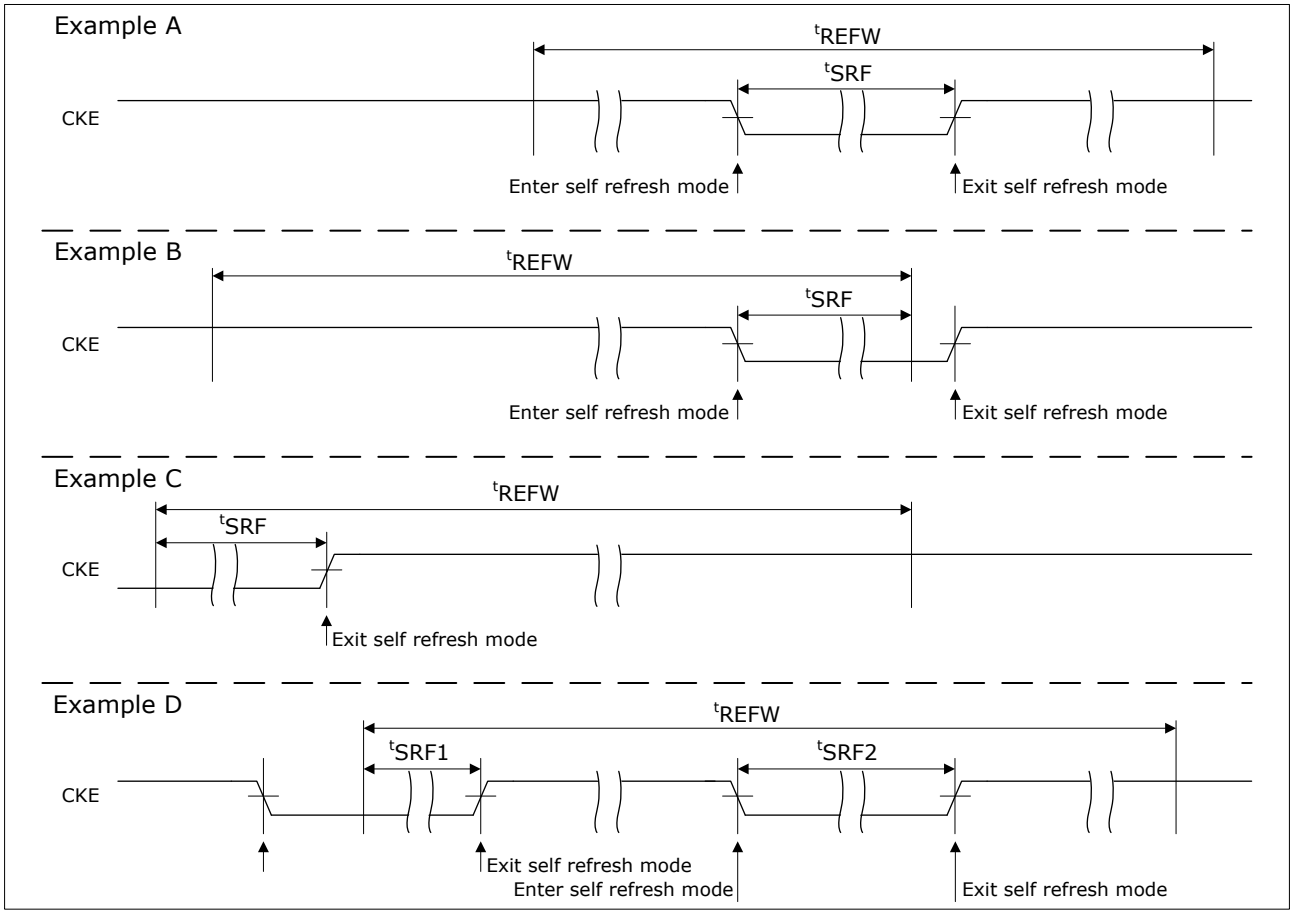


Figure 4.26 — Definition of tSRF

Several examples on how to ***t***SRF is calculated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (***t***REFW),
B: at Self-Refresh entry
C: at Self-Refresh exit
D: with several different intervals spent in Self Refresh during one ***t***REFW interval

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2 devices allow significant flexibiliy in scheduling REFRESH commends, as long as the boundary conditions above are met.
In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time. The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb) the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by tREFW - (R / 8) * tREFBW = tREFW - R * 4 * tRFCab. (e.g., for a LPDDR2-S4 1Gb device @ Tcase <= 85 C this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms).
While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in *every* rolling refresh window during the transition. Figure 4.28 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling tREFW intervals will have at least the required number of refreshes. Figure 4.29 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimmun number of REFRESH commands is not satisfied. The understanding of the pattern transition is extremly relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure 75 and begin with the burst phase upon exit from Self-Refresh.

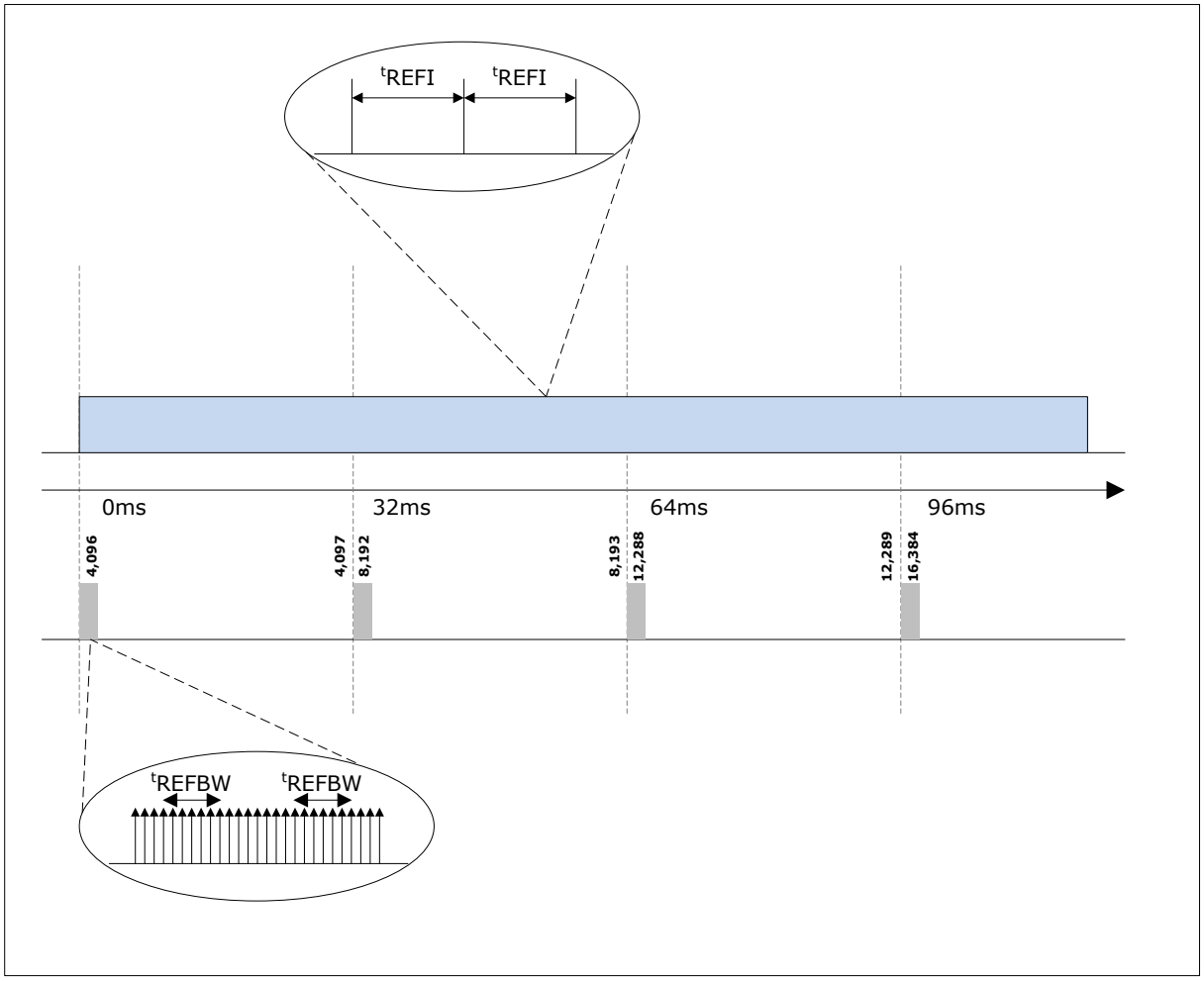


Figure 4.27 — Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause

NOTE 1 For a (e.g.) LPDDR2-S4 2 Gb device @ Tcase less than or equal to 85C the distributed refresh pattern would have one REFRESH command per 3.9 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command

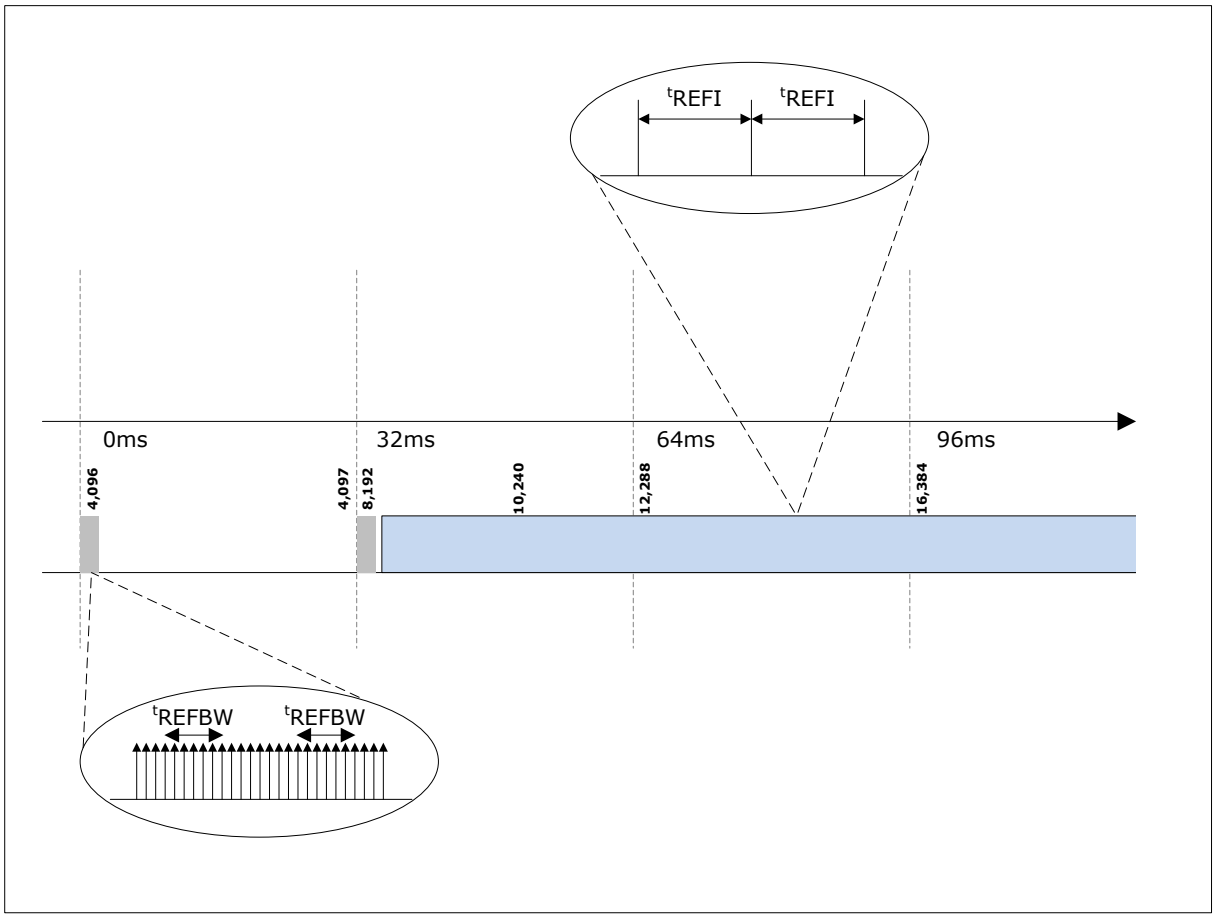


Figure 4.28 — Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE 1 For a (e.g.) LPDDR2-S4 2 Gb device @ Tcase less than or equal to 85 C the distributed refresh pattern would have one REFRESH command per 3.9 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

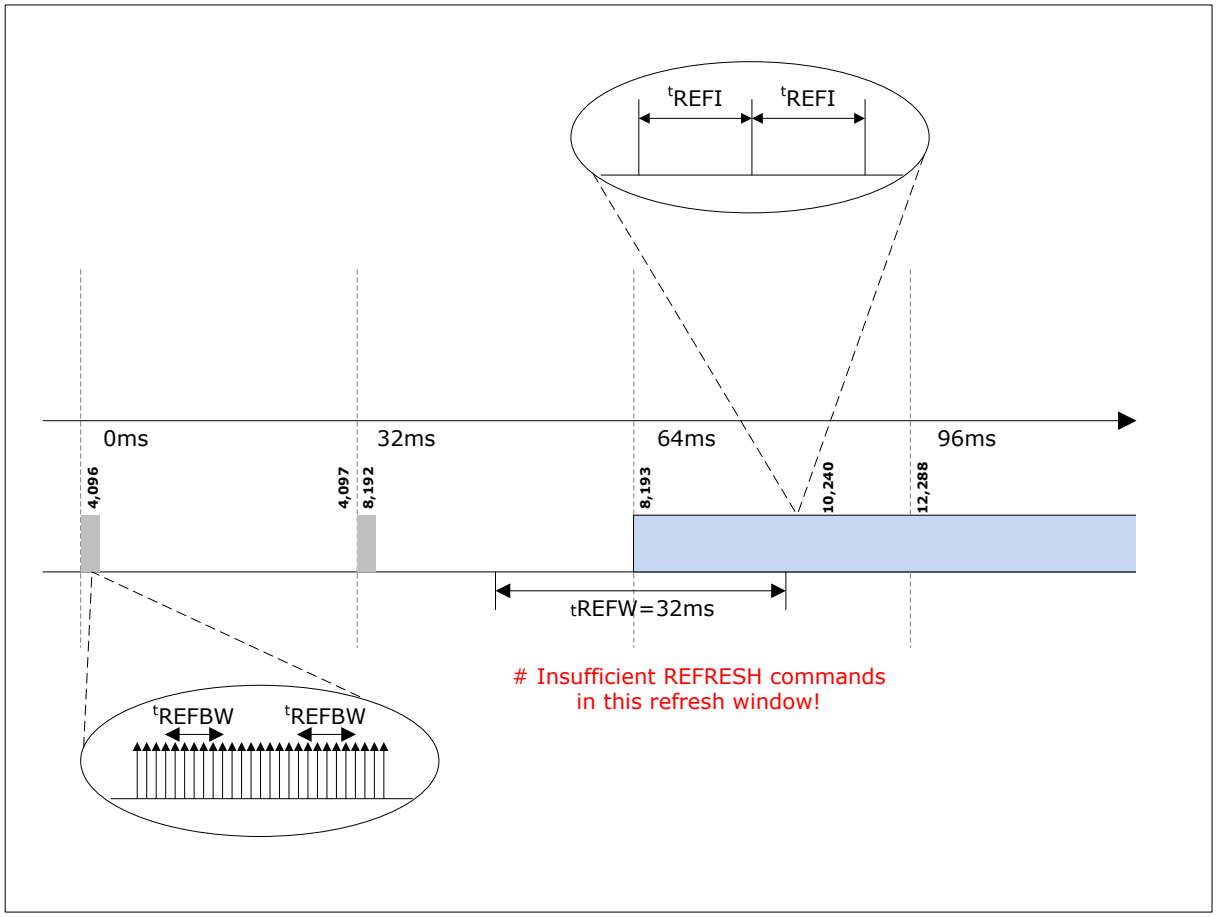


Figure 4.29 — NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE 1 Only ~2048 REFRESH commands (<R!!) in the indicated tREFW win-

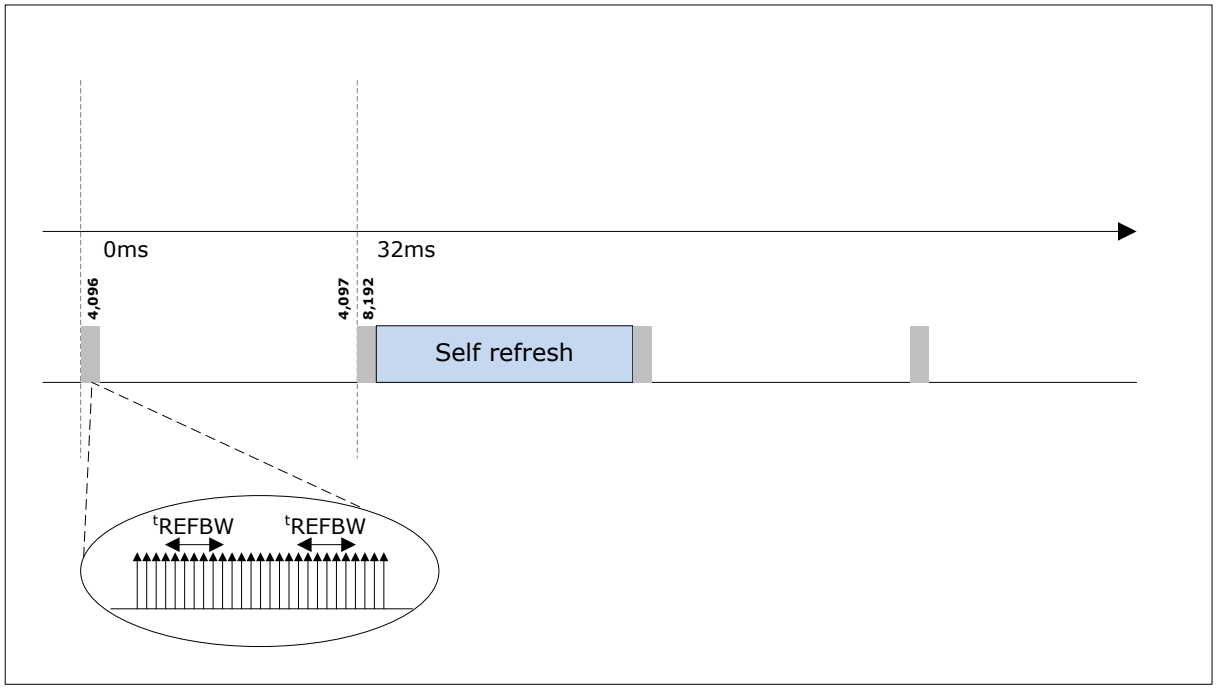


Figure 4.30 — Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns

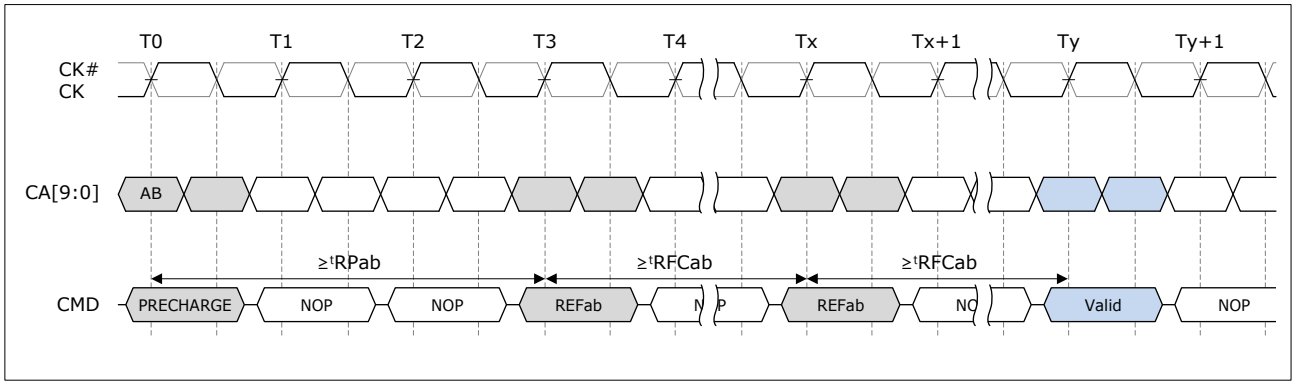
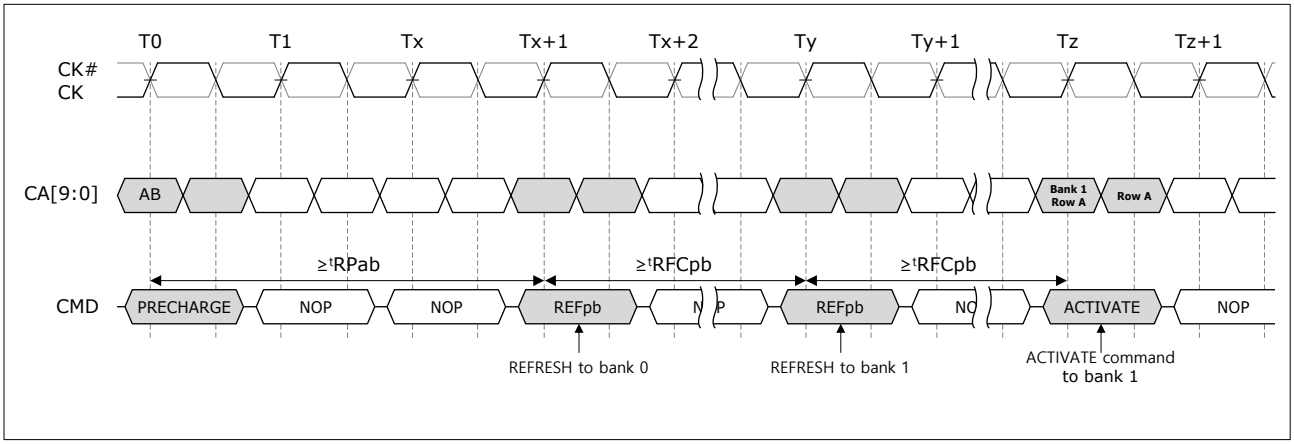


Figure 4.31 — All Bank Refresh Operation



NOTE 1 In the beginning of this example, the REFpb bank is pointing to Bank 0.
NOTE 2 Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

Figure 4.32 — Per Bank Refresh Operation

4.10 Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock.
CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.
LPDDR2 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2- SX devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures. See “LPDDR2 IDD Specification Parameters and Operating Conditions” for details.
Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”.
For proper self refresh operation, power supply pins (VDD1, VDD2, and VDD2) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see “Absolute Maximum DC Ratings”). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see “Recommended DC Operating Conditions”). The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.
The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.
The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section “LPDDR2 SDRAM Refresh Requirements”, since no refresh operations are performed in power-down mode

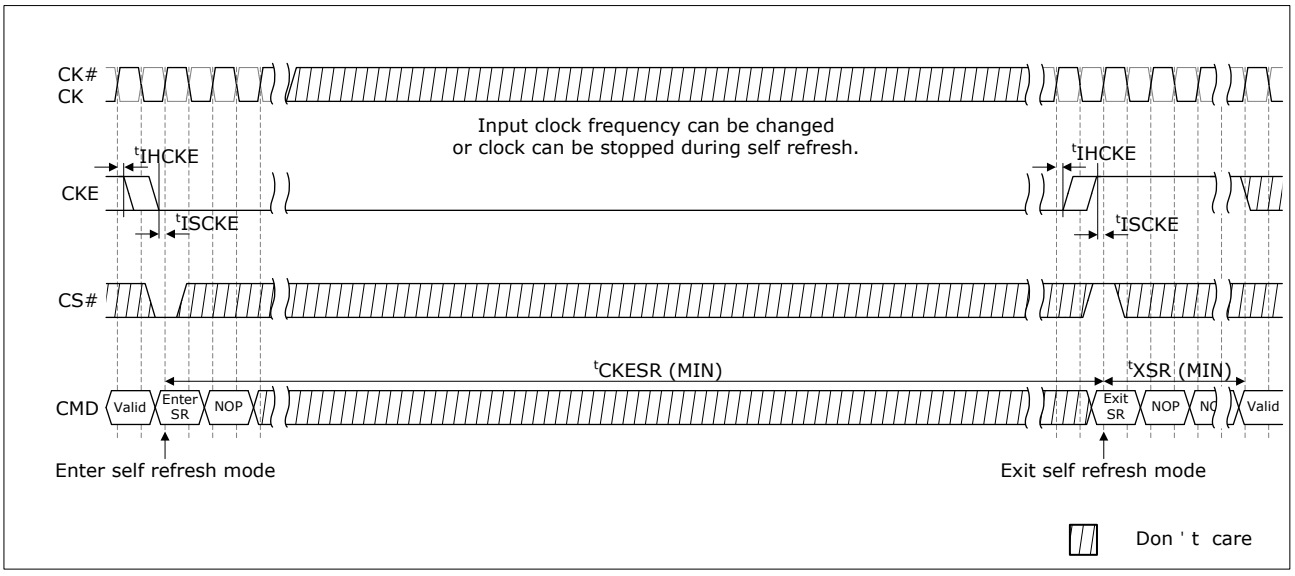


Figure 4.33 — Self-Refresh Operation

NOTE 1 Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
NOTE 2 Device must be in the “All banks idle” state prior to entering Self Refresh mode.
NOTE 3 tXSR begins at the rising edge of the clock after CKE is driven HIGH.
NOTE 4 A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

4.10.1 Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

4.10.2 Partial Array Self-Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. LPDDR2 SDRAM whose density is 64Mb, 128Mb, 256Mb, or 512Mb does not support segment masking. Only bank masking scheme is available. For 1Gb and larger densities, 8 segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. These 2 mode register units are noted as “not used” for low-density LPDDR2-S4 SDRAM and a programming of mask bits has no effect on the device operation.

Table 11 – Example of Bank and Segment Masking use in LPDDR2-S4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
segment 0	0		M						M
segment 1	0		M						M
segment 2	1	M	M	M	M	M	M	M	M
segment 3	0		M						M
segment 4	0		M						M
segment 5	0		M						M
segment 6	0		M						M
segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 7 are masked.

4.11 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers.
The Mode Register Read (MRR) command is initiated by having CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r- CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration". All DQS, DQS# shall be toggled for the duration of the Mode Register Read burst.

The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS, DQS# shall be toggled

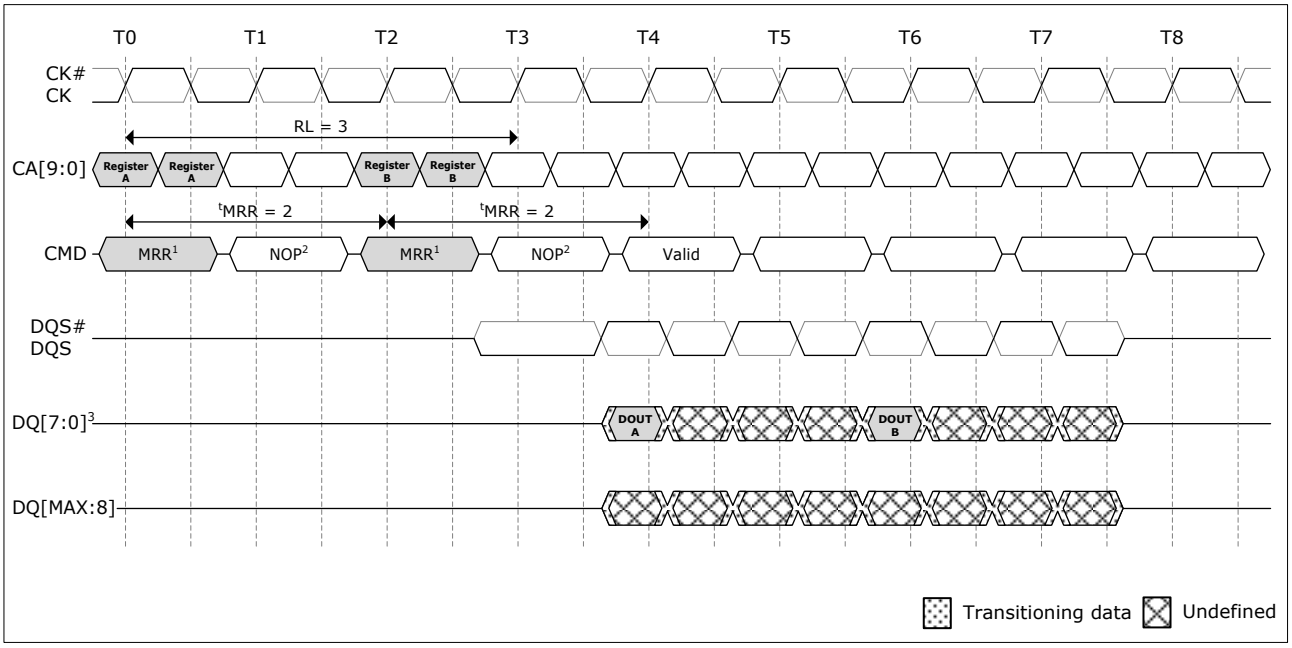


Figure 4.34 — Mode Register Read timing example: RL = 3, tMRR = 2

NOTE 1 Mode Register Read has a burst length of four.
NOTE 2 Mode Register Read operation shall not be interrupted.
NOTE 3 Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
NOTE 4 The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
NOTE 5 Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
NOTE 6 Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
NOTE 7 Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL".

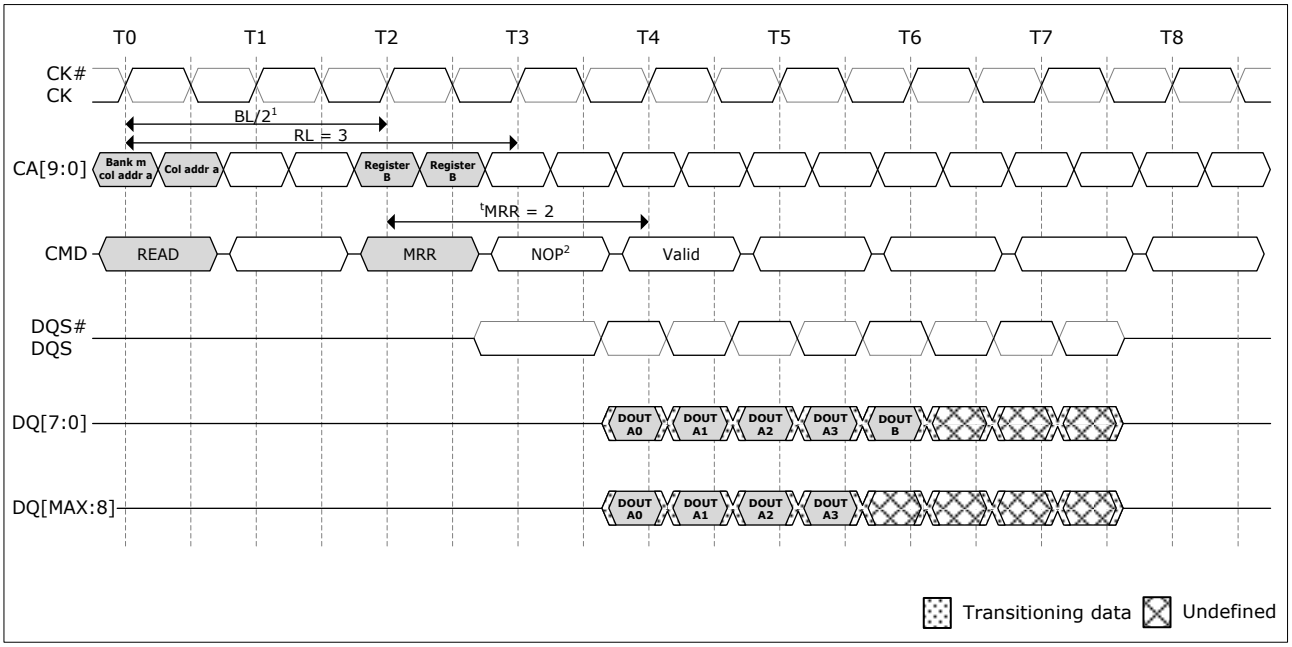


Figure 4.35 — Read to MRR timing example: RL = 3, tMRR = 2

NOTE 1: The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
NOTE 2: The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

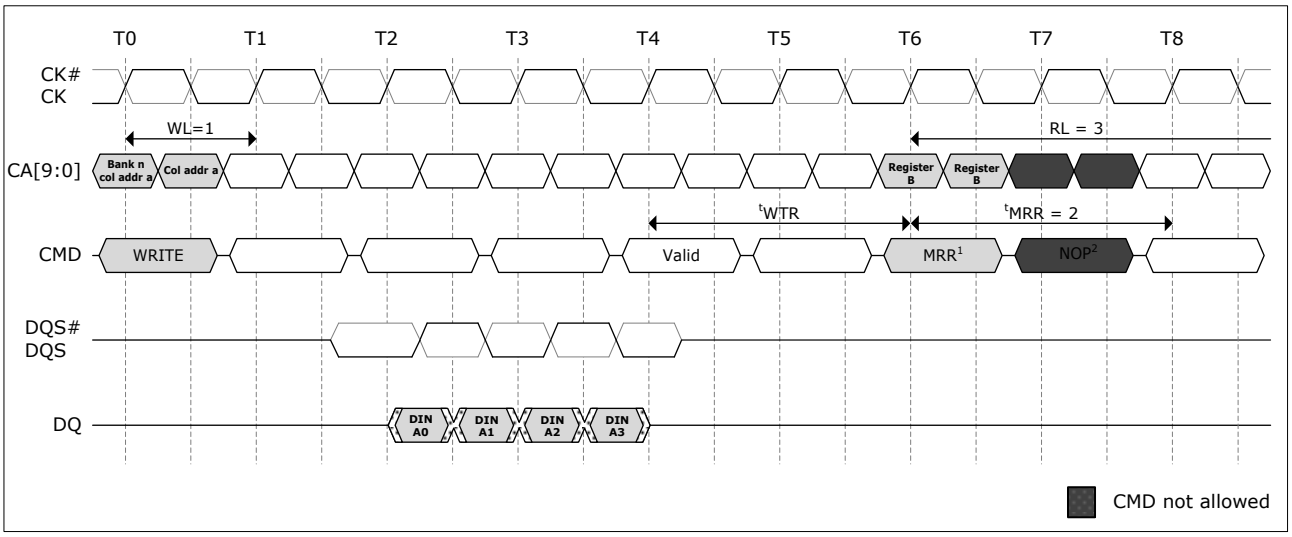


Figure 4.36 — Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
NOTE 2 The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed duringthis period.

4.11.1 Temperature Sensor

LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM), determine whether AC timing de-rating is required in the Extended Temperature Range (SDRAM), and/or monitor the operating temperature (SDRAM). Either the temperature sensor or the device TOPER (See “Operating Temperature Range”) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.
When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See “Operating Temperature Range”) that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85o C when MR4[2:0] equals 011B.
To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest

over a range of 2°C.

ReadInterval is the time period between MR4 reads from the system.
TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
SysRespDelay is the maximum time between a read of MR4 and the response by the system.

LPDDR2 devices shall allow for a 2°C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.
In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2C$$

Table 12 — Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	MAX	System Dependent	℃/s	
MR4 Read Interval	ReadInterval	MAX	System Dependent	ms	
Temperature Sensor Interval	tTSI	MAX	32	ms	
System Response Delay	SysRespDelay	MAX	System Dependent	ms	
Device Temperature Margin	TempMargin	MAX	2	℃	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 32ms + 1ms) \leq 2C$$

In this case, ReadInterval shall be no greater than 167 ms.

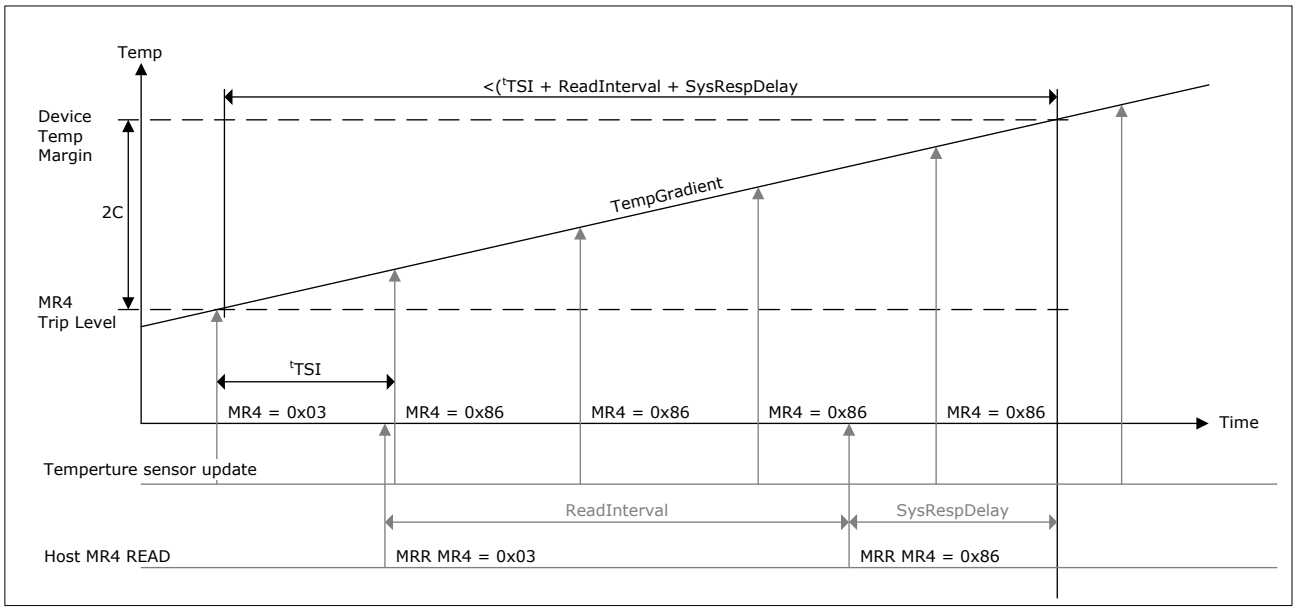


Figure 4.37 — Temp Sensor Timing

4.11.2 DQ Calibration

LPDDR2 feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] for x8 devices, DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

For LPDDR2 devices, MRR DQ Calibration commands may only occur in the Idle state

Table 13 — Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern "A"(MR32)	1	0	1	0
Pattern "B"(MR40)	0	0	1	1

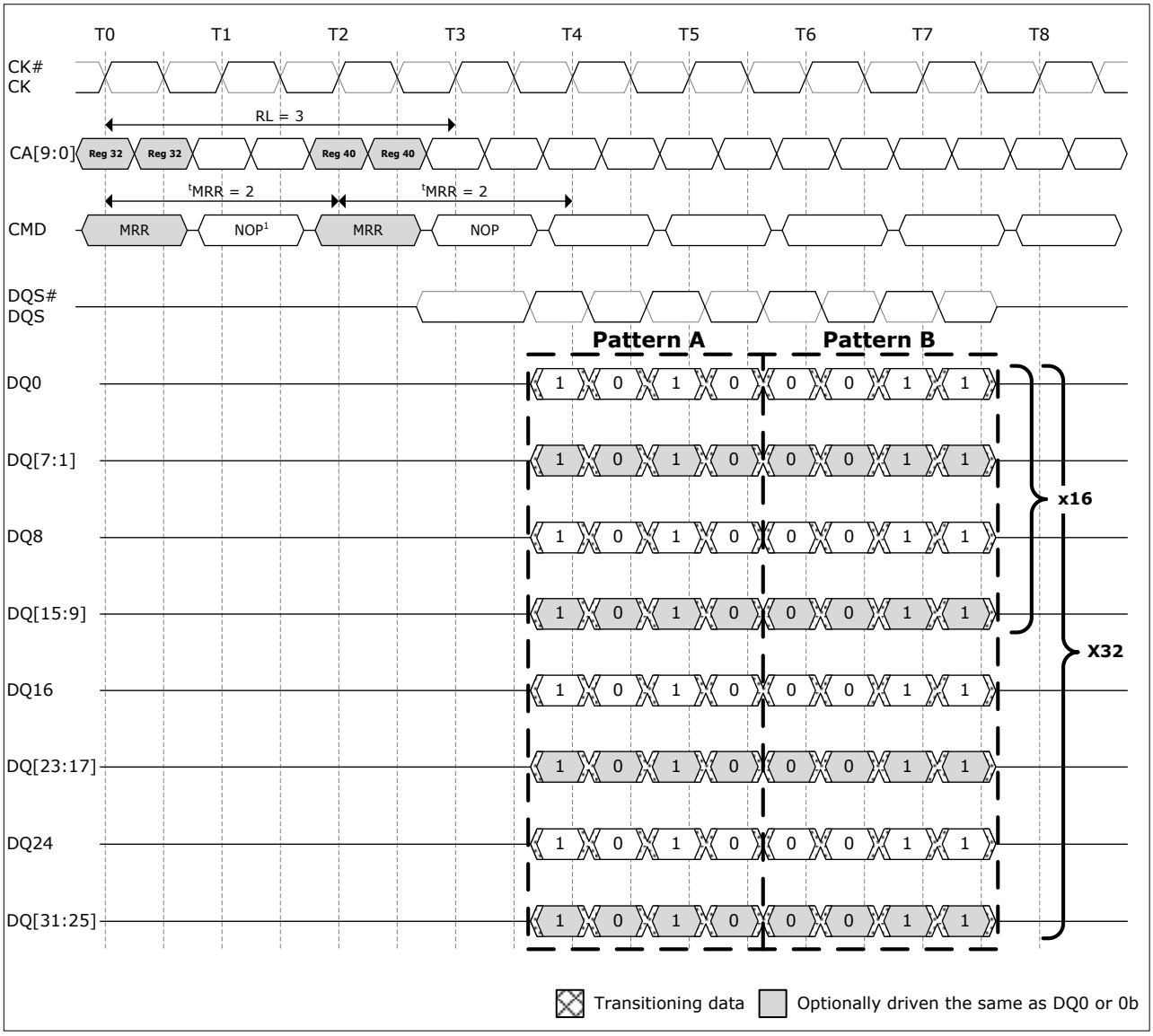


Figure 4.38 — MR32 and MR40 DQ Calibration timing example: RL = 3, tMRR = 2

NOTE 1 Mode Register Read has a burst length of four.
NOTE 2 Mode Register Read operation shall not be interrupted.
NOTE 3 Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
NOTE 4 For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
NOTE 5 The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period

4.12 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers.
The Mode Register Write (MRW) command is initiated by having CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

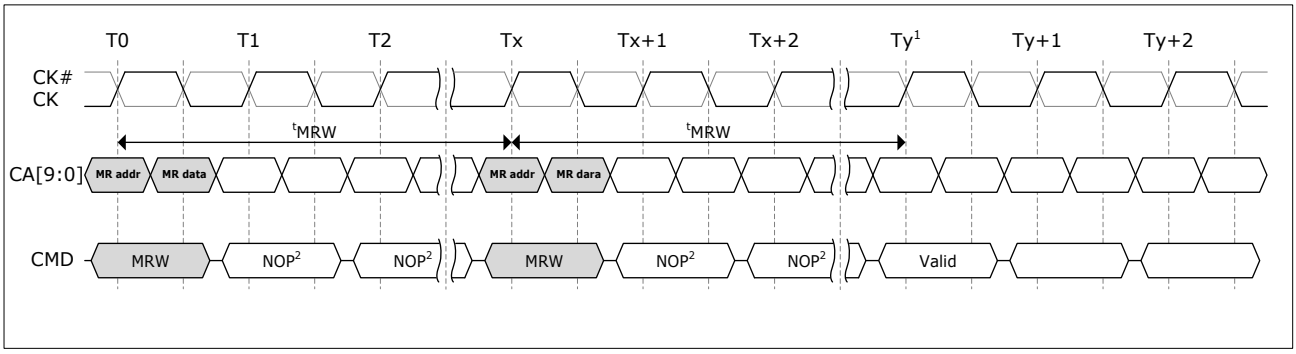


Figure 4.39 — Mode Register Write timing example: RL = 3, tMRW = 5

NOTE 1 The Mode Register Write Command period is tMRW. No command (other than Nop) is allowed during this period.
NOTE 2 At time Ty, the device is in the idle state.

4.12.1 Mode Register Write

For LPDDR2 devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

4.12.2 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence. The MRW Reset command may be issued from the Idle state for LPDDR2 devices. This command resets all Mode Registers to their default values..
No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period (**t**INIT4). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2 devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset.

4.12.3 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 ouput drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.
There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 for description on the command codes for the different ZQ Calibration commands.
The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.
The ZQReset Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.
One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities. For example, if TSens = 0.75% / oC, VSens = 0.20% / mV, Tdriftrate = 1 oC / sec and

Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as

$$\frac{1.5}{(0.75\times1)+(0.20\times15)}=0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.
No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.
In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDD2. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See "Output Driver DC Electrical Characteristics without ZQ Calibration")

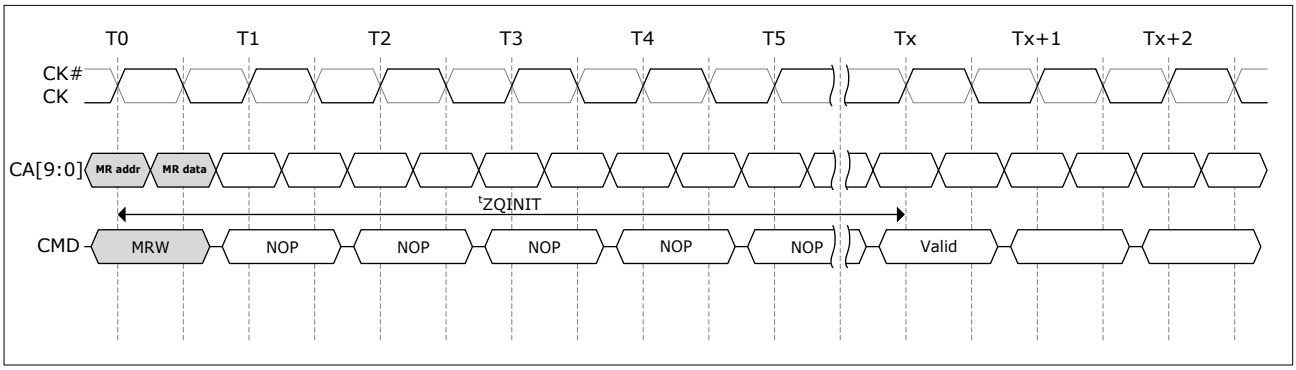


Figure 4.40 — ZQ Calibration Initialization timing example

NOTE 1: The ZQ Calibration Initialization period is tZQINIT. No command (other than Nop) is allowed during this period.
NOTE 2: CKE must be continuously registered HIGH during the calibration period.
NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.

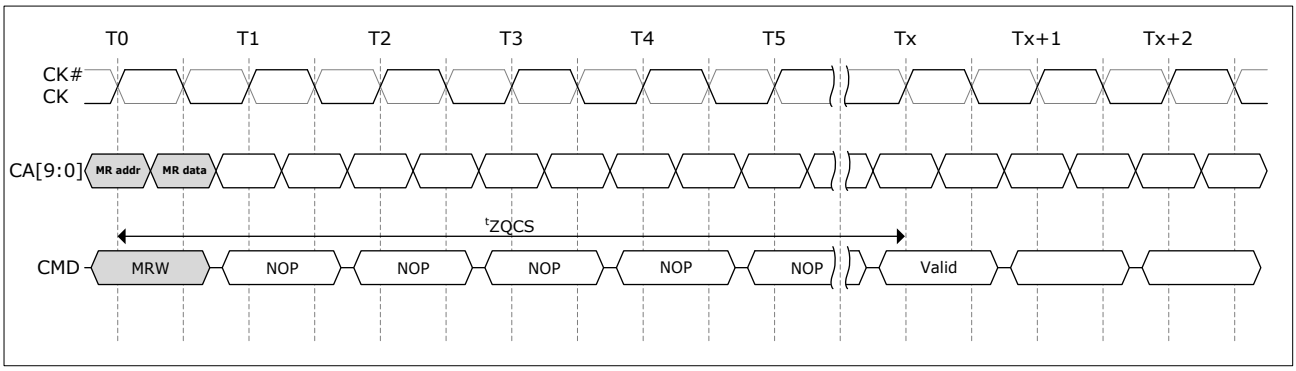


Figure 4.41 — ZQ Calibration Short timing example

NOTE 1: The ZQ Calibration Short period is tZQCS. No command (other than Nop) is allowed during this period.
NOTE 2: CKE must be continuously registered HIGH during the calibration period.
NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.

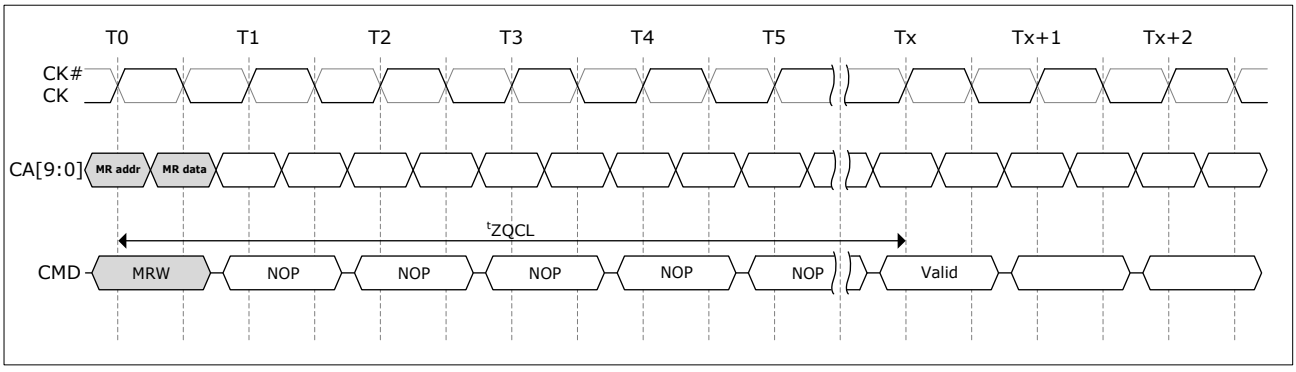


Figure 4.42 — ZQ Calibration Long timing example

NOTE 1 The ZQ Calibration Long period is tZQCL. No command (other than Nop) is allowed during this period.
NOTE 2 CKE must be continuously registered HIGH during the calibration period.
NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

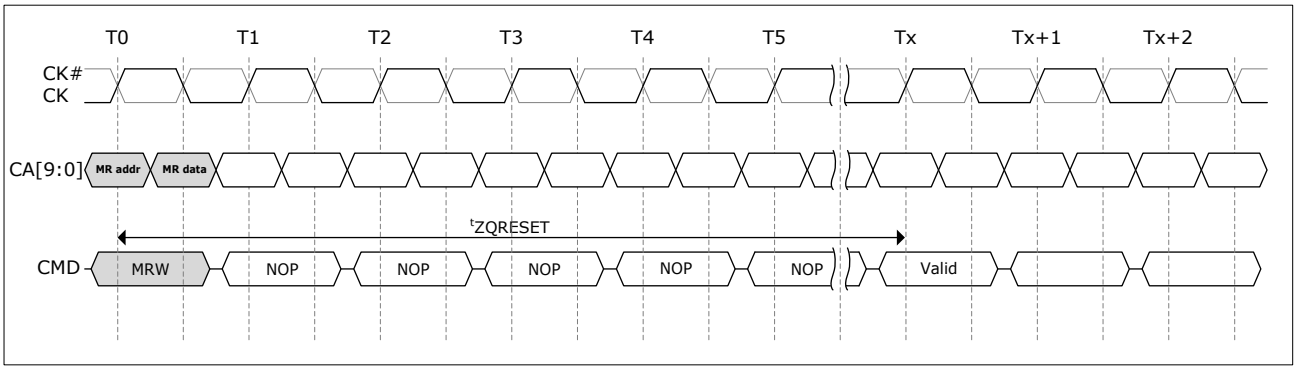


Figure 4.43 — ZQ Calibration Reset timing example

NOTE 1 The ZQ Calibration Reset period is tZQRESET. No command (other than Nop) is allowed during this peri
NOTE 2 CKE must be continuously registered HIGH during the calibration period.
NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

4.12.3.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See “Input/output capacitance”).

4.13 Power-down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS# HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, preactive, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.
Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until tCKE has been satisfied. VREF must be maintained at a valid level during power down.
VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See “Recommended DC Operating Conditions”).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section “LPDDR2 SDRAM Refresh Requirements” , as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.

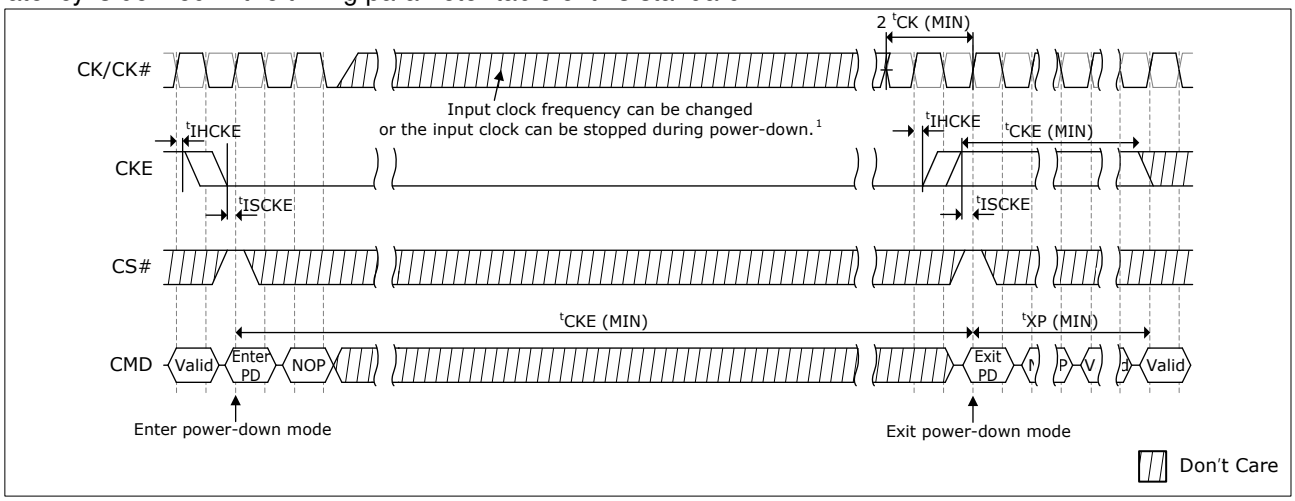


Figure 4.44 — Basic power down entry and exit timing diagram

NOTE 1 Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

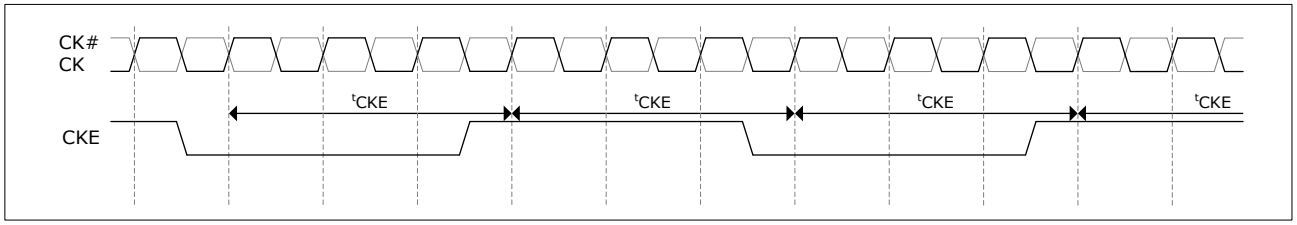


Figure 4.45 — Example of CKE intensive environment

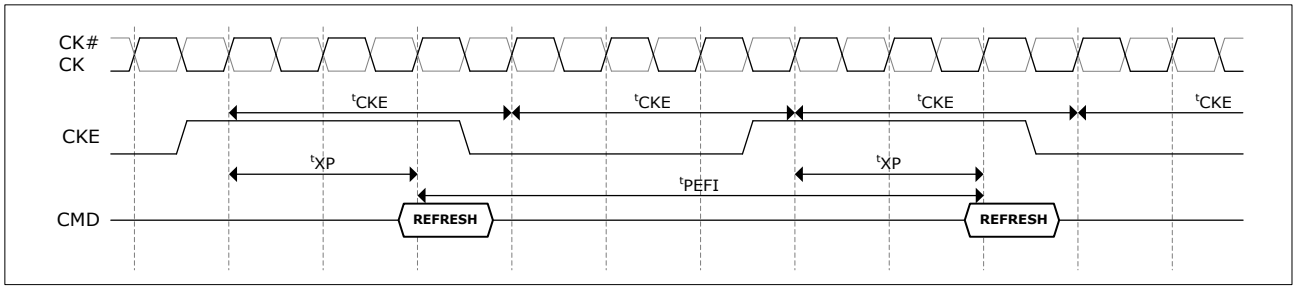


Figure 4.46 — REF to REF timing with CKE intensive environment for LPDDR2 SDRAM

NOTE 1 The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift

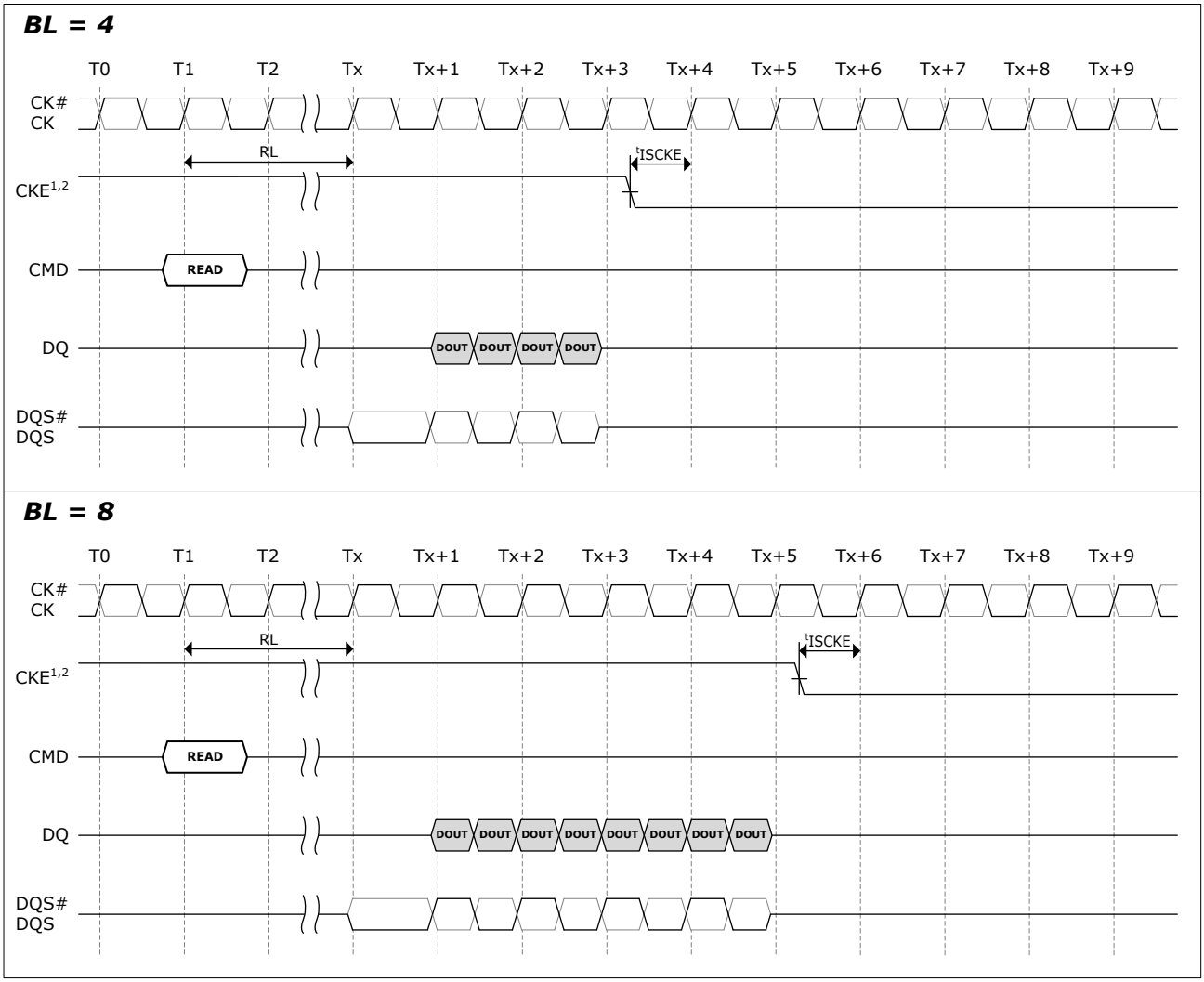


Figure 4.47 — Read to power-down entry

NOTE 1 CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.
NOTE 2 CKE must be held HIGH until the end of the burst operation.

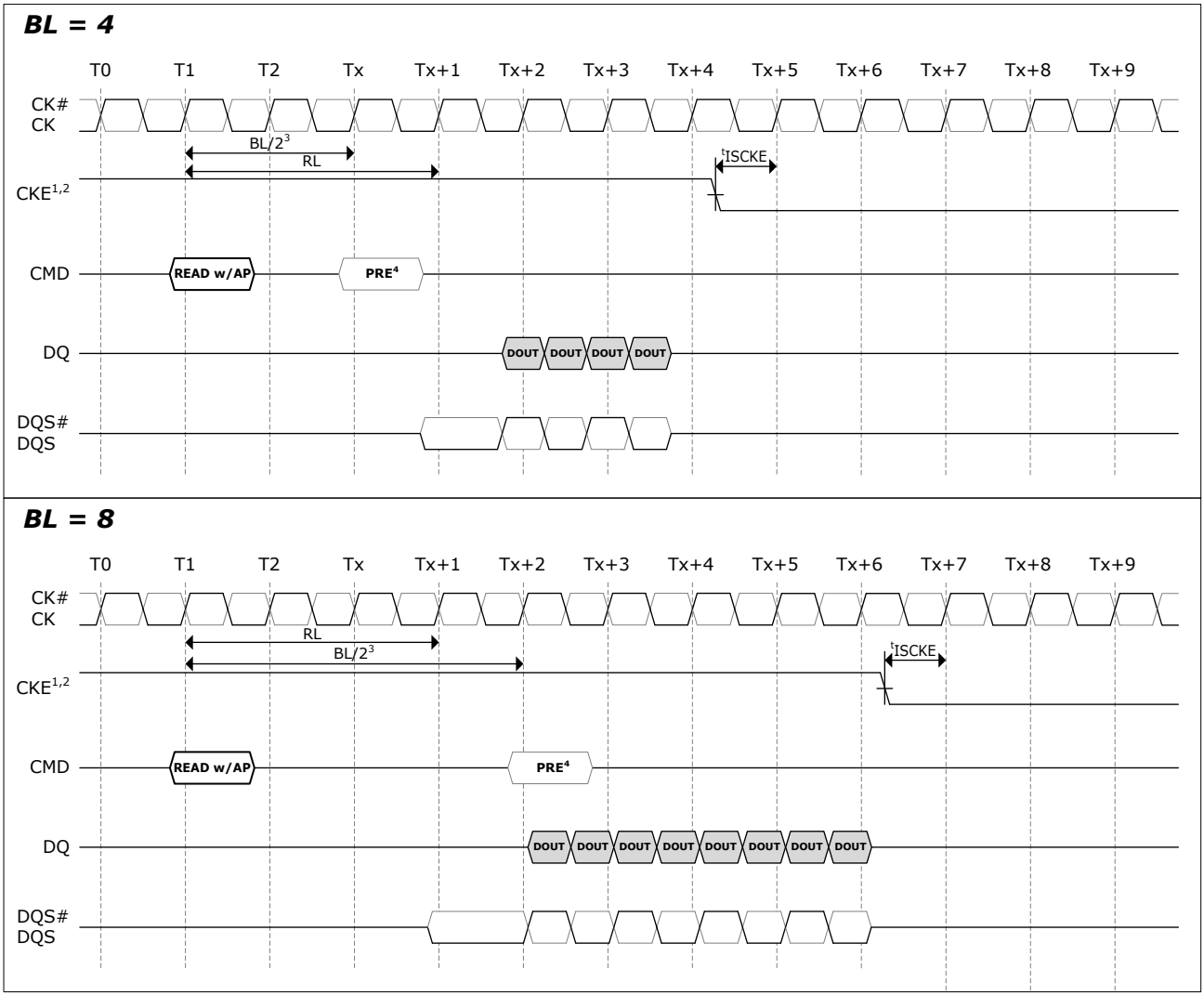


Figure 4.48 — Read with autoprecharge to power-down entry

NOTE 1 CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.
NOTE 2. CKE must be held HIGH until the end of the burst operation.
NOTE 3. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
NOTE 4. Start internal PRECHARGE.

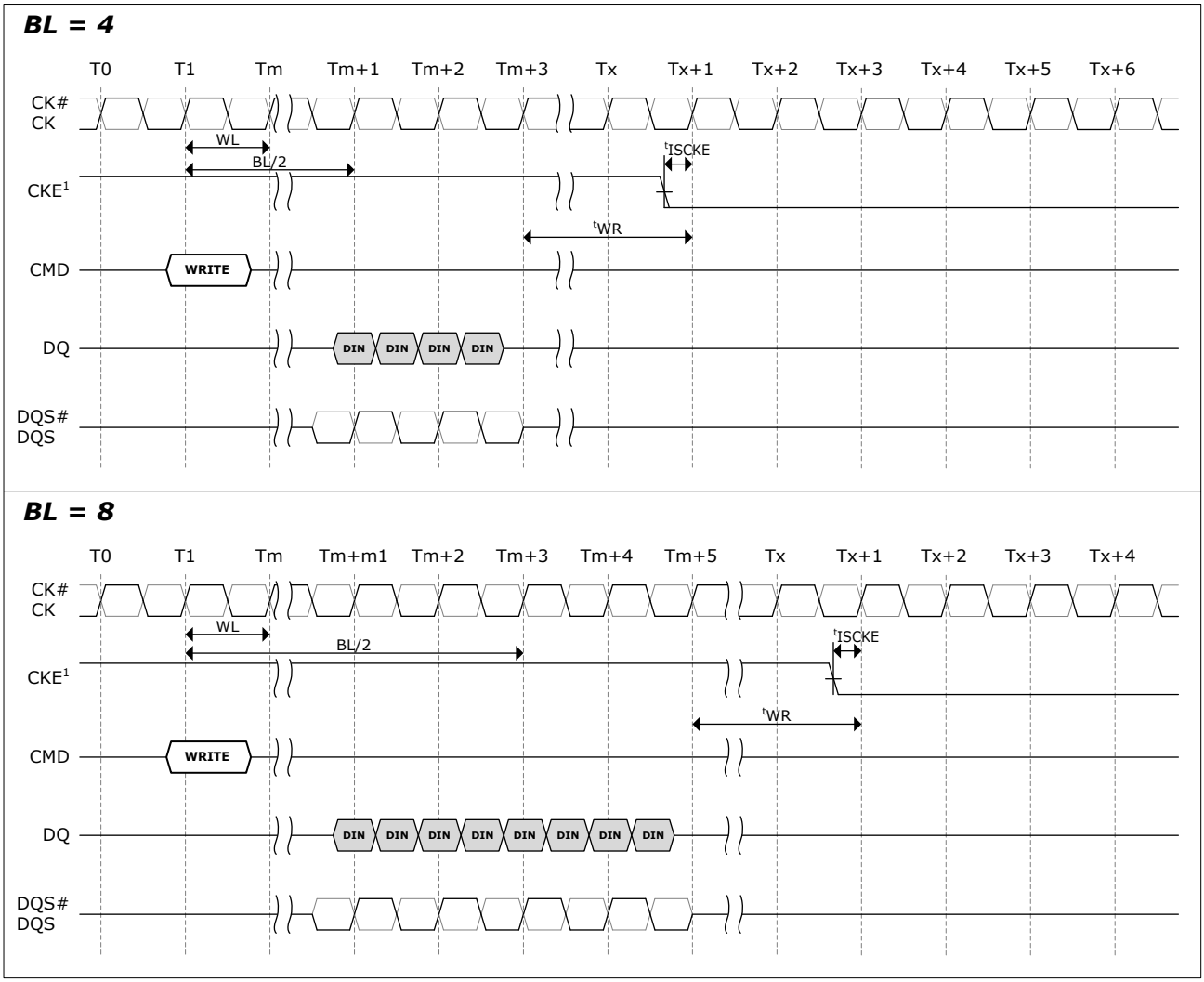


Figure 4.49 — Write to power-down entry

NOTE 1 CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the Write command is registered.

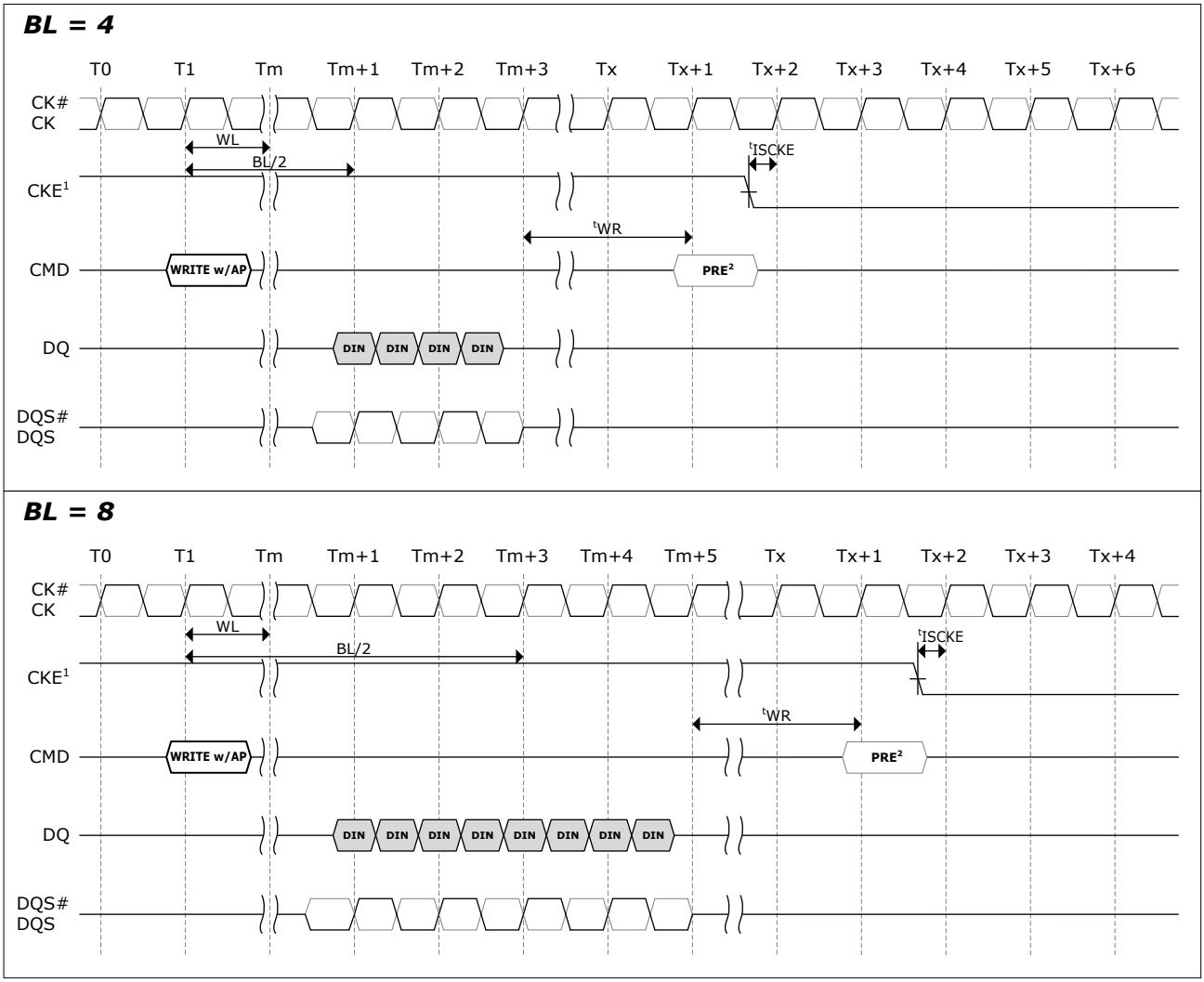


Figure 4.50 — Write with autoprecharge to power-down entry

NOTE 1 CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the Write command is registered.

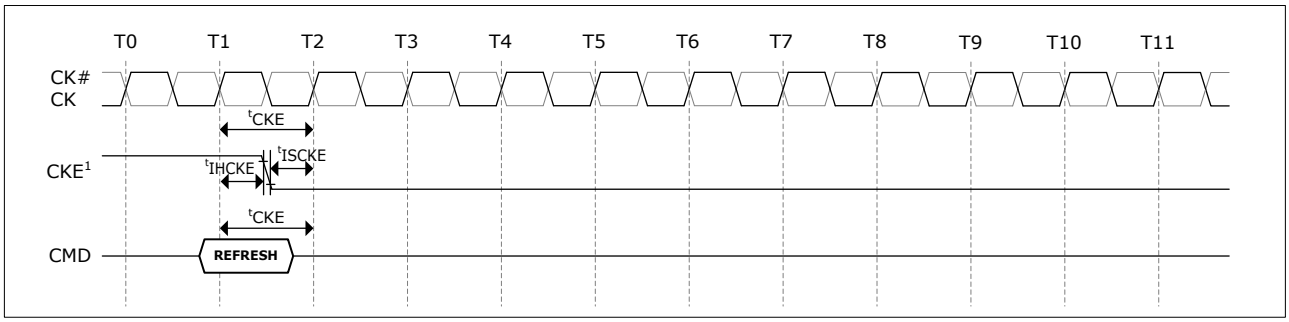


Figure 4.51 — Refresh command to power-down entry

NOTE 1 CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.

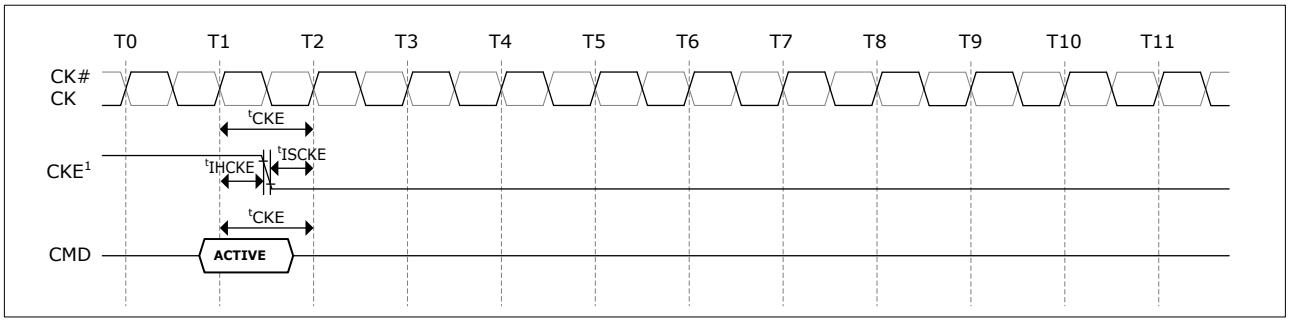


Figure 4.52 — Activate command to power-down entry

NOTE 1 CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

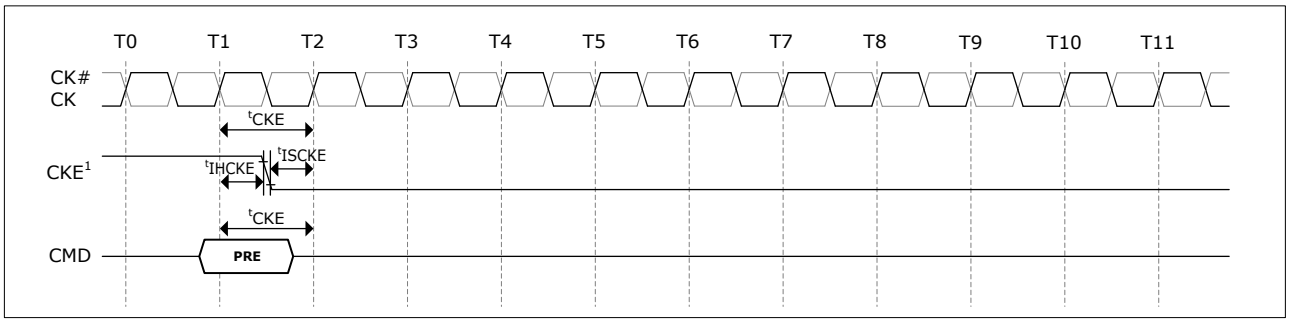


Figure 4.53 — Preactive/Precharge/Precharge-all command to power-down entry

NOTE 1 CKE may go LOW tIHCKE after the clock on which the Preactive/Precharge/Precharge-All command is registered.

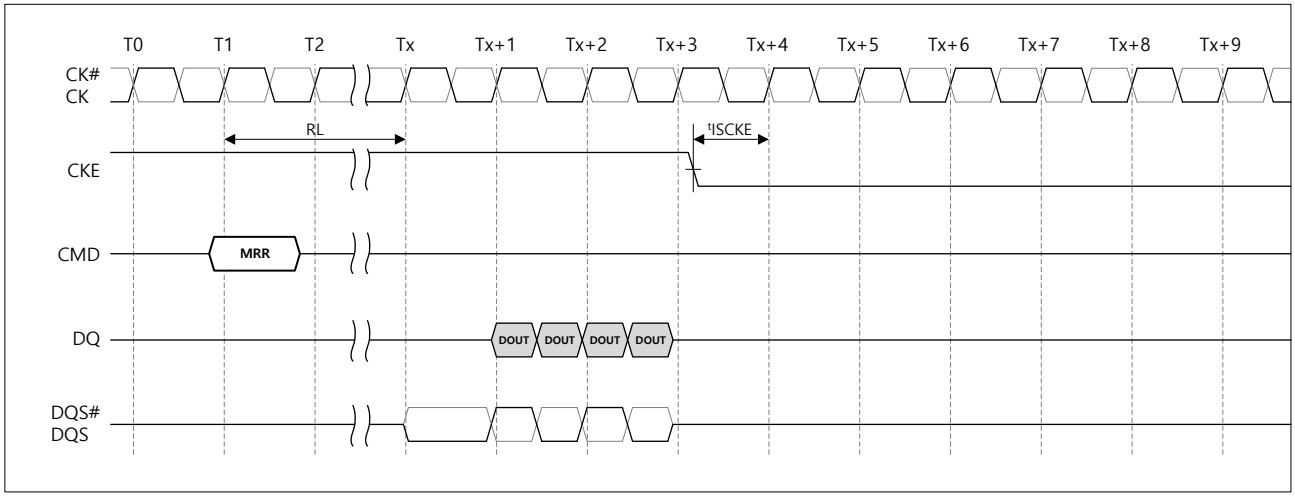


Figure 4.54 — Mode Register Read to power-down entry

NOTE 1 CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + 4/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

NOTE 2 Mode Register Read operation starts with a MRR command and CKE should be kept HIGH until the end of burst operation

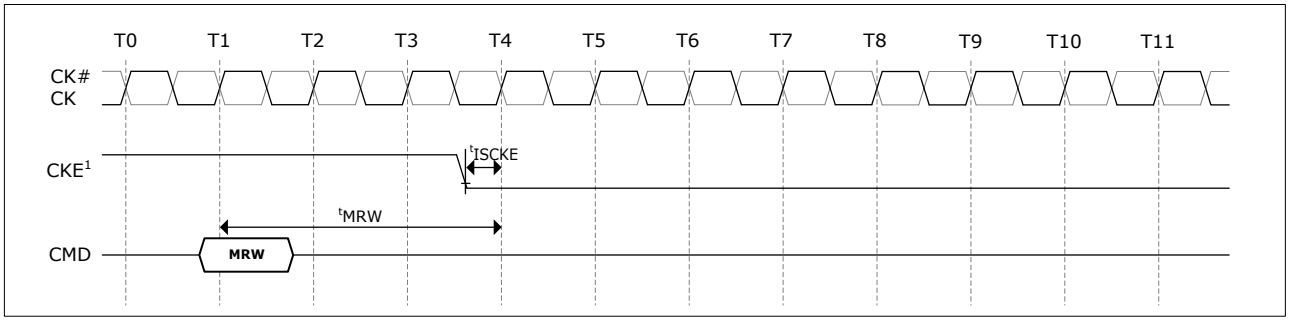


Figure 4.55 — MRW command to power-down entry

NOTE 1 CKE may be registered LOW tMRW after the clock on which the Mode Register Write command is registered

4.14 Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.

All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (See "Absolute Maximum DC Ratings"). However prior to exiting Deep Power-Down, Vref must be within specified limits (See "Recommended DC Operating Conditions").

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input.

The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence

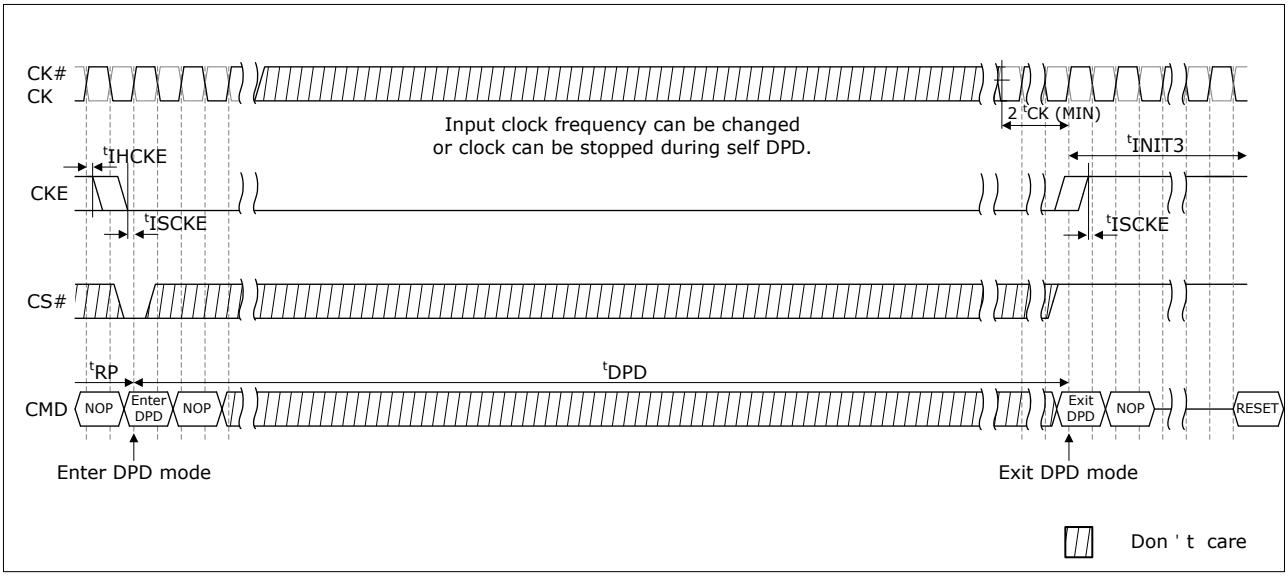


Figure 4.56 — Deep power down entry and exit timing diagram

NOTE 1 Initialization sequence may start at any time after Tc.

NOTE 2 tINIT3, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see 3.4.

NOTE 3 Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

4.15 Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:
• tCK(abs)min is met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• During clock frequency change, only REFab or REFpb commands may be executing;
• Any Activate, Preactive, or Precharge commands have executed to completion prior to changing the frequency;
• The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
• The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
• The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.
After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.
LPDDR2 devices support clock stop during CKE LOW under the following conditions:
• CK is held LOW and CK# is held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate, Preactive, or Precharge commands have executed to completion prior to stopping the clock;
• The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
• The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
• The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.
LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:
• tCK(abs)min is met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
• The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
• CS# shall be held HIGH during clock frequency change;
• During clock frequency change, only REFab or REFpb commands may be executing;
• The LPDDR2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.
After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc.
These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:
• CK is held LOW and CK# is held HIGH during clock stop;
• CS# shall be held HIGH during clock clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
• The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
• The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

4.16 No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS# HIGH at the clock rising edge N.
2. CS# LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

4.17 Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 14 — Command Truth Table

SDRAM	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK
Command	CK(n-1)	CK(n)												EDGE
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	X								↓
Refresh (per bank)*10	H	H	L	L	L	H	L	X						↑
				X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
				X										↓
Enter self Refresh	H	L	L	L	L	H	X							↑
				X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP3	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP3	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	X		BA0	BA1	BA2	↑
				X										↓
BST	H	H	L	H	H	L	L	X						↑
				X										↓
Enter Deep power Down	H	L	L	H	H	L	X							↑
				X										↓
NOP	H	H	L	H	H	H	X							↑
				X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	H	H	H	X							↑
				X										↓
NOP	H	H	H	X										↑
				X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
				X										↓
Enter Power Down	H	L	H	X										↑
				X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
				X										↓

Notes to Table 14

NOTE 1 All LPDDR2 commands are defined by states of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
NOTE 2 For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
NOTE 3 AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

NOTE 4 “X” means “H or L (but a defined logic level)”
NOTE 5 Self refresh exit and Deep Power Down exit are asynchronous.
NOTE 6 VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
NOTE 7 CAxr refers to command/address bit “x” on the rising edge of clock.
NOTE 8 CAxf refers to command/address bit “x” on the falling edge of clock.
NOTE 9 CS# and CKE are sampled at the rising edge of clock.
NOTE 10 Per Bank Refresh is only allowed in devices with 8 banks.
NOTE 11 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
NOTE 12 AB “high”during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

4.18 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

Table 15 – CKE Table

Device Current State *3	CKE_{n-1} *1	CKE_n *1	CS#*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep power down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE 1 “CKEn” is the logic state of CKE at clock rising edge n; “CKEn-1” was the state of CKE at the previous clock edge.
NOTE 2 “CS#” is the logic state of CS# at the clock rising edge n;
NOTE 3 “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
NOTE 4 “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
NOTE 5 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
NOTE 6 Power Down exit time (tXP) should elapse before a command other than NOP is issued.
NOTE 7 Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
NOTE 8 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
NOTE 9 The clock must toggle at least twice during the tXP period.
NOTE 10 The clock must toggle at least twice during the tXSR time.
NOTE 11 'X’ means ‘Don’t care’.
NOTE 12 Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired

Table 16 — Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	Active	Select and activate row	Active	
	Refresh(Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh(All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read Value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7,8
	Precharge	Deactivate row in bank or banks	Precharging	9,15
Row Active	Read	Select Column, and start read burst	Reading	
	Write	Select Column, and start write burst	Writing	
	MRR	Read Value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9

Reading	Read	Select Column, and start new read burst	Reading	10,11
	Write	Select Column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	Write	Select Column, and start write burst	Writing	10,11
	Read	Select Column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power on	Reset	Begin Device Auto-Initialization	Resetting	7,9
Resetting	MRR	Read Value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.
NOTE 2 All states and sequences not shown are illegal or reserved.
NOTE 3 Current State Definitions:

- Idle: The bank or banks have been precharged, and tRP has been met.
- Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accessesare in progress.
- Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 16, and according to Table 17.

- Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
- Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
- Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
- Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

- Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
- Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
- Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
- Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
- Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
- MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
- Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

NOTE 6 Bank-specific; requires that the bank is idle and no bursts are in progress.
NOTE 7 Not bank-specific; requires that all banks are idle and no bursts are in progress.
NOTE 8 Not bank-specific reset command is achieved through Mode Register Write command.
NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
NOTE 10 A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
NOTE 11 The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
NOTE 12 A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
NOTE 13 Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
NOTE 14 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
NOTE 15 If a Precharge command is issued to a bank in the Idle state, tRP shall still apply

Table 17 — Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Active	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10,11,13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8,16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8,15
	Write	Select column, and start write burst to Bank m	Writing	8,14,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8,15,16
	Write	Select column, and start write burst to Bank m	Writing	8,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12,17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

- Idle: the bank has been precharged, and tRP has been met.
- Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
- Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.

NOTE 5 A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.

NOTE 6 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

- Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
- Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
- Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
- MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

NOTE 7 tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

NOTE 8 Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 10 MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)

NOTE 11 MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.

NOTE 12 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 13 The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.

NOTE 14 A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to

asserting a Write command.
NOTE 15 Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Table 9 are followed.
NOTE 16 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
NOTE 17 Reset command is achieved through Mode Register Write command.
NOTE 18 BST is allowed only if a Read or Write burst is ongoing.

4.19 Data Mask Truth Table

Table 18 provides the data mask truth table.

Table 18 — DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data

5. Absolute Maximum Ratings

5.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS/ VSSCA	VDD2	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
storage Temperature	TSTG	-55	125	℃	5

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 See “Power-Ramp” section for relationships between power supplies.

NOTE 3 VREFDQ ≤ 0.6 x VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.

NOTE 4 VREFCA ≤ 0.6 x VDD2; however, VREFCA may be ≥ VDD2provided that VREFCA ≤ 300mV.

NOTE 5 Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device.
For the measurement conditions, please refer to JESD51-2 standard.

6. AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

6.1 Recommended DC Operating Conditions

Table 20 — Recommended LPDDR2-S4 DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.30	Core Power2 Input Buffer Power	V
VDDQ	1.14	1.20	1.30	I/O Buffer Power	V

NOTE 1 VDD1 uses significantly less power than VDD2

6.2 Input Leakage Current

Table 21 — Input Leakage Current

Parameter / Condition	Symbol	min	Max	Unit	Notes
Input Leakage current For CA, CKE, CS#, CK, CK# Any input 0 ≤ VIN ≤ VDD2 (All other pins not under test =0V	I_L	-2	2	uA	2
VREF supply leakage current VREFDQ = VDDQ/2 or VREFCA = VDD2/2 (All other pins not under test =0V)	IVREF	-1	1	uA	1

NOTE 1 The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS/DQS# output leakage specification.

6.3 Operating Temperature Range

Table 22 — Operating Temperature Range

Parameter / Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	℃

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
NOTE 2 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate , determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85℃ when the temperature sensor indicates a temperature of less than 85℃.

7. AC and DC Input Measurement Levels

7.1 AC and DC Logic Input Levels for Single-Ended Signals

7.1.1 AC and DC Input Levels for Single-Ended CA and CS# Signals

Table 23 — Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	LPDDR2-800		Unit	Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref +0.220	Note 2	V	1,2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1,2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDD2	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref -0.130	V	1
V_{refCA}(DC)	Reference Voltage for CA and CS# inputs	0.49 * VDD2	0.51 * VDD2	V	3,4

NOTE 1 For CA and CS# input only pins Vref = V_{refCA}(DC)
NOTE 2 See 8.5 Overshoot and Undershoot Specifications.
NOTE 3 The ac peak noise on VrefCA may not allow VrefCA to deviate from VrefCA(DC) by more than ± 1% VDD2 (for reference : approx. ±12mV)
NOTE 4 For reference : approx. VDD2/2 ±12mV

7.1.2 AC and DC Input Levels for CKE

Table 24 — Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE INPUT HIGH LEVEL	0.8* VDD2	Note 1	V	1
V_{ILCKE}	CKE INPUT LOW LEVEL	Note 1	0.2 * VDD2	V	1

NOTE 1 See 8.5 Overshoot and Undershoot Specifications.

7.1.3 AC and DC Input Levels for Single-Ended Data Signals

Table 25 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		Unit	Notes
		Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref +0.220	Note 2	V	1,2
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1,2
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref -0.130	V	1
V_{refDQ}(DC)	Reference Voltage for DQ , DM inputs	0.49 * VDDQ	0.51 * VDDQ	V	3,4

NOTE 1 For DQ input only pins Vref = VrefDQ(DC)
NOTE 2 See 8.5 Overshoot and Undershoot Specifications.
NOTE 3 The ac peak noise on VrefDQ may not allow VrefDQ to deviate from VrefDQ(DC) by more than ± 1% VDDQ (for reference : approx. ±12mV)
NOTE 4 For reference : approx. VDDDQ/2 ±12mV

7.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in Figure 7.1. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise). VDD stands for VDD2 for VRefCA and VDDQ for VRefDQ. VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDD2 also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 24. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDD2 if this would send Vref outside these specifications

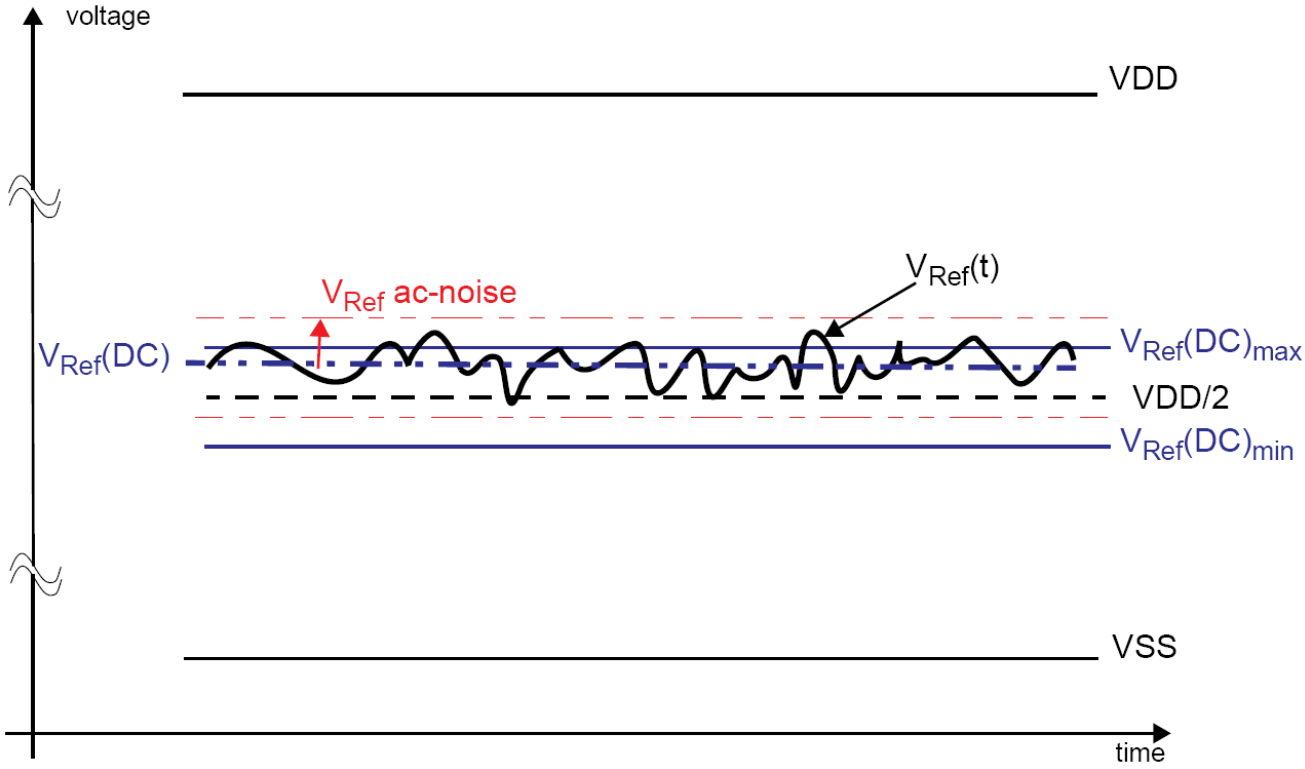


Figure 7.1 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef. "VRef " shall be understood as VRef(DC), as defined in Figure 7.1.

This clarifies that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as VREF is maintained between 0.44 x VDDQ (or VDD2) and 0.56 x VDDQ (or VDD2) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VREF (see the Single-Ended AC and DC Input Levels for CA and CS# Inputs Table and Single-Ended AC and DC Input Levels for DQ and DM.) Therefore, system timing and voltage budgets need to account for VREF deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

7.3 Input Signal

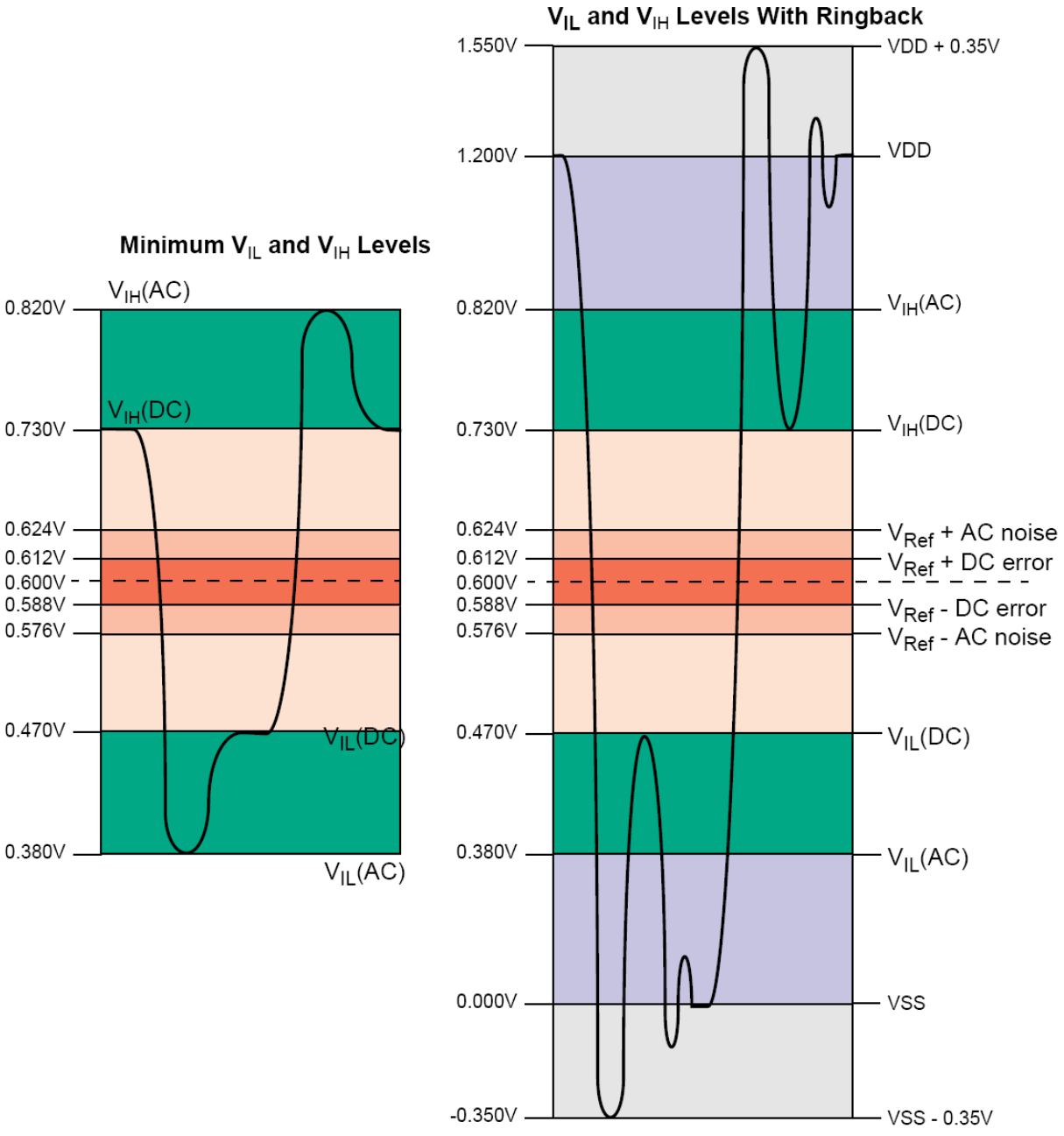


Figure 7.2 — LPDDR2-466 to LPDDR2-1066 Input Signal

NOTE 1 Numbers reflect nominal values.
NOTE 2 For CA0-9, CK, CK#,and CS#, VDD stands for VDD2. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
NOTE 3 For CA0-9, CK, CK#, and CS#, VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.

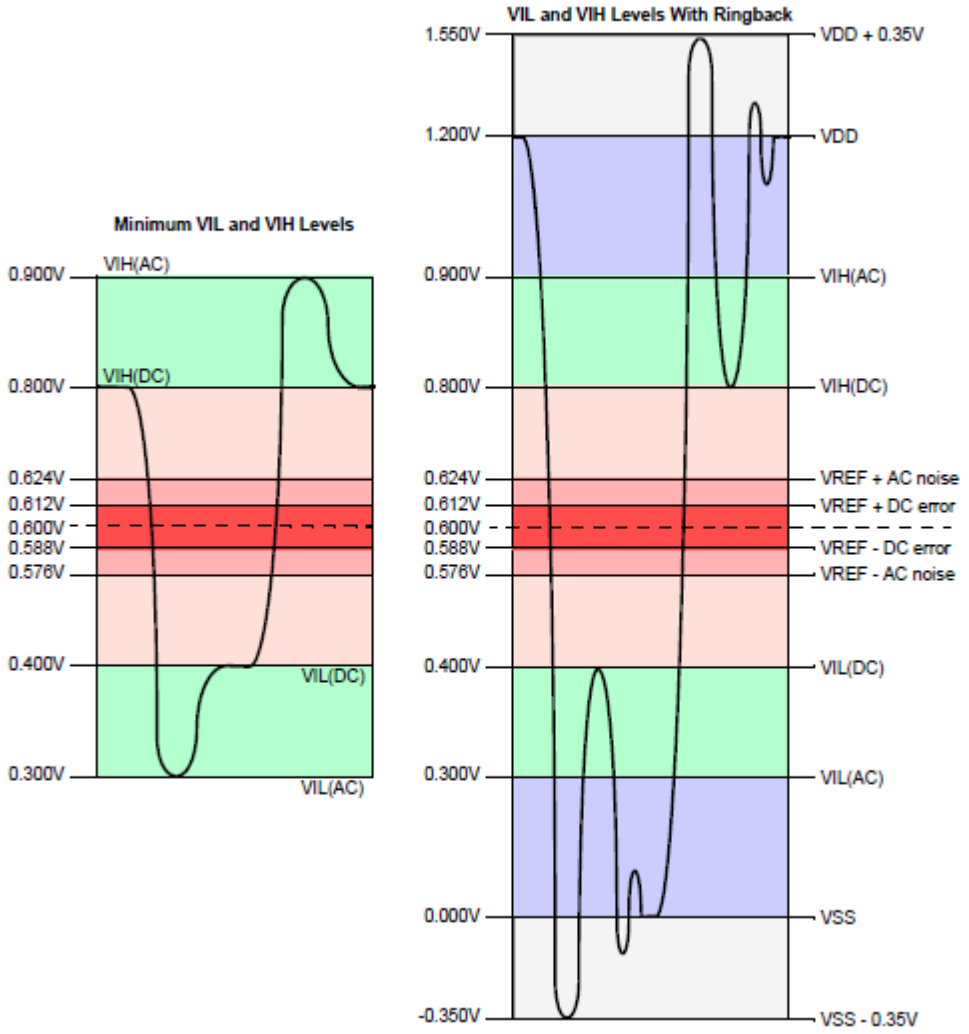


Figure 7.3 — LPDDR2-200 to LPDDR2-400 Input Signal

NOTE 1 Numbers reflect nominal values
NOTE 2 For CA0-9, CK, CK#, and CS#, VDD stands for VDD2. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
NOTE 3 For CA0-9, CK, CK#, and CS#, VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.

7.4 AC and DC Logic Input Levels for Differential Signals

7.4.1 Differential signal definition

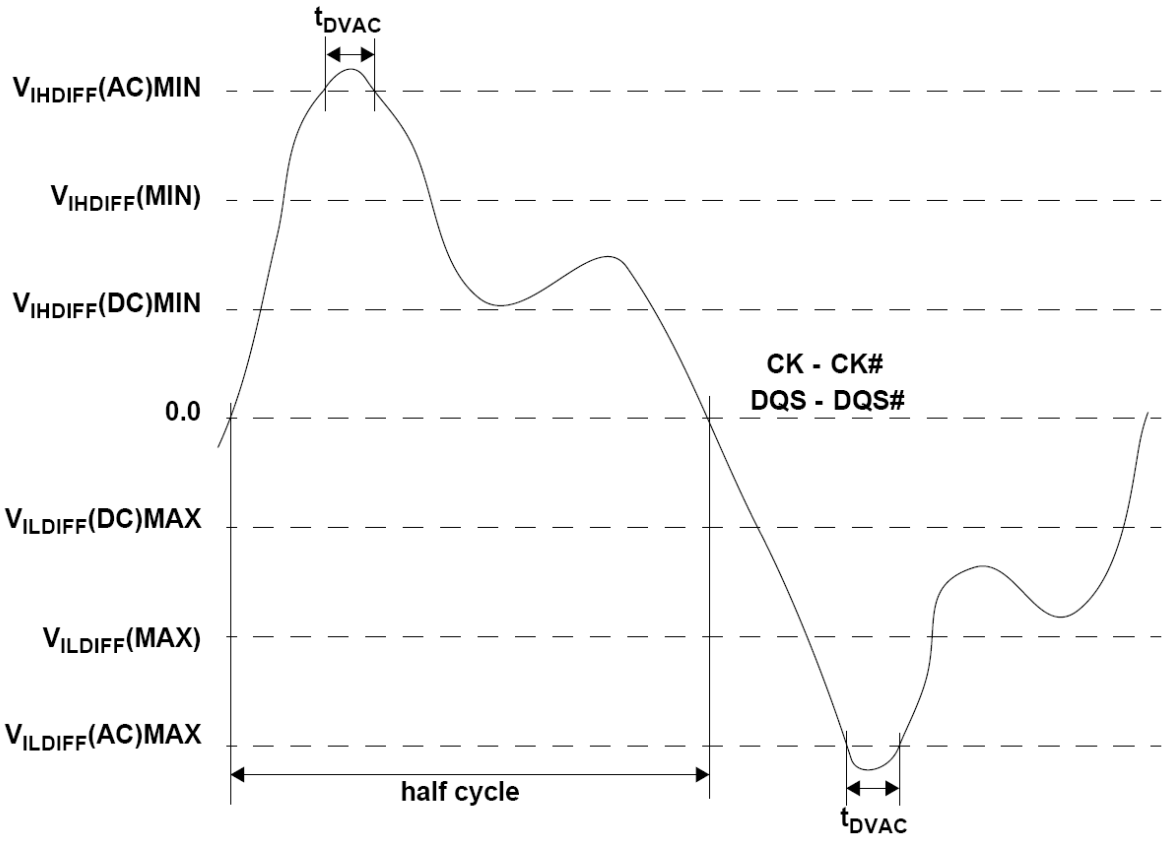


Figure 7.4 — Definition of differential ac-swing and "time above ac-level" tDVAC

7.4.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Table 26 — Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
V_{IHdiff}(DC)	Differential input high	2 x (VIH(DC)-Vref)	Note 3	2 x (VIH(DC)-Vref)	Note 3	V	1
V_{ILdiff}(DC)	Differential input low	Note 3	2 x (VIL(DC)-Vref)	Note 3	2 x (VIL(DC)-Vref)	V	1
V_{IHdiff}(AC)	Differential input high ac	2 x (VIH(AC)-Vref)	Note 3	2 x (VIH(AC)-Vref)	Note 3	V	2
V_{ILdiff}(AC)	Differential input low ac	Note 3	2 x (VIL(AC)-Vref)	Note 3	2 x (VIL(AC)-Vref)	V	2

NOTE 1 Used to define a differential signal slew-rate. For CK - CK# use VIH/VIL(dc) of CA and VREFCA ; for DQS - DQS#, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
NOTE 2 For CK - CK# use VIH/VIL(ac) of CA and VREFCA; for DQS - DQS#, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
NOTE 3 These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot Specifications"
NOTE 4 For CK and CK#, Vref = VrefCA(DC). For DQS and DQS#, Vref = VrefDQ(DC).

Table 27 — Allowed time before ring back (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/ns]	tDVAC [ps] @|VIH/Ldiff(ac)| =440mV	tDVAC [ps] @|VIH/Ldiff(ac)| =600mV
	Min	Min
>4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
<1.0	150	0

7.4.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, CK#, or DQS#) has also to comply with certain requirements for single-ended signals.
CK and CK# shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.
DQS, DQS# shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.
Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

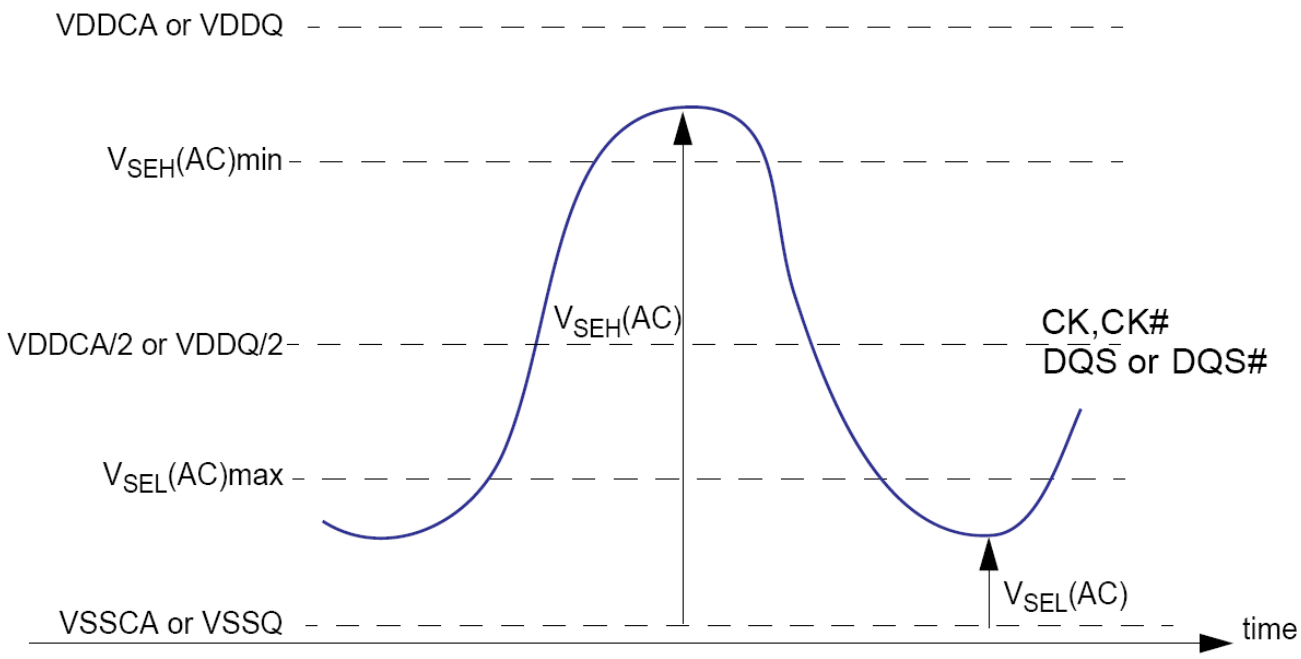


Figure 7.5 — Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS, DQS# and VDD2/2 for CK, CK#; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The Single-ended requirements for CK, CK#, DQS, and DQS# are found in tables 23 and Single-ended AC and DC Input Levels for DQ and DM in tables 25, respectively.

Table 28 — Single-ended levels for CK, DQS, CK#, DQS#

Symbol	Parameter	LPDDR2-800		Unit	Notes
		Min	Max		
VSEH(AC)	Single-ended high-level for strobes	(VDDQ/2) +0.220	Note 3	V	1,2
	Single-ended high-level for CK, CK#	(VDD2/2) +0.220	Note 3	V	1,2
VSEL(AC)	Single-ended low-level for strobes	Note 3	(VDDQ/2) - 0.220	V	1,2
	Single-ended low-level for CK, CK#	Note 3	(VDD2/2) - 0.220	V	1,2

NOTE 1 For CK, CK# use VSEH/VSEL(AC) of CA; for strobes (DQS0, DQS0#, DQS1, DQS1#, DQS2, DQS2#, DQS3, DQS3#) use VIH/VIL(AC) of DQs.

NOTE 2 VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, however the single-ended signals CK, CK#, DQS0, DQS0#, DQS1, DQS1#, DQS2, DQS2#, DQS3, DQS3# need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Refer to Overshoot and Undershoot Specifications”

7.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 28. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

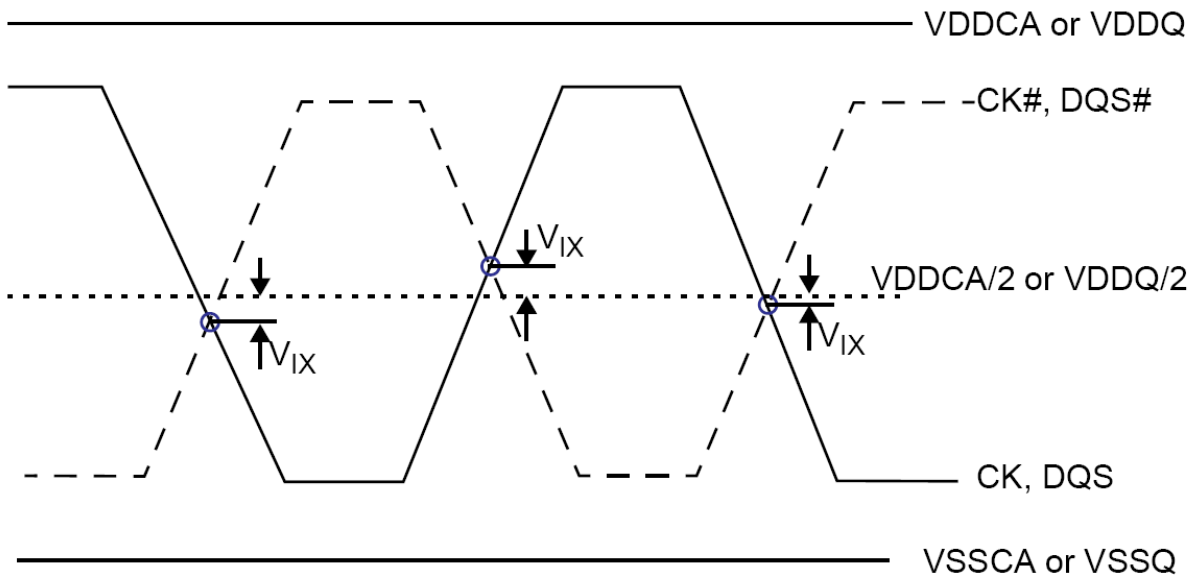


Figure 7.6 — Vix Definition

Table 29 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-800		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to VDD2/2 for CK, CK#	-120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS, DQS#	-120	120	mV	1,2

NOTE 1 The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
NOTE 2 For CK and CK#, Vref = VrefCA(DC). For DQS and DQS#, Vref = VrefDQ(DC).

7.6 Slew Rate Definitions for Single-Ended Input Signals

See “CA and CS# Setup, Hold and Derating” for single-ended slew rate definitions for address and command signals.
See “Data Setup, Hold and Slew Rate Derating” for single-ended slew rate definitions for data signals.

7.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table 30 and Figure 7.7.

Table 30 — Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - CK# and DQS - DQS#)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge (CK - CK# and DQS - DQS#)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff

NOTE 1 The differential signal (i.e. CK - CK# and DQS - DQS#) must be linear between these thresholds

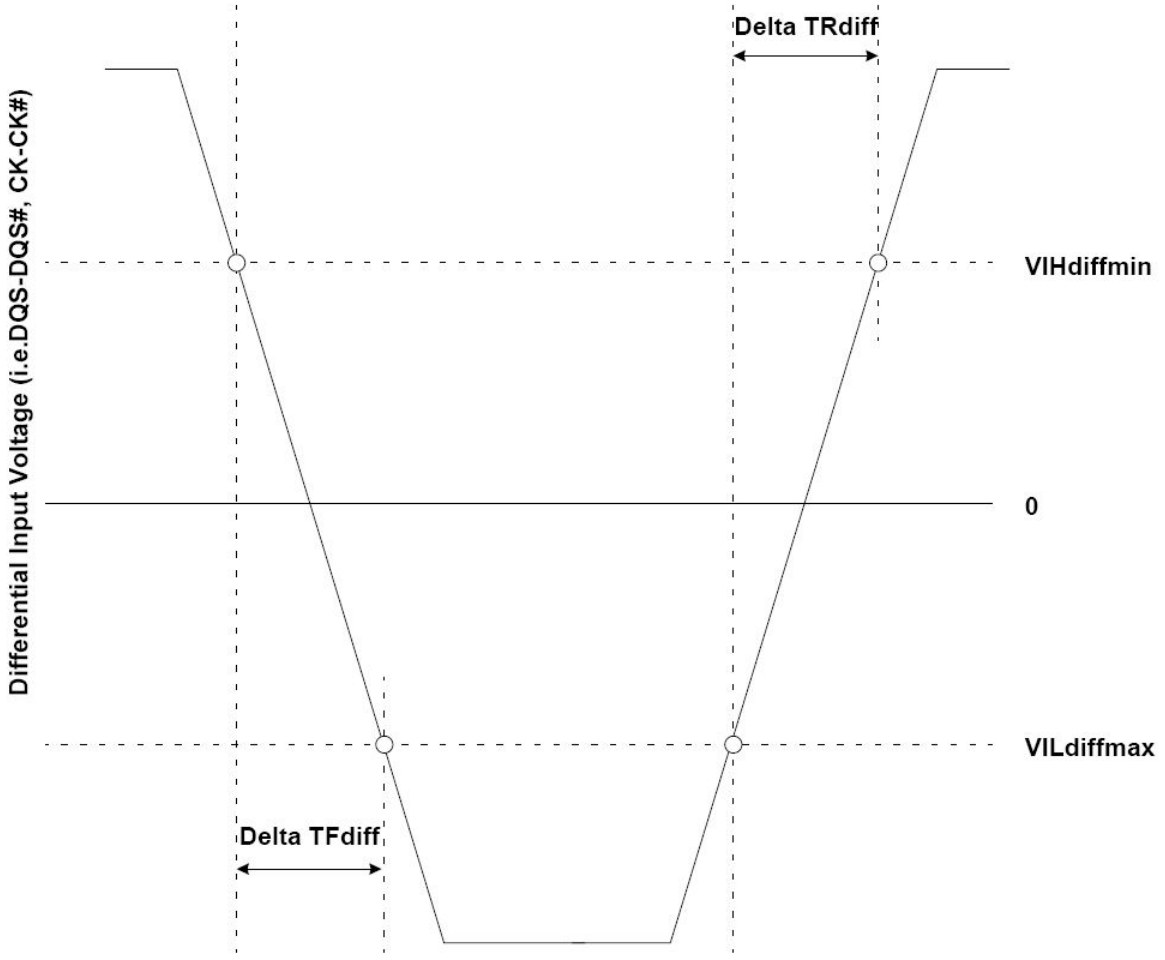


Figure 7.7 — Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

8. AC and DC Output Measurement Levels

8.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

Table 31 — Single-ended AC and DC Output Levels

Symbol	Parameter		LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x VDDQ	V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)		0.1 x VDDQ	V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		VREFDQ + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		VREFDQ - 0.12	V	
I_{OZ}	Output Leakage Current (DQ, DM, DQS, DQS#)	Min	-5	uA	
	DQS are disabled ; 0V ≤ VOUT ≤ VDDQ	Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE 1 IOH = -0.1mA.
NOTE 2 IOL = 0.1mA

8.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of diffential signals (DQS, DQS#).

Table 32 — Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OHdiff(DC)}$	AC differential output high measurement level (for output SR)	+0.20 x VDDQ	V	1
$V_{OLdiff(DC)}$	AC differential output low measurement level (for output SR)	-0.20 x VDDQ	V	2

NOTE 1 IOH = -0.1mA.
NOTE 2 IOL = 0.1mA

8.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 33 and Figure 8.1.

Table 33 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse

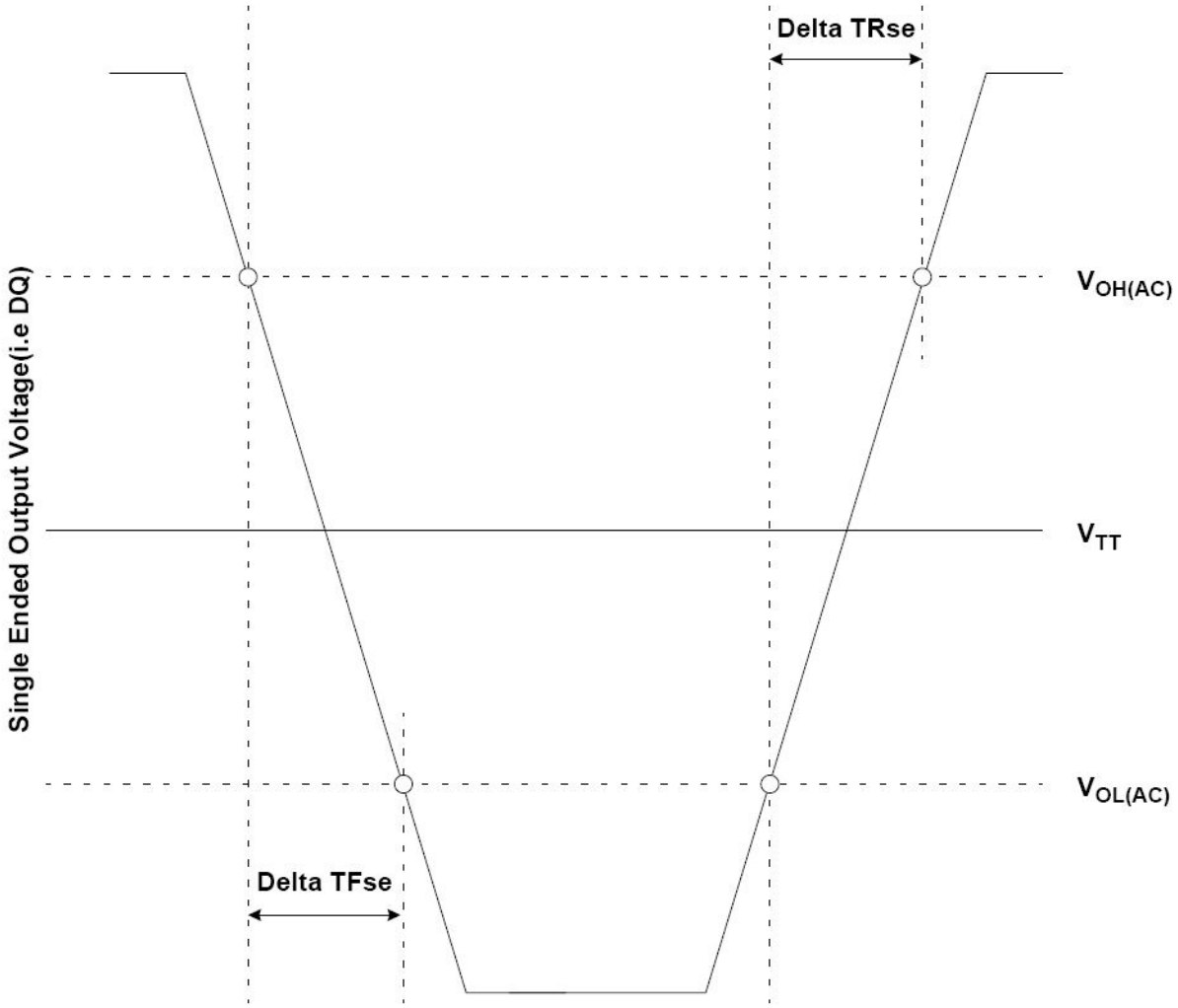


Figure 8.1 — Single Ended Output Slew Rate Definition

Table 34 — Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-800		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40Ω ± 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω ± 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description

SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals

NOTE 1 Measured with output reference load.
NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
NOTE 4 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

8.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 35 and Figure 8.2

Table 35 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate to rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / Delta TRdiff
Differential output slew rate to falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / Delta TFdiff

NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.

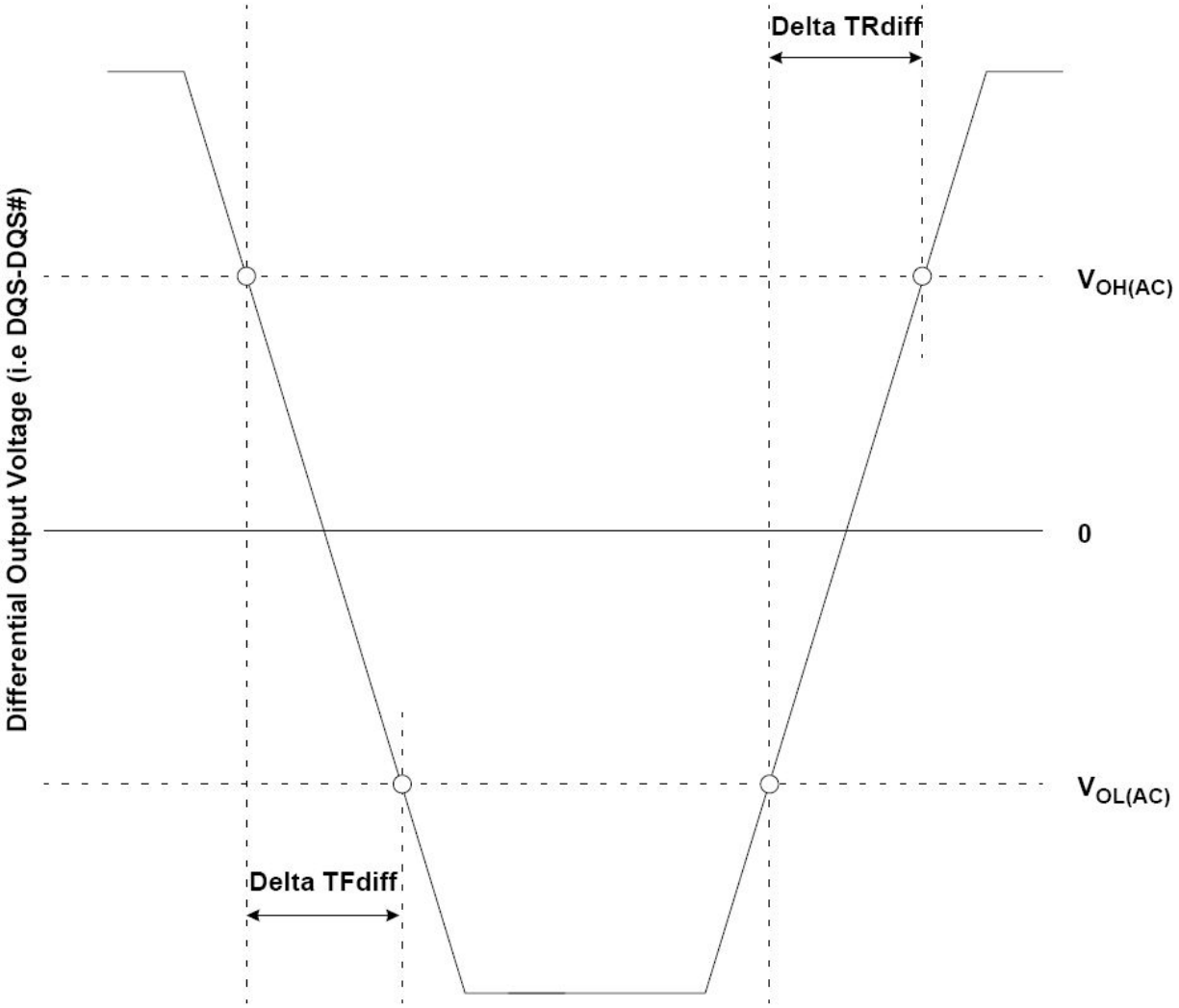


Figure 8.2 — Differential Output Slew Rate Definition

Table 36 — Differential Output Slew Rate

Parameter	Symbol	LPDDR2-1066 to LPDDR2-667		Units
		Min	Max	
Differential Output Slew Rate (RON = 40Ω ± 30%)	SRQse	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω ± 30%)	SRQse	2.0	5.0	V/ns

Description

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff : Differential Signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).

NOTE 3 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

8.5 Overshoot and Undershoot Specifications

Table 37 — AC Overshoot/Undershoot Specification

Parameter		LPDDR2-800	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 8.3)	Max	0.35	V
Maximum peak amplitude allowed for undershoot area (See Figure 8.3)	Max	0.35	V
Maximum area above VDD. (See Figure 8.3)	Max	0.20	V-ns
Maximum area below VSS. (See Figure 8.3)	Max	0.20	V-ns

(CA0-9, CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM)

NOTE 1 For CA0-9, CK, CK#, CS#, and CKE, VDD stands for VDD2. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.

NOTE 2 For CA0-9, CK, CK#, CS#, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.

NOTE 3 Values are referenced from actual VDDQ, VDD2, VSSQ and VSSCA levels.

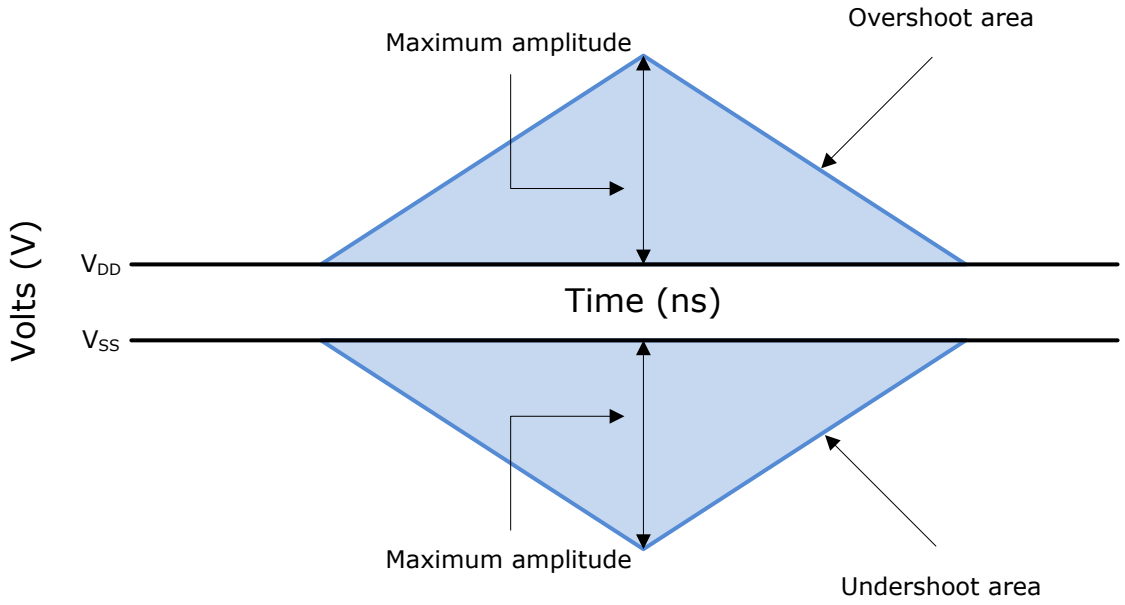


Figure 8.3 — Overshoot and Undershoot Definition

NOTE 1 For CA0-9, CK, CK#, CS#, and CKE, VDD stands for VDD2. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
NOTE 2 For CA0-9, CK, CK#, CS#, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.
NOTE 3 Maximum peak amplitude values are referenced from actual VDD and VSS values.
NOTE 4 Maximum area values are referenced from maximum operating VDD and VSS values.

8.6 Output buffer characteristics

8.6.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

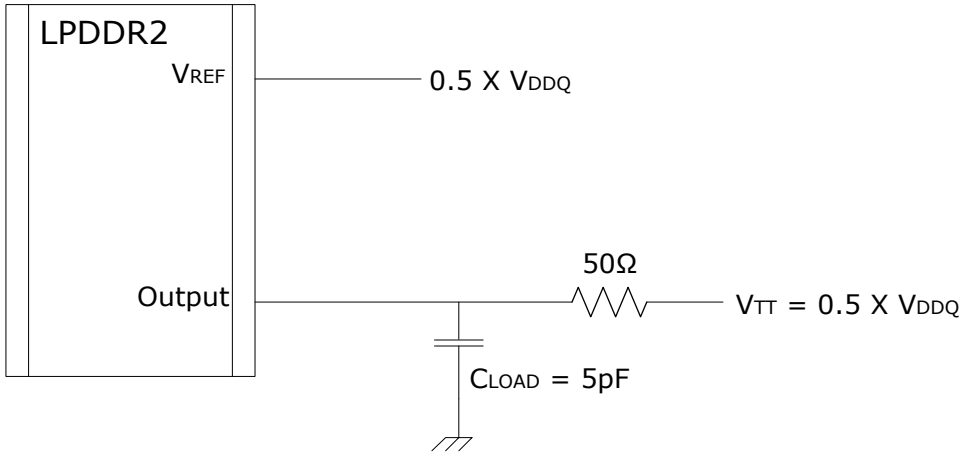


Figure 8.4 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE 1: All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

8.7 RONPU and RONPD Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE 1: This is under the condition that RONPD is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE 1: This is under the condition that RONPU is turned off

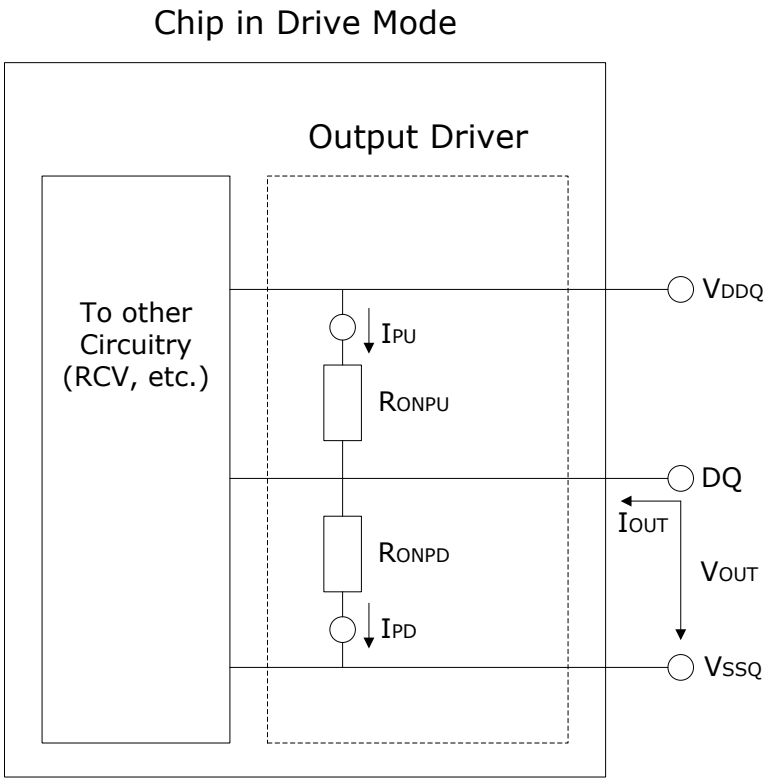


Figure 8.5 — Output Driver: Definition of Voltages and Currents

8.7.1 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table 38 — Output Driver DC Electrical Characteristics with ZQ Calibration

RONNOM	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3 Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0 Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0 Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0 Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0 Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0 Ω (Optional)	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between Pull-up and Pull-down	MMPUPD		-15.00		15.00	%	1,2,3,4,5

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2 RZQ = 240 .

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.

NOTE 5 Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

8.7.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 39 — Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	85 - (*dRONdT* x |ΔV|) - (*dRONdV* x|ΔV|)	115 + *(dRONdT* x |ΔV|) + (*dRONdV* x|ΔV|)	%	1,2
RONPU					

NOTE 1 $\Delta T = T - T$(@ calibration), $\Delta V = V - V$(@ calibration)

NOTE 2 dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 40 — Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	%/ ℃	
dRONdV	RON Voltage Sensitivity	0.00	0.75	%/ mV	

8.7.3 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 41 — Output Driver DC Electrical Characteristics without ZQ Calibration

RONNOM	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3 Ω	RON34PD	0.5 x VDDQ	24.0	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24.0	34.3	44.6	Ω	1
40.0 Ω	RON40PD	0.5 x VDDQ	28.0	40.0	52.0	Ω	1
	RON40PU	0.5 x VDDQ	28.0	40.0	52.0	Ω	1
48.0 Ω	RON48PD	0.5 x VDDQ	33.6	48.0	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48.0	62.4	Ω	1
60.0 Ω	RON60PD	0.5 x VDDQ	42.0	60.0	78.0	Ω	1
	RON60PU	0.5 x VDDQ	42.0	60.0	78.0	Ω	1
80.0 Ω	RON80PD	0.5 x VDDQ	56.0	80.0	104.0	Ω	1
	RON80PU	0.5 x VDDQ	26.0	80.0	104.0	Ω	1
120.0 Ω (Optional)	RON120PD	0.5 x VDDQ	84.0	120.0	156.0	Ω	1
	RON120PU	0.5 x VDDQ	84.0	120.0	156.0	Ω	1

NOTE 1 Across entire operating temperature range, without calibration.

8.7.4 RZQ I-V Curve

Table 42 — RZQ I-V Curve

Voltage [V]	RON = 240 Ω (RZQ)							
	Pull -Down				Pull -Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	Default value after ZQReset		With Calibration		Default value after ZQReset		With Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

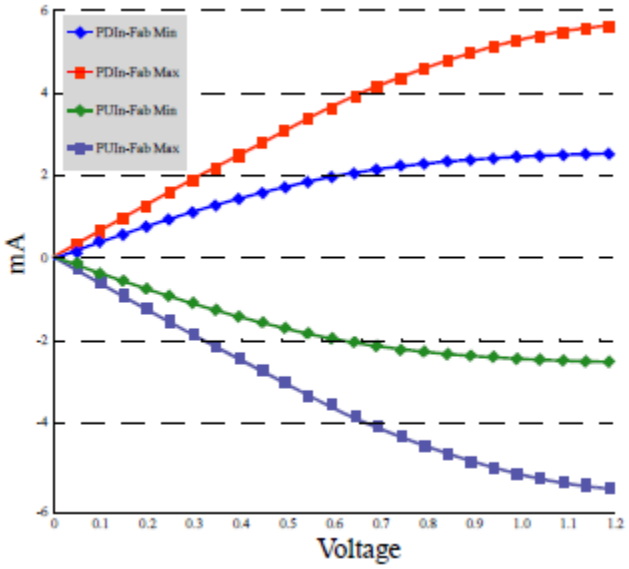


Figure 8.6 — RON = 240 Ohms
IV Curve after ZQReset

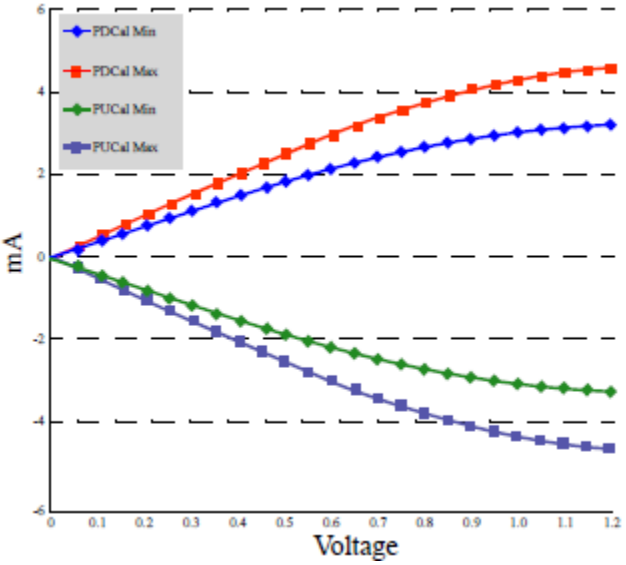


Figure 8.7 — RON = 240 Ohms
IV Curve after calibration

9. Input/Output Capacitance

9.1 Input/Output Capacitance

Table 43 — Input/output capacitance

Parameter	Symbol		LPDDR2	Units	Notes
Input capacitance, CK and CK#	CCK	Min	1.00	pF	1,2
		Max	3.00	pF	1,2
Input capacitance delta, CK and CK#	CDCK	Min	0.00	pF	1,2,3
		Max	0.20	pF	1,2,3
Input capacitance, All other input -only pins	CI	Min	1.00	pF	1,2,4
		Max	3.00	pF	1,2,4
Input capacitance delta, All other input -only pins	CDI	Min	-0.50	pF	1,2,5
		Max	0.50	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, DQS#	CIO	Min	1.25	pF	1,2,6,7
		Max	3.50	pF	1,2,6,7
Input/output capacitance delta, DQS, DQS#	CDDQS	Min	0.00	pF	1,2,7,8
		Max	0.25	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.50	pF	1,2,7,9
		Max	0.50	pF	1,2,7,9
Input/output capacitance ZQ pin	CZQ	Min	0.00	pF	1,2
		Max	3.50	pF	1,2

(T_{OPER}; VDDQ = 1.14-1.3V; VDD2 = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

NOTE 1. This parameter applies to die device only (does not include package capacitance).
NOTE 2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
NOTE 3. Absolute value of CCK - CCK#.
NOTE 4. CI applies to CS#, CKE, CA0-CA9.
NOTE 5. CDI = CI - 0.5 * (CCK + CCK#)
NOTE 6. DM loading matches DQ and DQS.
NOTE 7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
NOTE 8. Absolute value of CDQS and CDQS#.
NOTE 9. CDIO = CIO - 0.5 * (CDQS + CDQS#) in byte-lane.

10. IDD Specification Parameters and Test Conditions

10.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: VIN VIL(DC) MAX
HIGH: VIN VIH(DC) MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See Table 44 and Table 45.

Table 44 — Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)
Cycle	N		N+1		N+2		N+3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1. CS# must always be driven HIGH.
NOTE 2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
NOTE 3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

Table 45 — Definition of Switching for IDD4R

Clock	CKE	CS#	Clock Cycle Number	Command	CA0 - CA2	CA3-CA9	ALL DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N+2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N+2	Read_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N+3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+3	NOP	HLH	LHLHLHL	L

NOTE 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

Table 46 — Definition of Switching for IDD4W

Clock	CKE	CS#	Clock Cycle Number	Command	CA0 - CA2	CA3-CA9	ALL DQ
Rising	HIGH	LOW	N	Write_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N+2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N+2	Write_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N+3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+3	NOP	HLH	LHLHLHL	L

NOTE 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2. Data masking (DM) must always be driven LOW.
NOTE 3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

10.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

Table 47 — LPDDR2 IDD Specification Parameters and Operating Conditions (2Gb 2stack)

Parameter / Condition	Symbol		Power Supply	400 MHz	533MHz	Units	Notes
				X32	X32		
Operating one bank active-precharge current (SDRAM):	$IDD0_1$		VDD1	20	20	mA	3
$t_{CK} = t_{CK(avg)min}$; $t_{RC} = t_{RCmin}$;	$IDD0_2$		VDD2	70	70	mA	3
CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_{IN}$		VDDQ	0.1	0.1	mA	3,4
Idle power-down standby current:	$IDD2P_1$	85℃	VDD1	0.8	0.8	mA	3
$t_{CK} = t_{CK(avg)min}$;		105℃		1.0	1.0		
CKE is LOW;	$IDD2P_2$	85℃	VDD2	2	2	mA	3
CS# is HIGH;		105℃		2.4	2.4		
All banks/RBs idle;	$IDD2P_{IN}$	85℃	VDDQ	0.1	0.1	mA	3,4
CA bus inputs are SWITCHING; Data bus inputs are STABLE		105℃		0.1	0.1		
Idle power-down standby current with clock stop:	$IDD2PS_1$	85℃	VDD1	0.8	0.8	mA	3
CK =LOW, CK# =HIGH;		105℃		1.0	1.0		
CKE is LOW;	$IDD2PS_2$	85℃	VDD2	2	2	mA	3
CS# is HIGH;		105℃		2.4	2.4		
All banks/RBs idle;	$IDD2PS_{IN}$	85℃	VDDQ	0.1	0.1	mA	3,4
CA bus inputs are SWITCHING; Data bus inputs are STABLE		105℃		0.1	0.1		
Idle non power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH; CS# is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$		VDD1	2	2	mA	3
	$IDD2N_2$		VDD2	26	30	mA	3
	$IDD2N_{IN}$		VDDQ	0.1	0.1	mA	3,4
Idle non power-down standby current with clock stop: CK =LOW, CK# =HIGH; CKE is HIGH; CS# is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2NS_1$		VDD1	2	2	mA	3
	$IDD2NS_2$		VDD2	14	16	mA	3
	$IDD2NS_{IN}$		VDDQ	0.1	0.1	mA	3,4
Active power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is LOW; CS# is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	85℃	VDD1	4	4	mA	3
		105℃		6	6		
	$IDD3P_2$	85℃	VDD2	8	8	mA	3
		105℃		10	10		
	$IDD3P_{IN}$	85℃	VDDQ	0.1	0.1	mA	3,4
		105℃		0.1	0.1		
Active power-down standby current with clock stop: CK=LOW, CK#=HIGH;	$IDD3PS_1$	85℃	VDD1	4	4	mA	3
		105℃		6	6		
	$IDD3PS_2$	85℃	VDD2	6	6	mA	3
		105℃		10	10		
CKE is LOW; CS# is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_{IN}$	85℃	VDDQ	0.1	0.1	mA	3,4
		105℃		0.1	0.1		

Parameter / Condition	Symbol	Power Supply	400MHz	533MHz	Units	Notes
			X32	X32		
Active non power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH; CS# is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	4	4	mA	3
	$IDD3N_2$	VDD2	32	32	mA	3
	$IDD3N_{IN}$	VDDQ	0.1	0.1	mA	3,4
Active non power-down standby current with clock stop: CK=LOW, CK#=HIGH; CKE is HIGH; CS# is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3NS_1$	VDD1	4	4	mA	3
	$IDD3NS_2$	VDD2	18	22	mA	3
	$IDD3NS_{IN}$	VDDQ	0.1	0.1	mA	3,4
Operating burst read current: $t_{CK} = t_{CK(avg)min}$; CS# is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	VDD1	4	4	mA	3
	$IDD4R_2$	VDD2	230	300	mA	3
Operating burst write current: $t_{CK} = t_{CK(avg)min}$; CS# is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	4	4	mA	3
	$IDD4W_2$	VDD2	230	300	mA	3
	$IDD4W_{IN}$	VDDQ	15	15	mA	3,4
All Bank Refresh Burst current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5_1$	VDD1	60	60	mA	3
	$IDD5_2$	VDD2	200	200	mA	3
	$IDD5_{IN}$	VDDQ	0.1	0.1	mA	3,4
All Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5AB_1$	VDD1	4	4	mA	3
	$IDD5AB_2$	VDD2	32	36	mA	3
	$IDD5AB_{IN}$	VDDQ	0.1	0.1	mA	3,4
Per Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI/8}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5PB_1$	VDD1	4	4	mA	1,3
	$IDD5PB_2$	VDD2	36	36	mA	1,3
	$IDD5PB_{IN}$	VDDQ	0.1	0.1	mA	1,3,4
Self refresh current (Standard Temperature Range): CK=LOW, CK#=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	$IDD6_1$	VDD1	1.2	1.2	mA	2,3,8,9,10
	$IDD6_2$	VDD2	5	5	mA	2,3,8,9,10
	$IDD6_{IN}$	VDDQ	0.1	0.1	mA	2,3,4,8,9,10

Parameter / Condition	Symbol		Power Supply	533 MHz X32	400 MHz X32	Units	Notes
Deep Power-Down current: CK=LOW, CK#=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	85℃	VDD1	40	40	uA	3,11, 12
	$IDD8_2$	85℃	VDD2	200	200	uA	3,11, 12
	$IDD8_{IN}$	85℃	VDDQ	200	200	uA	3,4, 11,12

NOTE 1. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities
NOTE 2. This is the general definition that applies to full array Self Refresh. Refer to Table 48 for details of Partial Array Self Refresh IDD6 specification.
NOTE 3. IDD values published are the maximum of the distribution of the arithmetic mean.
NOTE 4. Measured currents is VDDQ.
NOTE 5. To calculate total current consumption, the currents of all active operations must be considered.
NOTE 6. Guaranteed by design with output load of 5pF and RON = 40Ohm.
NOTE 7. IDD current specifications are tested after the device is properly initialized.
NOTE 8. In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.
NOTE 9. 1x Self-Refresh Rate is the rate at which the LPDDR2-S4 device is refreshed internally during Self-Refresh before going into the Extended Temperature range.
NOTE 10. IDD6 85℃ is guaranteed.
NOTE 11. IDD8 85℃ is guaranteed.
NOTE 12. DPD (Deep Power Down) is an optional feature, and it will be enabled upon request.
Please contact JSC for more information

Table 48 — IDD6 Partial Array Self-Refresh Current

Parameter		Symbol	Power Supply	LPDDR2		Unit
				85℃	105℃	
IDD6 Partial Array Self Refresh Current (max)	Full Array	$IDD6_1$	VDD1	1.2	8.4	mA
		$IDD6_2$	VDD2	5	17.6	
		$IDD6_{IN}$	VDDQ	0.1	0.1	
	1/2 Array	$IDD6_1$	VDD1	1	8	mA
		$IDD6_2$	VDD2	4	11.6	
		$IDD6_{IN}$	VDDQ	0.1	0.1	
	1/4 Array	$IDD6_1$	VDD1	0.9	7.2	mA
		$IDD6_2$	VDD2	3.4	8	
		$IDD6_{IN}$	VDDQ	0.1	0.1	
	1/8 Array	$IDD6_1$	VDD1	0.84	6.8	mA
		$IDD6_2$	VDD2	3	7.2	
		$IDD6_{IN}$	VDDQ	0.1	0.1	

NOTE 1. IDD6 105℃ is the maximum.
NOTE 2. IDD6 85℃ is guaranteed.
NOTE 3. PASR (Partial Array Self Refresh) function will be supported upon request. Please contact JSC for more information.

11. Electrical Characteristics and AC Timing

11.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

11.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left\{ \sum_{j=1}^{N} tCKj \right\} / N$$
$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

11.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
tCK(abs) is not subject to production test.

11.1.3 12.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses

$$tCH(avg) = \left\{ \sum_{j=1}^{N} tCHj \right\} / (N \times tCK(avg))$$
$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left\{ \sum_{j=1}^{N} tCLj \right\} / (N \times tCK(avg))$$
$$where \qquad N = 200$$

11.1.4 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act is the actual clock jitter for a given system.
tJIT(per),allowed is the specified allowed clock period jitter.
tJIT(per) is not subject to production test.

11.1.5 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCKi +1 - tCKi}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

11.1.6 6 Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act is the actual clock jitter over n cycles for a given system.
tERR(nper),allowed is the specified allowed clock period jitter over n cycles.
tERR(nper) is not subject to production test.

$$tERR(nper) = \left\{ \sum_{j=1}^{i+n-1} tCKj \right\} - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper),min = (1 + 0.68LN(n)) \times tJIT(per),min$$

tERR(nper),max can be calculated by the formula shown below:

$$tERR(nper),max = (1 + 0.68LN(n)) \times tJIT(per),max$$

Using these equations, **t**ERR(nper) tables can be generated for each **t**JIT(per),act value.

11.1.7 Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty),min = MIN((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) \times tCK(avg)$$

$$tJIT(duty),max = MAX((tCH(abs),max - tCH(avg),max),(tCL(abs),max - tCL(avg),max)) \times tCK(avg)$$

11.1.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 49 — Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	t_{CK} (abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	t_{CH} (abs)	tCH(avg),min + tJIT(duty),min/ tCK(avg),min	t_{CK} (avg)
Absolute Clock LOW Pulse Width	t_{CL} (abs)	tCL(avg),min + tJIT(duty),min/ tCK(avg),min	t_{CK} (avg)

NOTE 1 tCK(avg),min is expressed is ps for this table.
NOTE 2 tJIT(duty),min is a negative value.

11.2 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 52 and how to determine cycle time de-rating and clock cycle de-rating.

11.2.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.
When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

11.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right),0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

11.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).
For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right)\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

11.2.2 Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e., tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.3 12.2.3 Clock jitter effects on Read timing parameters

11.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9\left\{\frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}\right\}$$

For example,
if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max = + 193 ps, then
tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500=0.8628 tCK(avg)

11.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

11.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.
tQSH(abs)min = tCH(abs)min – 0.05
tQSL(abs)min = tCL(abs)min – 0.05
These parameters determine absolute Data-Valid window at the LPDDR2 device pin.
Absolute min data-valid window @ LPDDR2 device pin =
min {(tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax)}

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

11.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

11.2.4 Clock jitter effects on Write timing parameters

11.2.4.1 1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn, DQSn# : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx, DQSx#) crossing to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx, DQSx#) crossing to the subsequent clock signal (CK/CK#) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(\min, derated) = 0.75 - \frac{tJIT(per, act, min) - tJIT(per), allowed, min}{tCK(avg)}$$

$$tDQSS(\min, derated) = 1.25 - \frac{tJIT(per, act, max) - tJIT(per), allowed, max}{tCK(avg)}$$

For example,
if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then
tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = 0.7788 tCK(avg)
and
tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

11.3 Refresh Requirements

Table 50 —Refresh Requirement Parameters

Parameter		Symbol	4Gb (2Gb 2stack)	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85℃		t_{REFW}	32	ms
Refresh Window 85℃≤ Tcase ≤ 105℃		t_{REFW}	8	ms
Required number of REFRESH commands (min)		R	8,192	
average time between REFRESH commands (for reference only) Tcase ≤ 85℃	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	us

11.4 AC Timings

Table 51 — AC Timing Table[*6]

Parameter	Symbol	min/ max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
Max. Frequency[*4]		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	t_{CK}(avg)	min		1.875	2.15	2.5	3	3.75	5	6	ns
		max		100							
Average high pulse width	t_{CH}(avg)	min		0.45							t_{CK}(avg)
		max		0.55							
Average low pulse width	t_{CL}(avg)	min		0.45							
		max		0.55							
Absolute Clock Period	t_{CK}(abs)	min		t_{CK}(avg),min -/+ t_{JIT}(per),min							ps
Absolute clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	min		0.43							t_{CK}(avg)
		max		0.57							
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	min		0.43							
		max		0.57							
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	min		-90	-95	-100	-110	-120	-140	-150	ps
		max		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed Jitter)	t_{JIT}(cc), allowed	max		180	190	200	220	240	280	300	ps
Duty cycle Jitter (with allowed Jitter)	t_{JIT}(duty), allowed	min		min((t_{CH}(abs),min-t_{CH}(avg),min), (t_{CL}(abs),min-t_{CL}(avg),min)) X t_{CK}(avg)							ps
		max		max((t_{CH}(abs),max-t_{CH}(avg),max), (t_{CL}(abs),max-t_{CL}(avg),max)) X t_{CK}(avg)							ps
Cumulative errors across 2cycles	t_{ERR}(2per), allowed	min		-132	-140	-147	-162	-177	-206	-221	ps
		max		132	140	147	162	177	206	221	
Cumulative errors across 3cycles	t_{ERR}(3per), allowed	min		-157	-166	-175	-192	-210	-245	-262	ps
		max		157	166	175	192	210	245	262	
Cumulative errors across 4cycles	t_{ERR}(4per), allowed	min		-175	-185	-194	-214	-233	-272	-291	ps
		max		175	185	194	214	233	272	291	
Cumulative errors across 5cycles	t_{ERR}(5per), allowed	min		-188	-199	-209	-230	-251	-293	-314	ps
		max		188	199	209	230	251	293	314	
Cumulative errors across 6cycles	t_{ERR}(6per), allowed	min		-200	-211	-222	-244	-266	-311	-333	ps
		max		200	211	222	244	266	311	333	
Cumulative errors across 7cycles	t_{ERR}(7per), allowed	min		-209	-221	-232	-256	-279	-325	-348	ps
		max		209	221	232	256	279	325	348	
Cumulative errors across 8cycles	t_{ERR}(8per), allowed	min		-217	-229	-241	-266	-290	-338	-362	ps
		max		217	229	241	266	290	338	362	
Cumulative errors across 9cycles	t_{ERR}(9per), allowed	min		-224	-237	-249	-274	-299	-349	-374	ps
		max		224	237	249	274	299	349	374	
Cumulative errors across 10cycles	t_{ERR}(10per), allowed	min		-231	-244	-257	-282	-308	-359	-385	ps
		max		231	244	257	282	308	359	385	
Cumulative errors across 11cycles	t_{ERR}(11per), allowed	min		-237	-250	-263	-289	-316	-368	-395	ps
		max		237	250	263	289	316	368	395	
Cumulative errors across 12cycles	t_{ERR}(12per), allowed	min		-242	-256	-269	-296	-323	-377	-403	ps
		max		242	256	269	296	323	377	403	
Cumulative errors across n= 13, 14, … 49, 50cycles	t_{ERR}(nper), allowed	min		tERR(nper),allowed,min = (1+0.68ln(n)) X tJIT(per),allowed,min							ps
		max		tERR(nper),allowed,max = (1+0.68ln(n)) X tJIT(per),allowed,max							

Parameter	Symbol	min/max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
ZQ Calibration Parameters											
Initialization Calibration Time	t_{ZQINIT}	min		1							us
Long Calibration Time	t_{ZQCL}	min	6	360							ns
Short Calibration Time	t_{ZQCS}	min	6	90							
Calibration Reset Time	$t_{ZQRESET}$	min	3	50							
Read Parameters*11,*12											
DQS output access time from CK /CK#	t_{DQSCK}	min		2500							ps
		max		5500							
DQSCK Delta Short*15	$t_{DQSCKDS}$	max		330	380	450	540	670	900	1080	
DQSCK Delta Medium*16	$t_{DQSCKDM}$	max		680	780	900	1050	1350	1800	1900	
DQSCK Delta Long*17	$t_{DQSCKDL}$	max		920	1050	1200	1400	1800	2400	-	
DQS - DQ skew	t_{DQSQ}	max		200	220	240	280	340	400	500	
Data hold skew factor	t_{QHS}	max		230	260	280	340	400	480	600	
DQS Output High pulse width	t_{QSH}	min		tCH(abs)-0.05							t_{CK}(avg)
DQS Output Low pulse width	t_{QSL}	min		tCL(abs)-0.05							
Data Half period	t_{QHP}	min		$min(t_{QSH}, t_{QSL})$							
DQ/DQS output hold time from DQS	t_{QH}	min		t_{QHP}-t_{QHS}							ps
Read preamble*13	t_{RPRE}	min		0.9							t_{CK}(avg)
Read postamble*14	t_{RPST}	min		$t_{CL(abs)}$-0.05							
DQS low-Z from clock	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)}$-300							ps
DQ low-Z from clock	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)}$-(1.4 X $t_{QHS(MAX)}$)							
DQS high-Z from clock	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)}$-100							
DQ high-Z from clock	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)}$+(1.4 X $t_{DQSQ(MAX)}$)							

Parameter	Symbol	min/max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
Write Parameters[*11]											
DQ and DM input hold time (V_{REF} based)	t_{DH}	min		210	235	270	350	430	480	600	ps
DQ and DM input setup time (V_{REF} based)	t_{DS}	min		210	235	270	350	430	480	600	
DQ and DM input pulse width	t_{DIPW}	min		0.35							tCK(avg)
Write command to first DQS latching transition	t_{DQSS}	min		0.75							tCK(avg)
		max		1.25							
DQS input high-level width	t_{DQSH}	min		0.4							tCK(avg)
DQS input low-level width	t_{DQSL}	min		0.4							tCK(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2							tCK(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2							tCK(avg)
Write postamble	t_{WPST}	min		0.4							tCK(avg)
Write preamble	t_{WPRE}	min		0.35							tCK(avg)

Parameter	Symbol	min/max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
CKE Input parameters											
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3							tCK(avg)
CKE input setup time	t_{ISCKE} [*2]	min		0.25							tCK(avg)
CKE input hold time	t_{IHCKE} [*3]	min		0.25							tCK(avg)
Command Address Input Parameters [*1]											
Address and control input setup time (Vref based)	t_{IS} [*1]	min		220	250	290	370	460	600	740	ps
Address and control input hold time (Vref based)	t_{IH} [*1]	min		220	250	290	370	460	600	740	ps
Address and control input pulse width	t_{IPW}	min	0.40								tCK(avg)
Boot Parameters (10MHz - 55MHz) [*5 *7 *8]											
Clock Cycle Time	t_{CKb}	max	-	100							ns
		min		18							ns
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5							ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5							ps
Address & Control Input Setup Time	t_{ISb}	min	-	1150							ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150							ps
DQS Output Data Access Time from CK_t/CK_c	t_{DQSCKb}	min	-	2							ns
		max		10.0							
Data Strobe Edge to Ouput Data Edge	t_{DQSQb}	max	-	1.2							ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2							ns
Mode Register Parameters											
MODE REGISTER Write command period	t_{MRW}	min	5	5							tCK(avg)
Mode Register Read command period	t_{MRR}	min	2	2							tCK(avg)

Parameter	Symbol	min/max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
LPDDR2 SDRAM Core Parameters [*9]											
Read Latency	RL	min	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	min	1	4	4	3	2	2	1	1	tCK(avg)
ACTIVE to ACTIVE command period	t_{RC}	min		t_{RAS}+t_{RPab} (with all-bank Precharge) t_{RAS} +t_{RPpb} (with per-bank Precharge)							ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15							ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab} +10							ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5							ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2							tCK(avg)
LPDDR2-S2 CAS to CAS delay	t_{CCD}	min	1	1							tCK(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5							ns
RAS to CAS Delay	t_{RCD}	Fast	3	15							ns
		Typ	3	18							ns
		Slow	3	24							ns
Row Precharge Time (single bank)	t_{RPpb}	Fast	3	15							ns
		Typ	3	18							ns
		Slow	3	24							ns
Row Precharge Time (all banks)	t_{RPab} 4-bank	Fast	3	15							ns
		Typ	3	18							ns
		Slow	3	24							ns
Row Precharge Time (all banks)	t_{RPab} 8-bank	Fast	3	18							ns
		Typ	3	21							ns
		Slow	3	27							ns
Row Active Time	t_{RAS}	min	3	42							ns
		max	-	70							us
Write Recovery Time	t_{WR}	min	3	15							ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5					10		ns
Active bank A to Active bank B	t_{RRD}	min	2	10							ns
Four Bank Activate Window[*18]	t_{FAW}	min	8	50						60	ns
Minimum Deep Power Down Time	t_{DPD}	min		500							us

Parameter	Symbol	min/max	min t_{CK}	LPDDR2							Unit
				1066	933	800	667	533	400	333	
LPDDR2 Temperature De-Rating											
tDQSCK De-Rating	t_{DQSCK} (Derated)	max		5620	6000						ps
Core Timings Temperature De-Rating for SDRAM	t_{RCD} (Derated)	min		t_{RCD} + 1.875							ns
	t_{RC} (Derated)	min		t_{RC} + 1.875							ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875							ns
	t_{RP} (Derated)	min		t_{RP} + 1.875							ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875							ns

NOTE 1. Input set-up/hold time for signal(CA0 ~ 9, CS#)
NOTE 2. CKE input setup time is measured from CKE reaching high/low voltage level to CK/CK# crossing.
NOTE 3. CKE input hold time is measured from CK/CK# crossing to CKE reaching high/low voltage level .
NOTE 4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
NOTE 5. To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table 51 . Boot parameter symbols have the letter b appended, e.g., tCK during boot is tCKb.
NOTE 6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
NOTE 7. The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in 3.3.
NOTE 8. The output skew parameters are measured with Ron default settings into the reference load.
NOTE 9. The min tCK column applies only when tCK is greater than 6ns for LPDDR2. In this case, both min tCK values and analog timings (ns) shall be satisfied.
NOTE 10. All AC timings assume an input slew rate of 1V/ns.
NOTE 11. Read, Write, and Input Setup and Hold values are referenced to Vref.

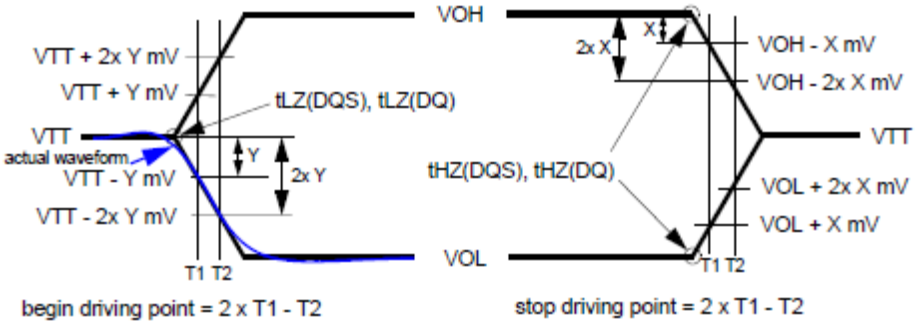


Figure 11.1 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-DQS#.

NOTE 12. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 11.1 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
NOTE 13. Measured from the start driving of DQS - DQS# to the start driving the first rising strobe edge.
NOTE 14. Measured from the start driving the last falling strobe edge to the stop driving DQS - DQS#.
NOTE 15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a Temperature drift in the system is < 10C/s. Values do not include clock jitter.
NOTE 16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
NOTE 17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
NOTE 18. tFAW is only applied in devices with 8 banks.

11.5 CA and CS# Setup, Hold and Derating

For all input signals (CA and CS#) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 52) to the tIS and tIH derating value (see Table 53) respectively. Example: tIS (total setup time) = tIS(base) + tIS. Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value (see Figure Figure 11.2). If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 11.4).
Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value (see Figure 11.3). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 11.5).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 53).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in Table 53, the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization

Table 52 — CA and CS# Setup and Hold Base-Values for 1V/ns

unit [ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tIS(base)	0	30	70	150	240	300	$V_{IH/L(ac)}$ = VREF(dc) +/- 220mV
tIH(base)	90	120	160	240	330	390	$V_{IH/L(ac)}$ = VREF(dc) +/- 130mV

unit [ps]	LPDDR2				reference
	400	333	266	200	
tIS(base)	300	440	600	850	$V_{IH/L(ac)}$ = VREF(dc) +/- 300mV
tIH(base)	400	540	700	950	$V_{IH/L(ac)}$ = VREF(dc) +/- 200mV

NOTE 1 ac/dc referenced for 1V/ns CA and CS# slew rate and 2V/ns differential CK-CK# slew rate.

Table 53 — Derating values LPDDR2 tIS/tIH - ac/dc based AC220

△tIS △IH derating in [ps] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS# Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 54 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-

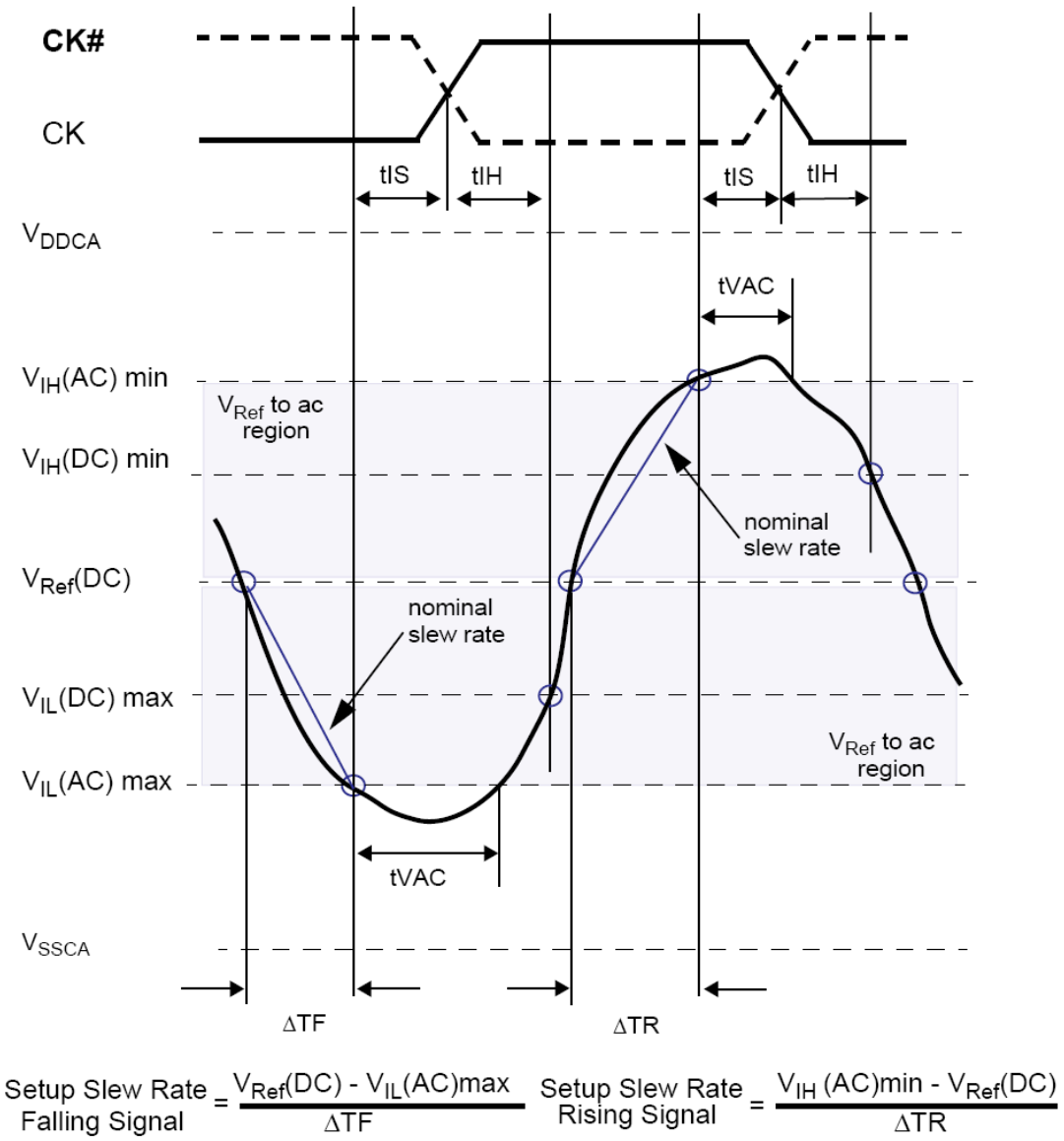


Figure 11.2 — Illustration of nominal slew rate and tVAC for setup time tIS for CA and CS# with respect to clock.

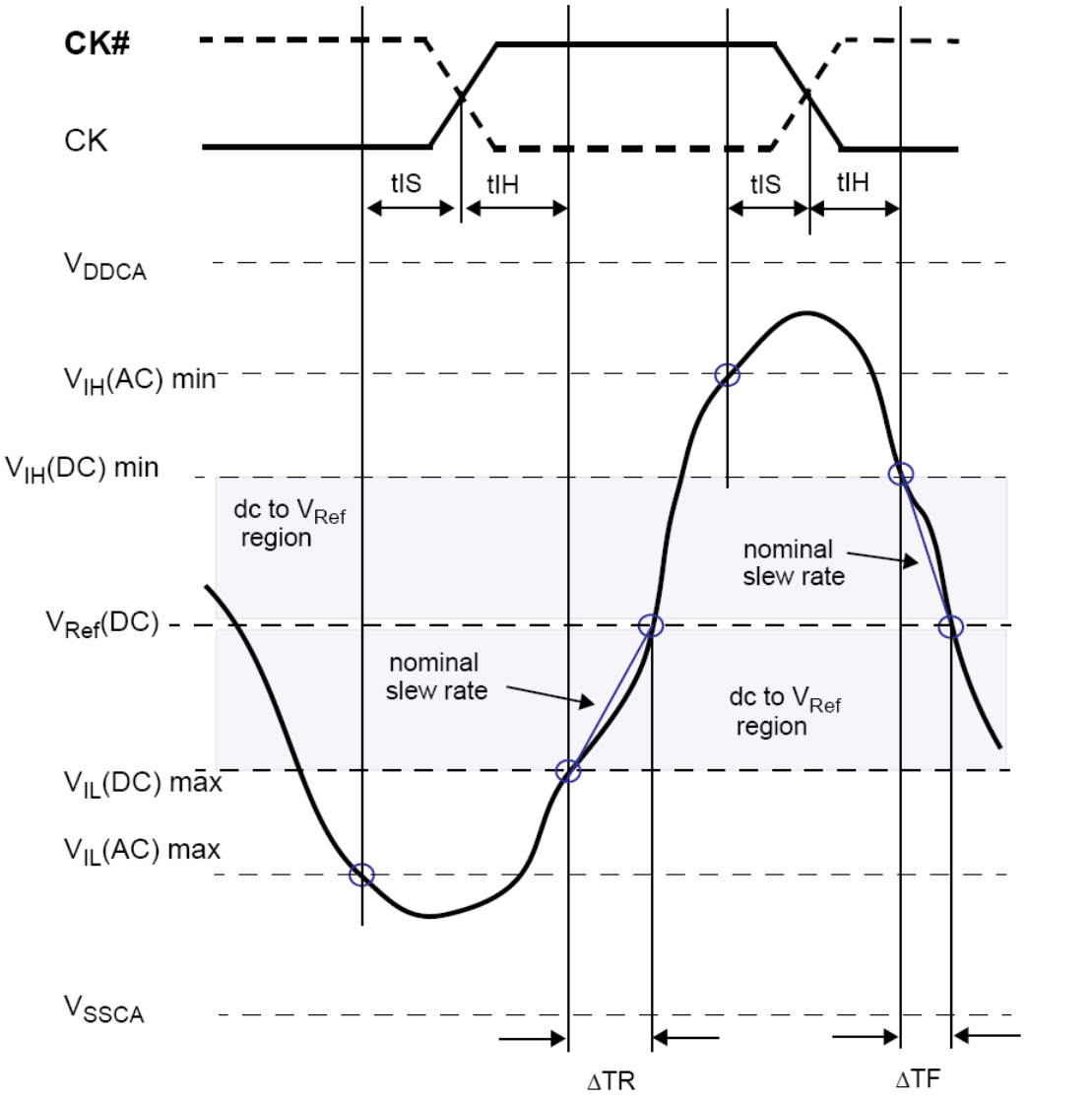


Figure 11.3 — Illustration of nominal slew rate for hold time tIH for CA and CS# with respect to clock

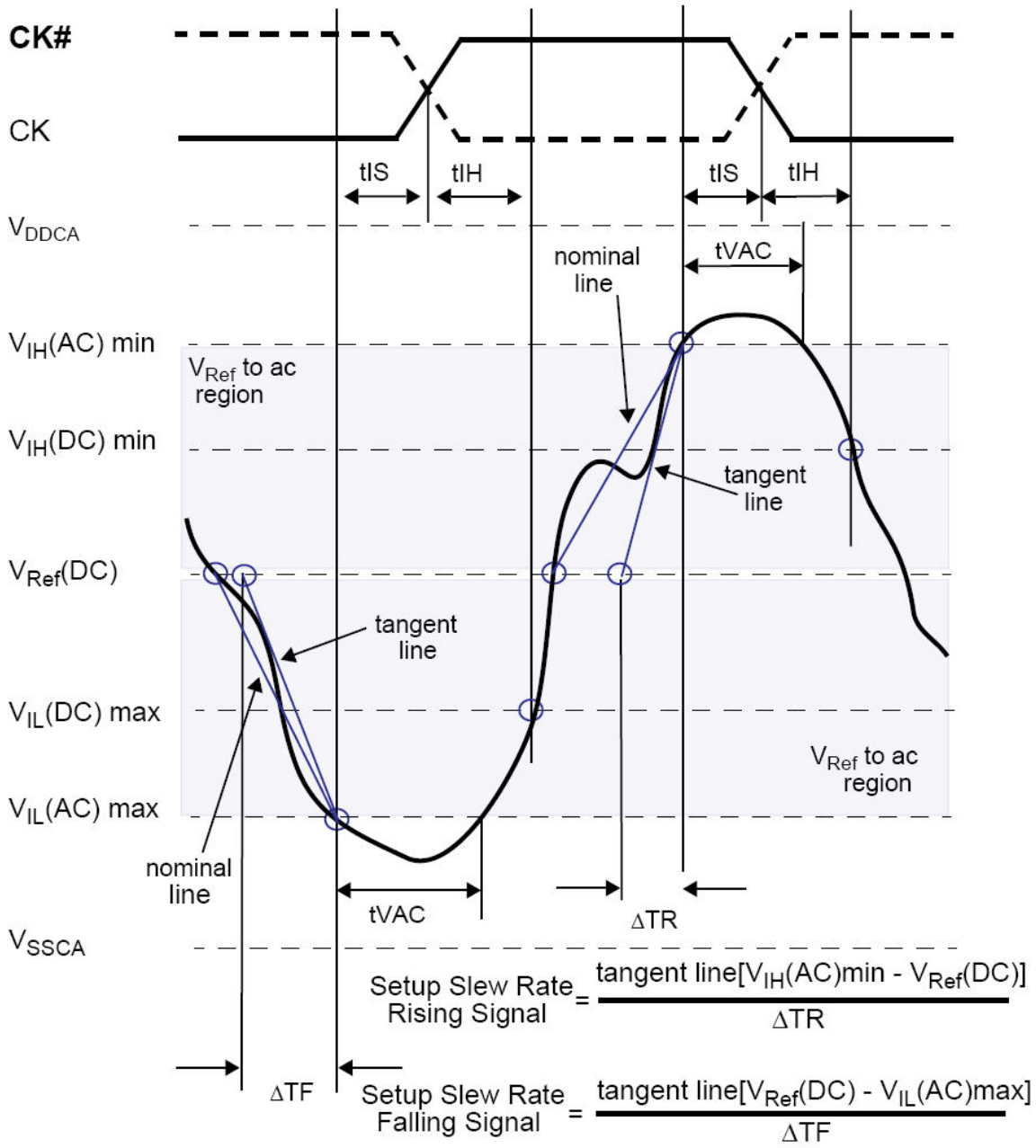
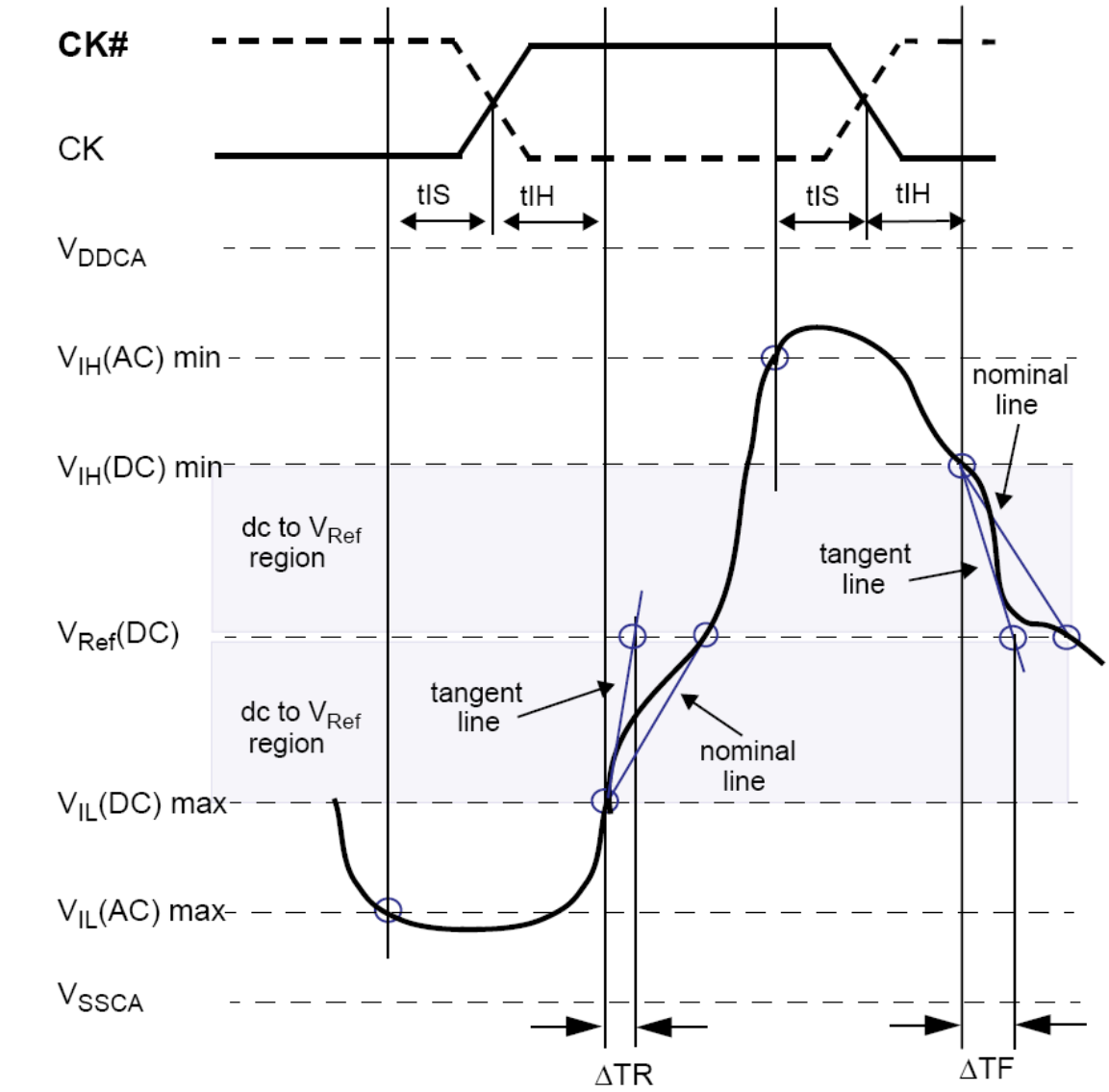


Figure 11.4 — Illustration of tangent line for setup time tIS for CA and CS# with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)\text{max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)\text{min} - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 11.5 — Illustration of tangent line for for hold time tIH for CA and CS# with respect to clock

11.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 55) to the tDS and tDH (see Table 56) derating value respectively. Example: tDS (total setup time) = tDS(base) + tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max(see Figure 11.6). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 11.8).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see Figure 11.7). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 11.9).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 57).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 55 — Data Setup and Hold Base-Values

unit [ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tDS(base)	-10	15	50	130	210	230	$V_{IH/L(ac)}$ = VREF(dc) +/- 220mV
tDH(base)	80	105	140	220	300	320	$V_{IH/L(ac)}$ = VREF(dc) +/- 130mV

unit [ps]	LPDDR2				reference
	400	333	266	200	
tDS(base)	180	300	450	700	$V_{IH/L(ac)}$ = VREF(dc) +/- 300mV
tDH(base)	280	400	550	800	$V_{IH/L(ac)}$ = VREF(dc) +/- 200mV

NOTE 1 ac/dc referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS-DQS# slew rate.

Table 56 — Derating values LPDDR2 tDS/tDH - ac/dc based AC220

△tDS, △DH derating in [ps] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 57 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-

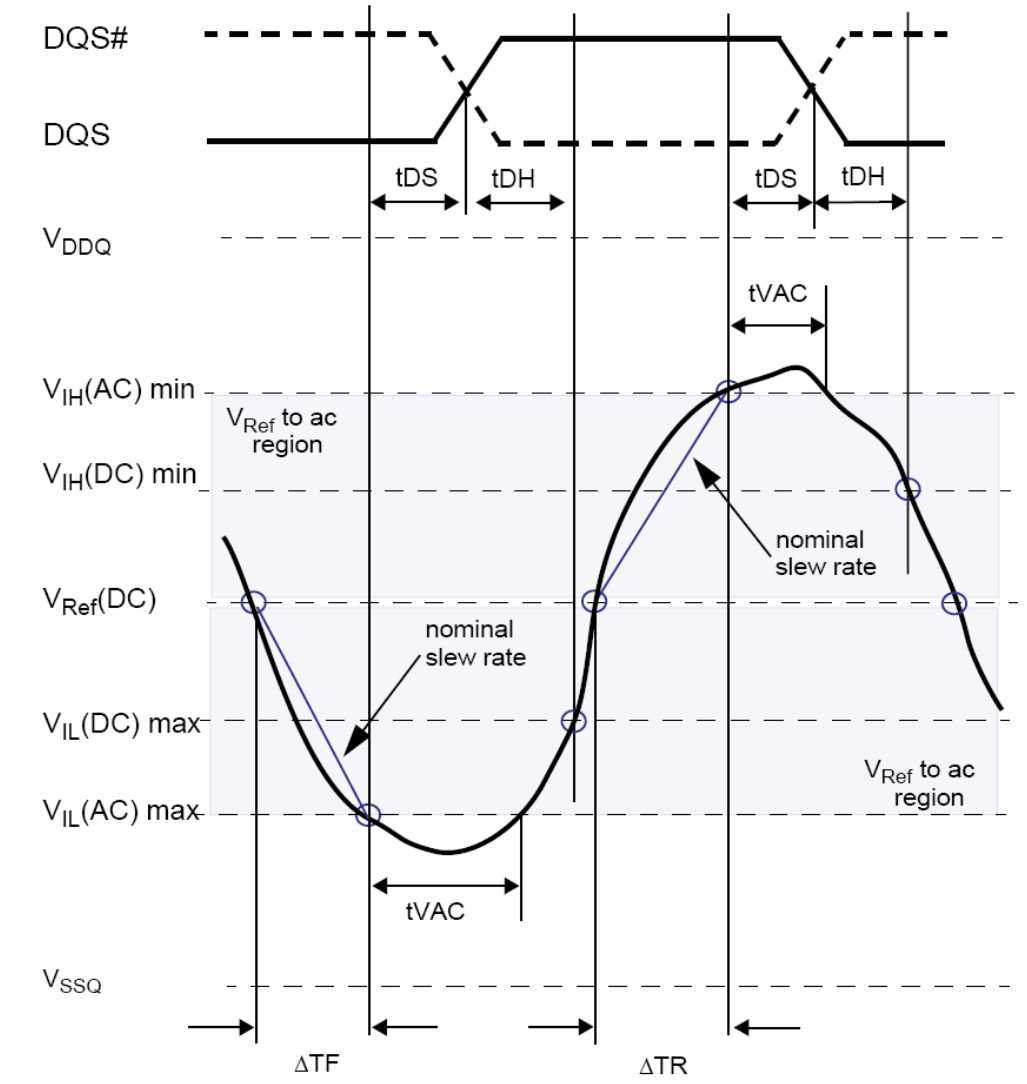
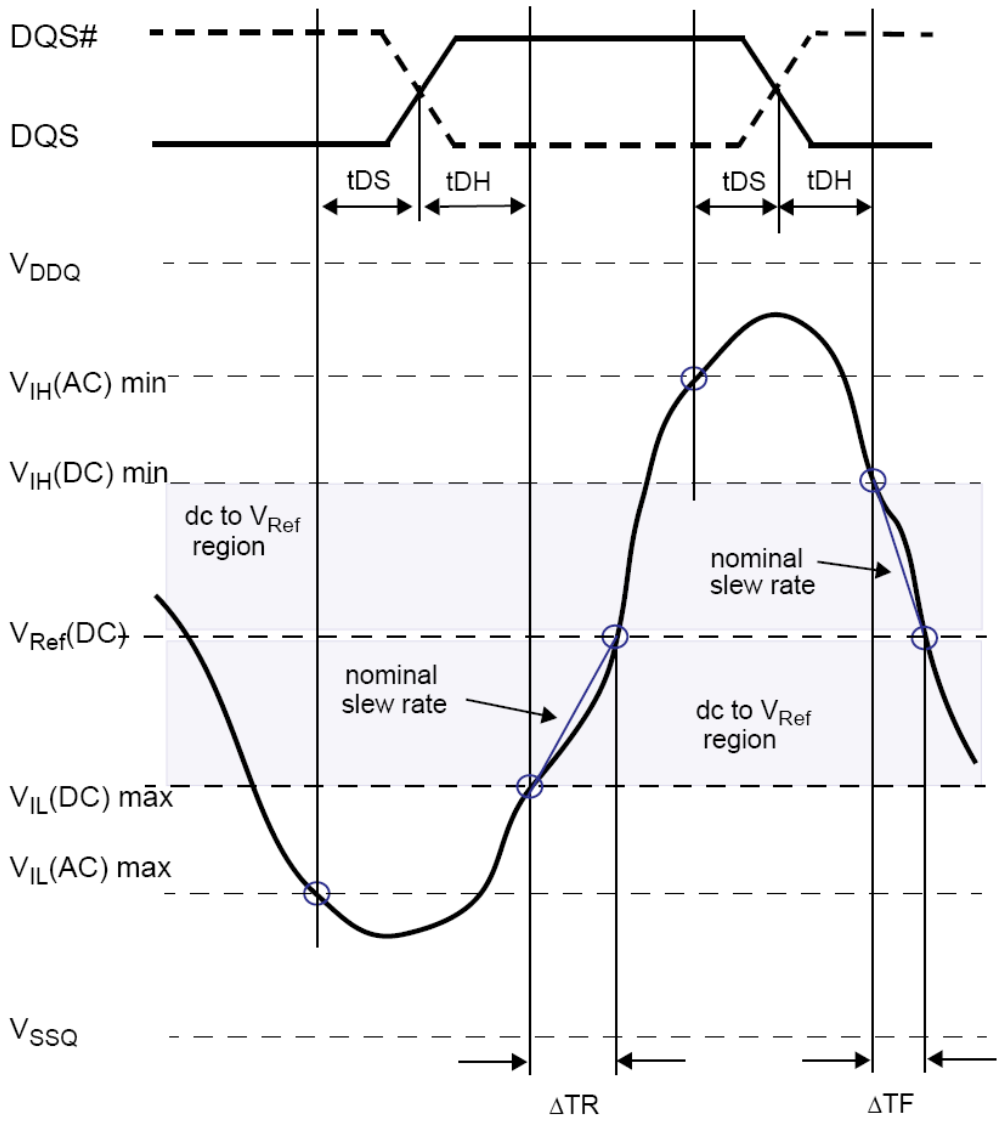


Figure 11.6 — Illustration of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref}(DC) - V_{IL}(DC)max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{Ref}(DC)}{\Delta TF}$$

Figure 11.7 — Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

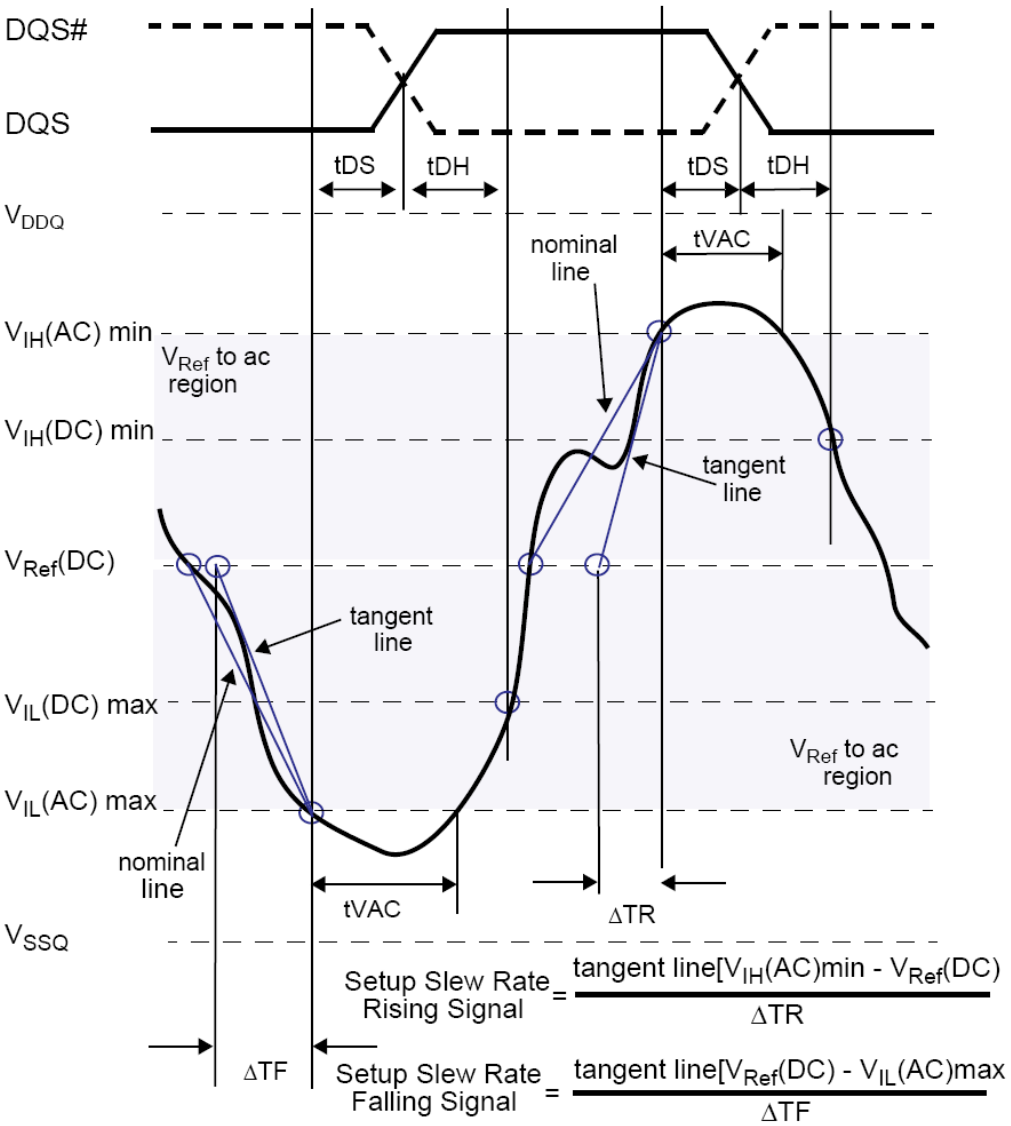
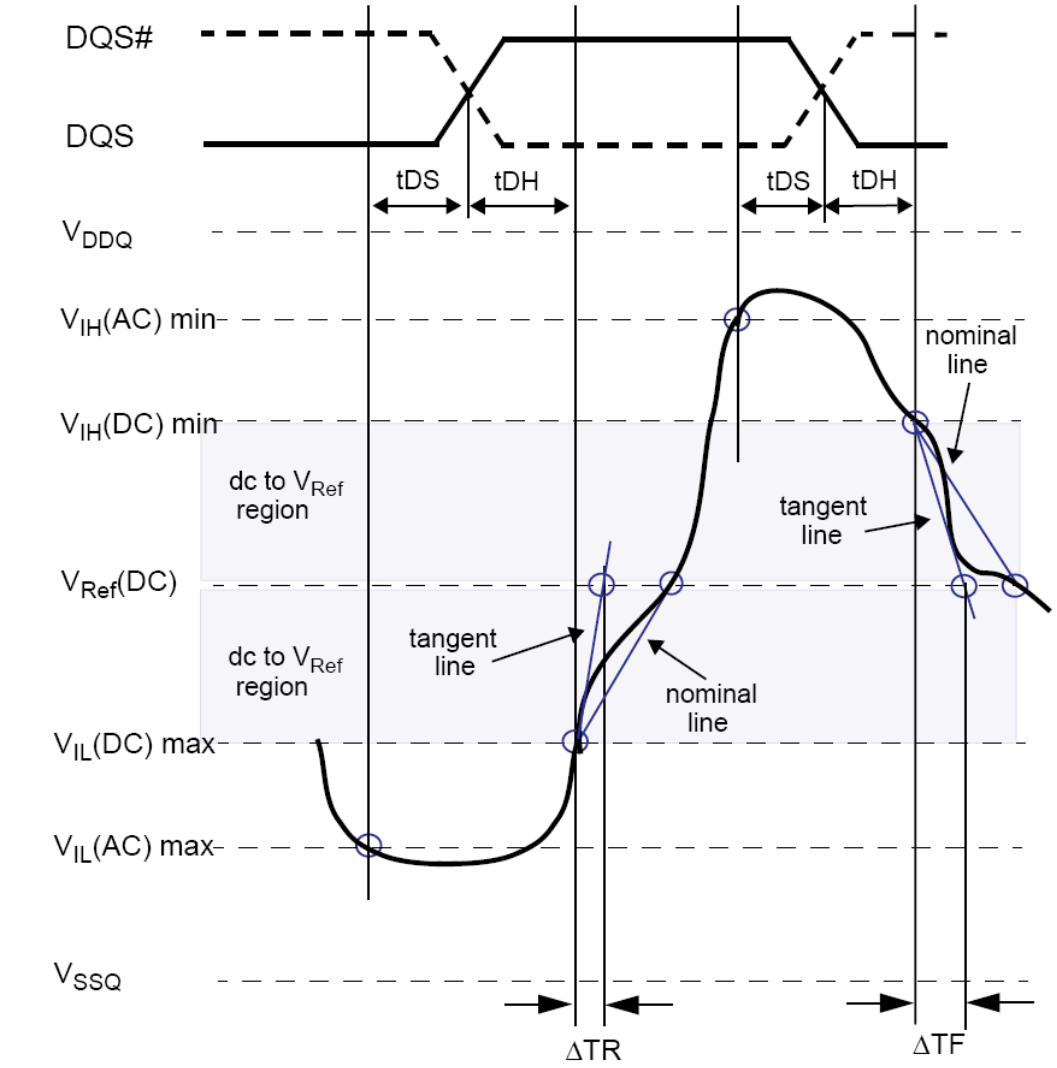


Figure 11.8 — Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

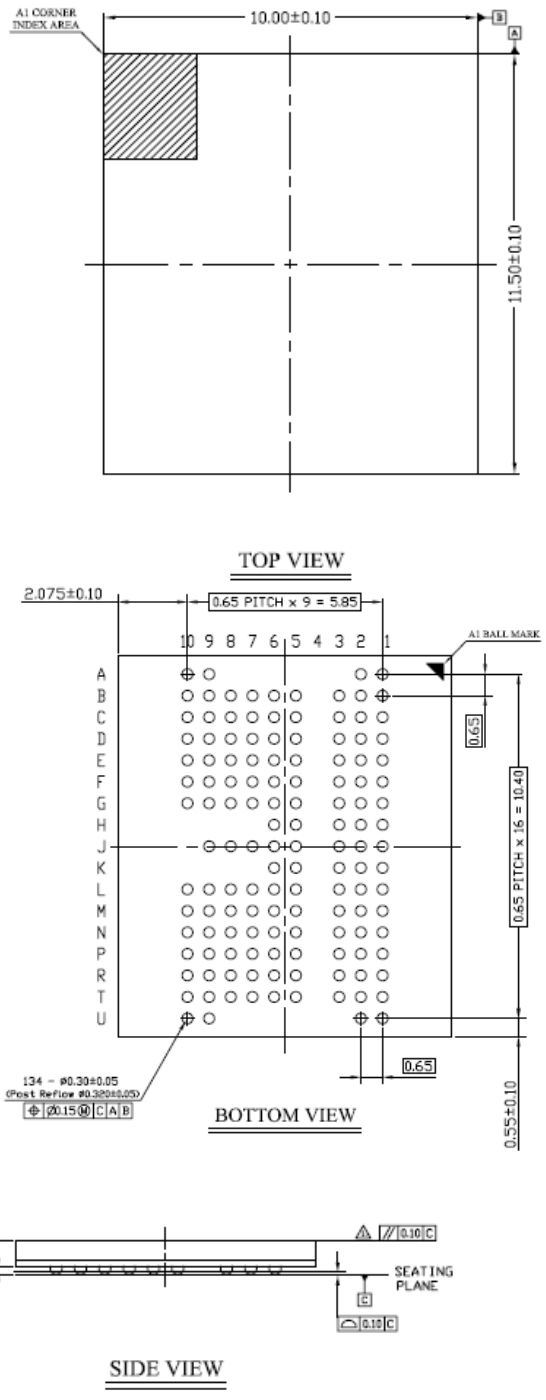


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)max \text{]}}{\Delta TR}$$

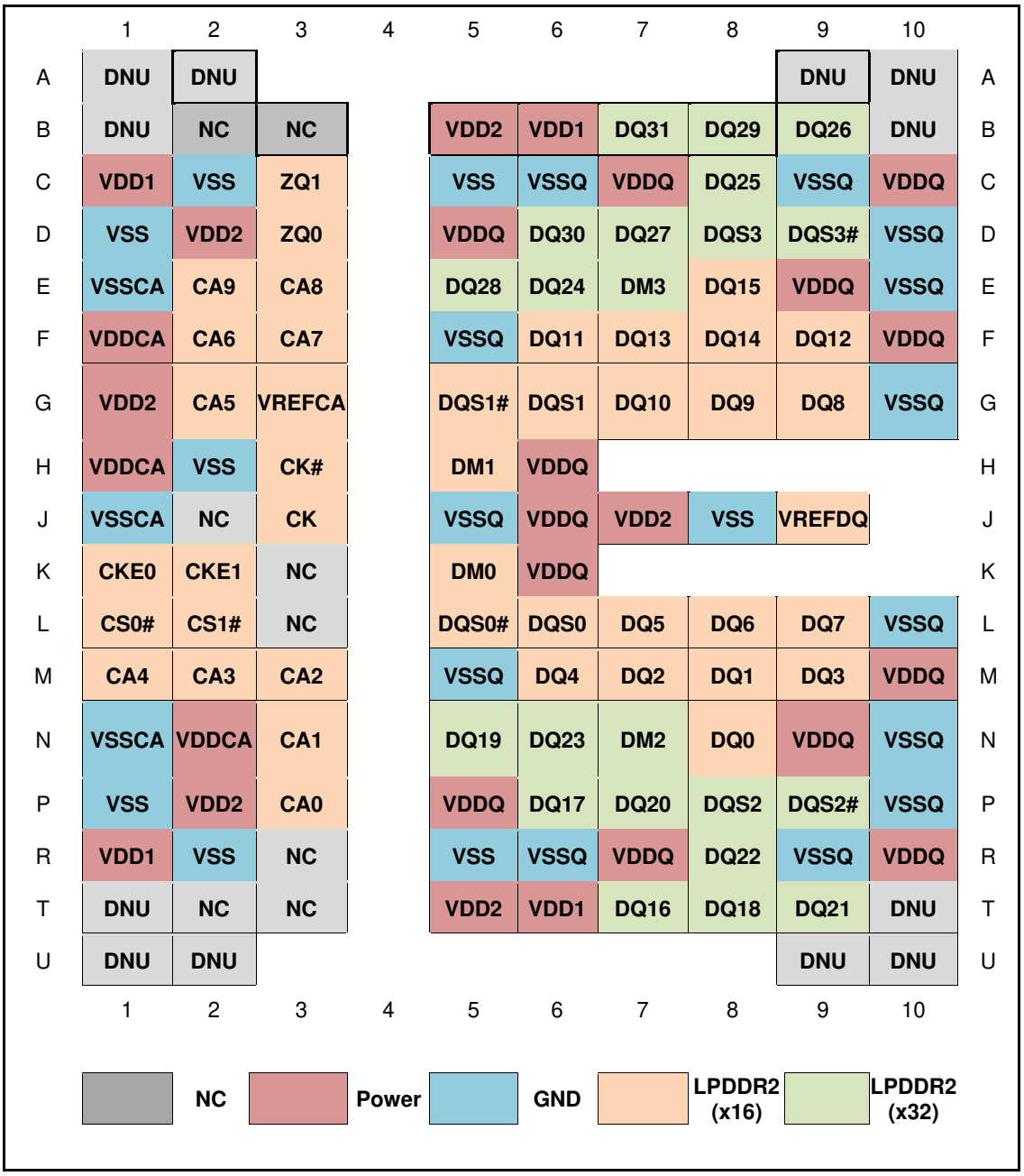
$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)min - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 11.9 — Illustration of tangent line for for hold time t_{DH} for DQ with respect to strobe

PKG Information
[134-Ball FBGA – 10mm x 11.5mm x 1.0mm (max)]



[134-Ball FBGA – Ball Out]



	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU	B
C	VDD1	VSS	ZQ1		VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ	C
D	VSS	VDD2	ZQ0		VDDQ	DQ30	DQ27	DQS3	DQS3#	VSSQ	D
E	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ	E
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	VREFCA		DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ	G
H	VDDCA	VSS	CK#		DM1	VDDQ					H
J	VSSCA	NC	CK		VSSQ	VDDQ	VDD2	VSS	VREFDQ		J
K	CKE0	CKE1	NC		DM0	VDDQ					K
L	CS0#	CS1#	NC		DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ	L
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSSCA	VDDCA	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ	N
P	VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2	DQS2#	VSSQ	P
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ	R
T	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU	T
U	DNU	DNU							DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	

NC Power GND LPDDR2 (x16) LPDDR2 (x32)

*Note : 1. DQ15~32 , DQS2,3,DQS#2,3,DM2,3 are NC for the x16 LPDRAM device.
2. CS1#,ZQ1,CKE1 are only used for 2CS device. In other case is NC
3. VSS pins are shared ground

REVISION HISTORY

VERSION	DATE	DESCRIPTION
0.1	Mar/2018	Initial draft
0.2	Apr/2018	Update DC table.
0.3	Apr/2018	Update table 7
0.4	Dec/2018	Remove no-wrap function Update DC table
0.5	Jan/2019	Update DC table
0.6	Mar/2019	Update DC table for AT
1.0	Aug/2019	Update IDD6 Version update for mass production
1.1	Nov/2019	Update ordering Information Table Update Taqble 50: Add tREFW
1.2	Aug/2020	Correction of typo [Table 31]
1.3	Apr/2022	Update DC table

Important Notice

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