

HEF4060B

14-stage ripple-carry binary counter/divider and oscillator

Rev. 11 — 3 September 2024

Product data sheet

1. General description

The HEF4060B is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered parallel outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (REXT and CEXT) floating. The counter advances on the HIGH-to-LOW transition of RS. A HIGH level on MR clears all counter stages and forces all outputs LOW, independent of the other input conditions. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standard JESD 13-B
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4060BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4060BTT	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

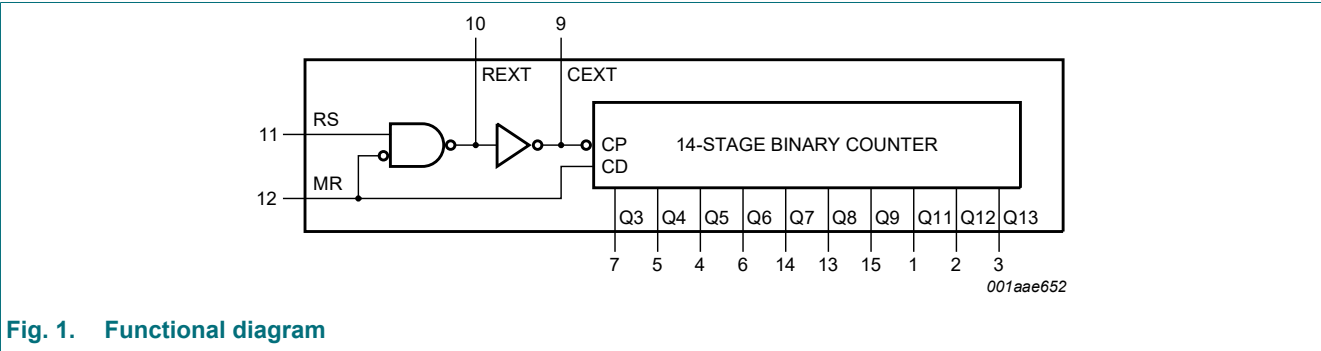


Fig. 1. Functional diagram

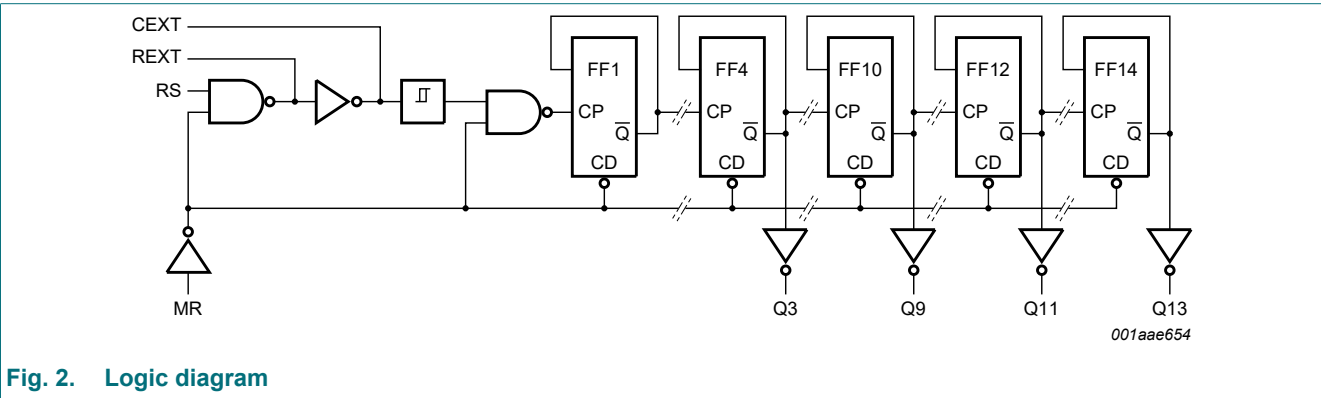


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning

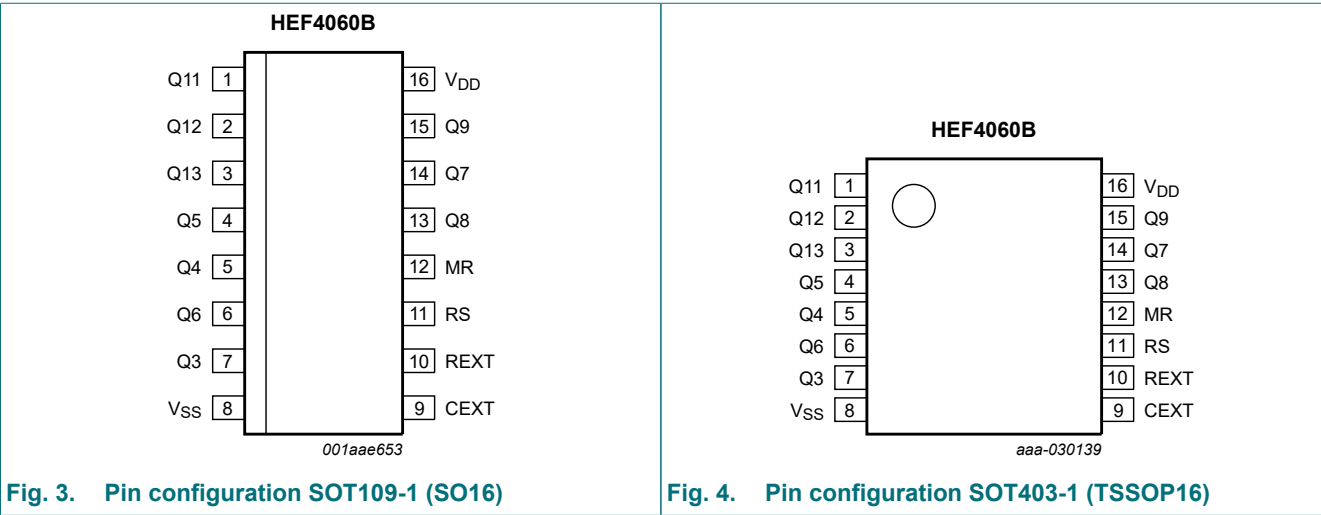


Fig. 3. Pin configuration SOT109-1 (SO16)

Fig. 4. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
V _{SS}	8	ground supply voltage
CEXT	9	external capacitor connection
REXT	10	oscillator pin
RS	11	clock input/oscillator pin
MR	12	master reset
V _{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input		Output
RS	MR	Q3 to Q9 and Q11 to Q13
↑	L	no change
↓	L	count
X	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	input MR				
		V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; $C_L = 50\text{ pF}$; $t_r = t_f \leq 20\text{ ns}$; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t _{pd}	propagation delay	RS → Q3; see Fig. 5	5 V	[2] 183 ns + (0.55 ns/pF) C _L	-	210	420	ns
			10 V	69 ns + (0.23 ns/pF) C _L	-	80	160	ns
			15 V	42 ns + (0.16 ns/pF) C _L	-	50	100	ns
		Qn → Qn + 1; see Fig. 5	5 V	-	-	25	50	ns
			10 V	-	-	10	20	ns
			15 V	-	-	6	12	ns
		MR → Qn; HIGH to LOW see Fig. 5	5 V	73 ns + (0.55 ns/pF) C _L	-	100	200	ns
			10 V	29 ns + (0.23 ns/pF) C _L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF) C _L	-	30	60	ns
t _t	transition time	see Fig. 5	5 V	[3] 10 ns + (1.00 ns/pF) C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C _L	-	20	40	ns
t _w	pulse width	minimum width; RS HIGH; see Fig. 5	5 V		120	60	-	ns
			10 V		50	25	-	ns
			15 V		30	15	-	ns
		minimum width; MR HIGH; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t _{rec}	recovery time	input MR; see Fig. 5	5 V		160	80	-	ns
			10 V		80	40	-	ns
			15 V		60	30	-	ns
f _{max}	maximum frequency	input RS; see Fig. 5	5 V		4	8	-	MHz
			10 V		10	20	-	MHz
			15 V		15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_t is the same as t_{THL} and t_{TLH}.

Table 8. Power dissipation

Dynamic power dissipation P_D and total power dissipation P_{tot} can be calculated from the formulas shown. $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	V_{DD}	Typical formula for P_D and P_{tot} (μW)[1]
P_D	dynamic power dissipation	per device	5 V	$P_D = 700 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
			10 V	$P_D = 3300 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
			15 V	$P_D = 8900 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$
P_{tot}	total power dissipation	when using the on-chip oscillator	5 V	$P_{tot} = 700 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 690 \times V_{DD}$
			10 V	$P_{tot} = 3300 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 6900 \times V_{DD}$
			15 V	$P_{tot} = 8900 \times f_{osc} + \sum(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 22000 \times V_{DD}$

- [1] Where:
- f_i = input frequency in MHz;
 - f_o = output frequency in MHz;
 - C_L = output load capacitance in pF;
 - V_{DD} = supply voltage in V;
 - $\sum(f_o \times C_L)$ = sum of the outputs;
 - C_t = timing capacitance (pF);
 - f_{osc} = oscillator frequency (MHz).

10.1. Waveforms and test circuit

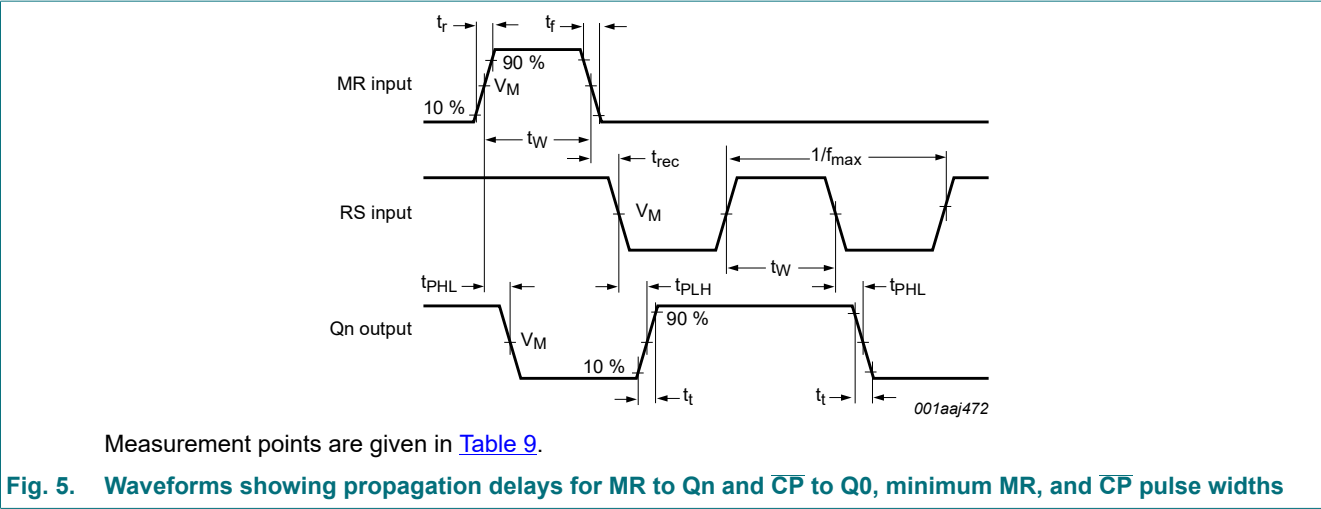


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

14-stage ripple-carry binary counter/divider and oscillator

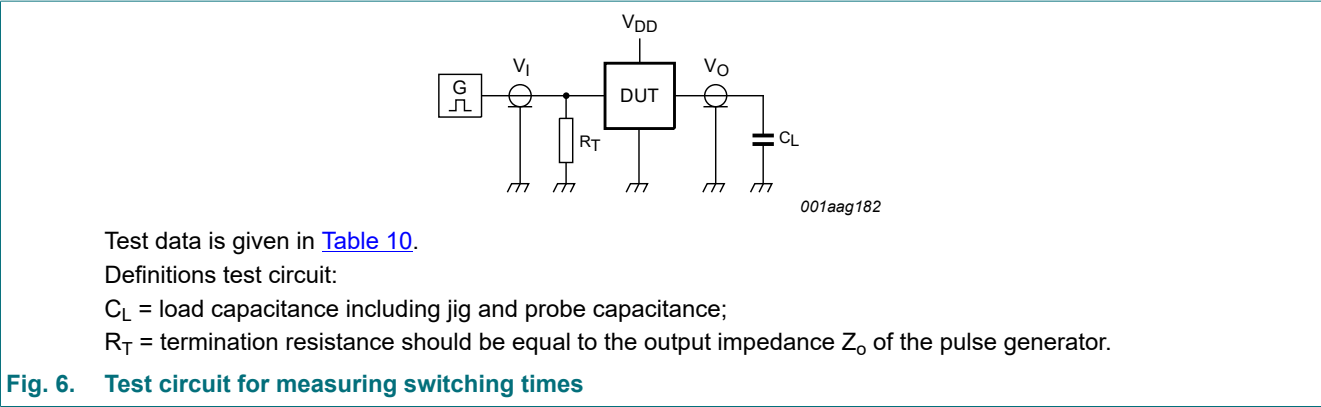
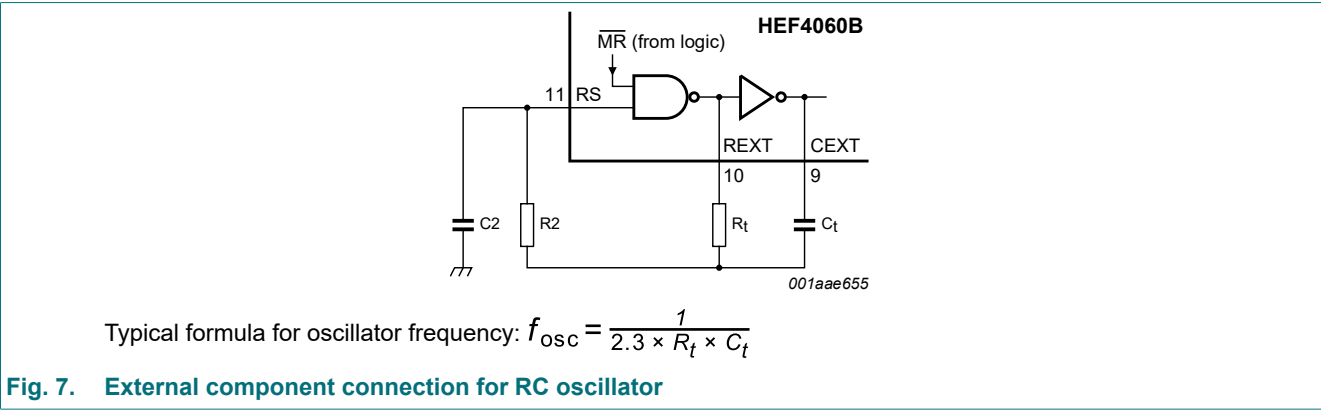


Table 10. Measurement point and test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. RC oscillator



11.1. Timing component limitations

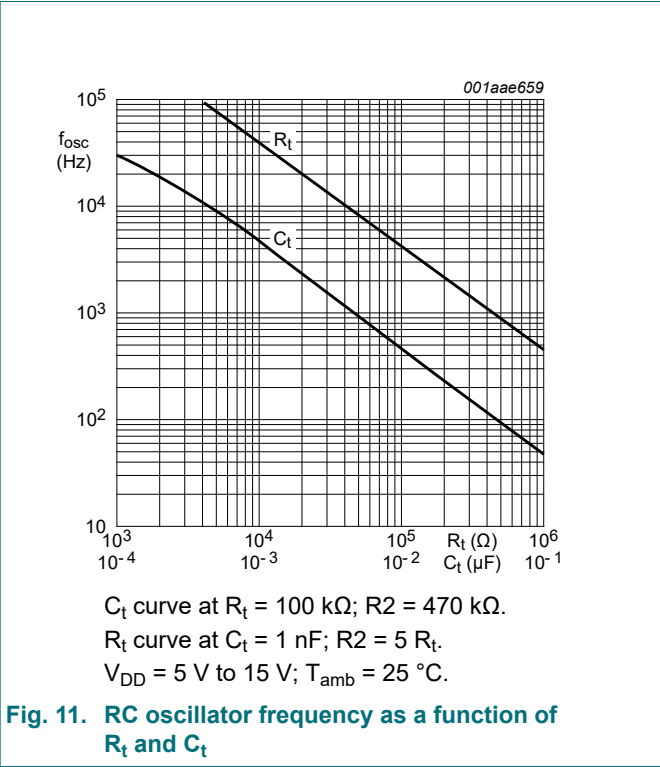
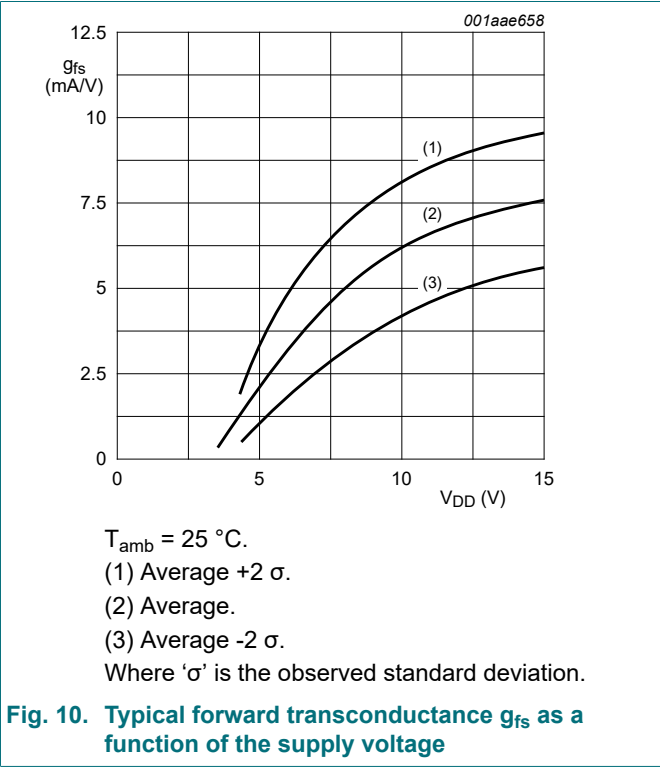
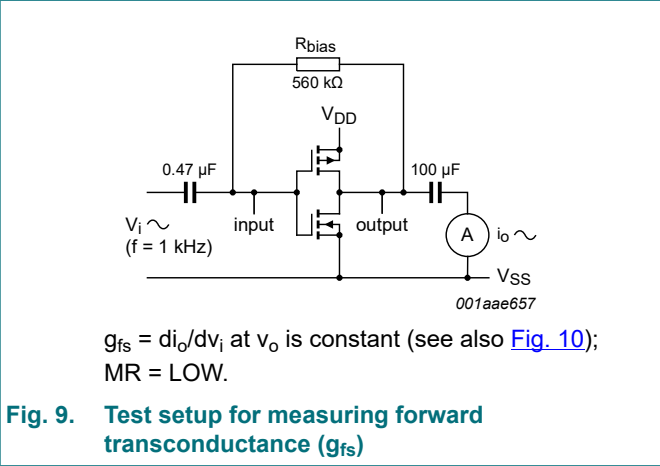
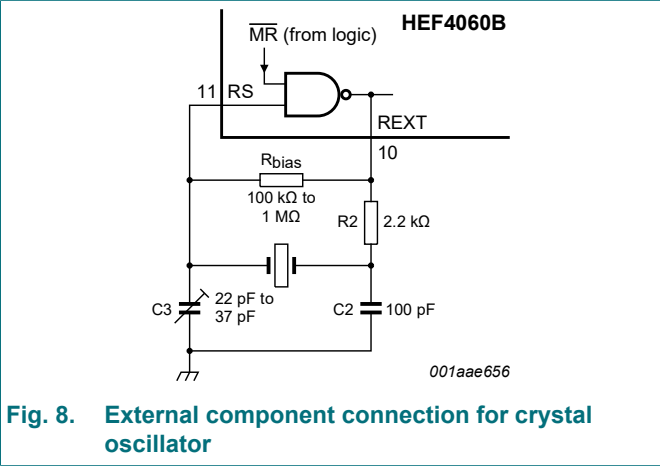
The oscillator frequency is mainly determined by $R_t \times C_t$, provided $R_t \ll R_2$ and $R_2 \times C_2 \ll R_t \times C_t$. The influence of the forward voltage across the input protection diodes on the frequency is minimized by R_2 . The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS (Local Oxidation Complementary Metal-Oxide Semiconductor) 'ON' resistance in series with it, which typically is 500 Ω at $V_{DD} = 5$ V, 300 Ω at $V_{DD} = 10$ V and 200 Ω at $V_{DD} = 15$ V.

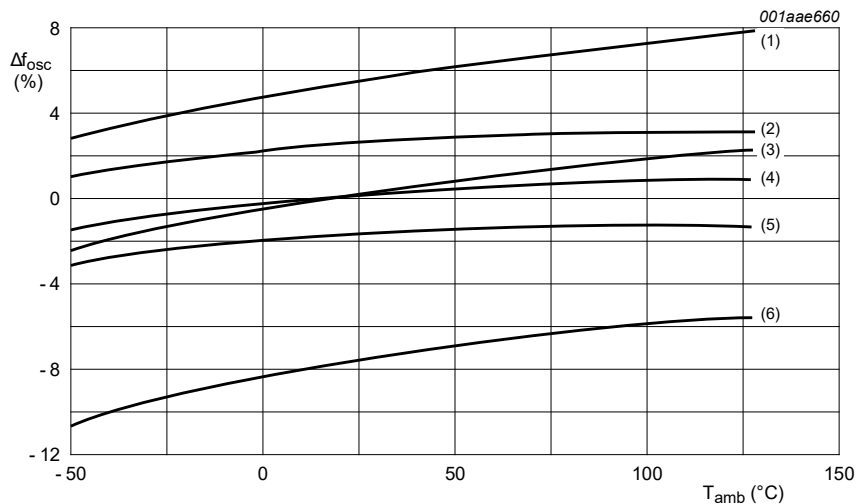
The recommended values for these components to maintain agreement with the typical oscillation formula are:

- $C_t \geq 100$ pF, up to any practical value,
- $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$.

11.2. Typical crystal oscillator circuit

In Fig. 8, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.





Lines (1) and (2): $V_{DD} = 15\text{ V}$.

Lines (3) and (4): $V_{DD} = 10\text{ V}$.

Lines (5) and (6): $V_{DD} = 5\text{ V}$.

Lines (1), (3), (6): $R_t = 100\text{ k}\Omega$; $C_t = 1\text{ nF}$; $R_2 = 0\text{ }\Omega$.

Lines (2), (4), (5): $R_t = 100\text{ k}\Omega$; $C_t = 1\text{ nF}$; $R_2 = 300\text{ k}\Omega$.

Referenced at: f_{osc} at $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_{DD} = 10\text{ V}$.

Fig. 12. Oscillator frequency deviation (Δf_{osc}) as a function of ambient temperature

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

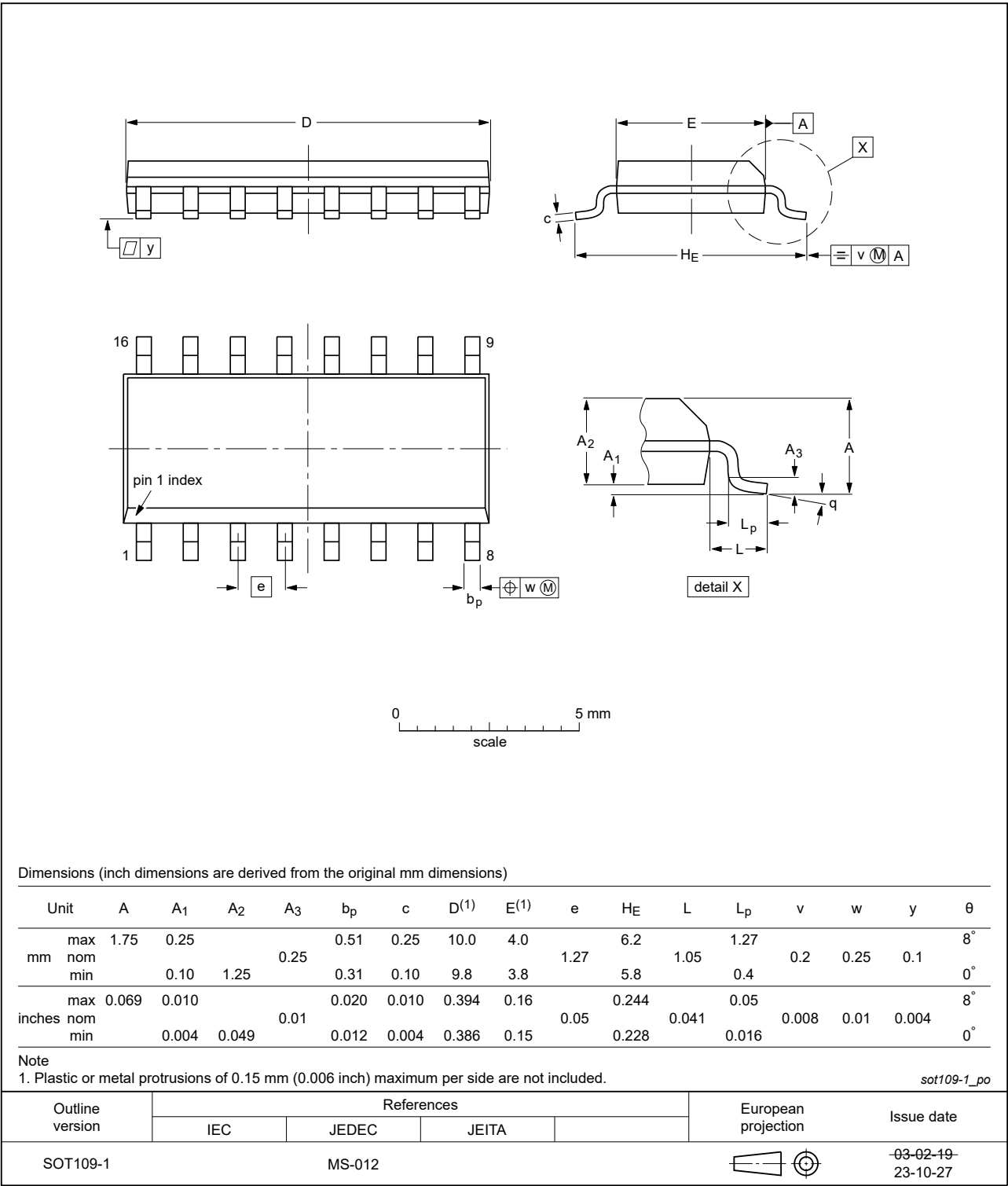


Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

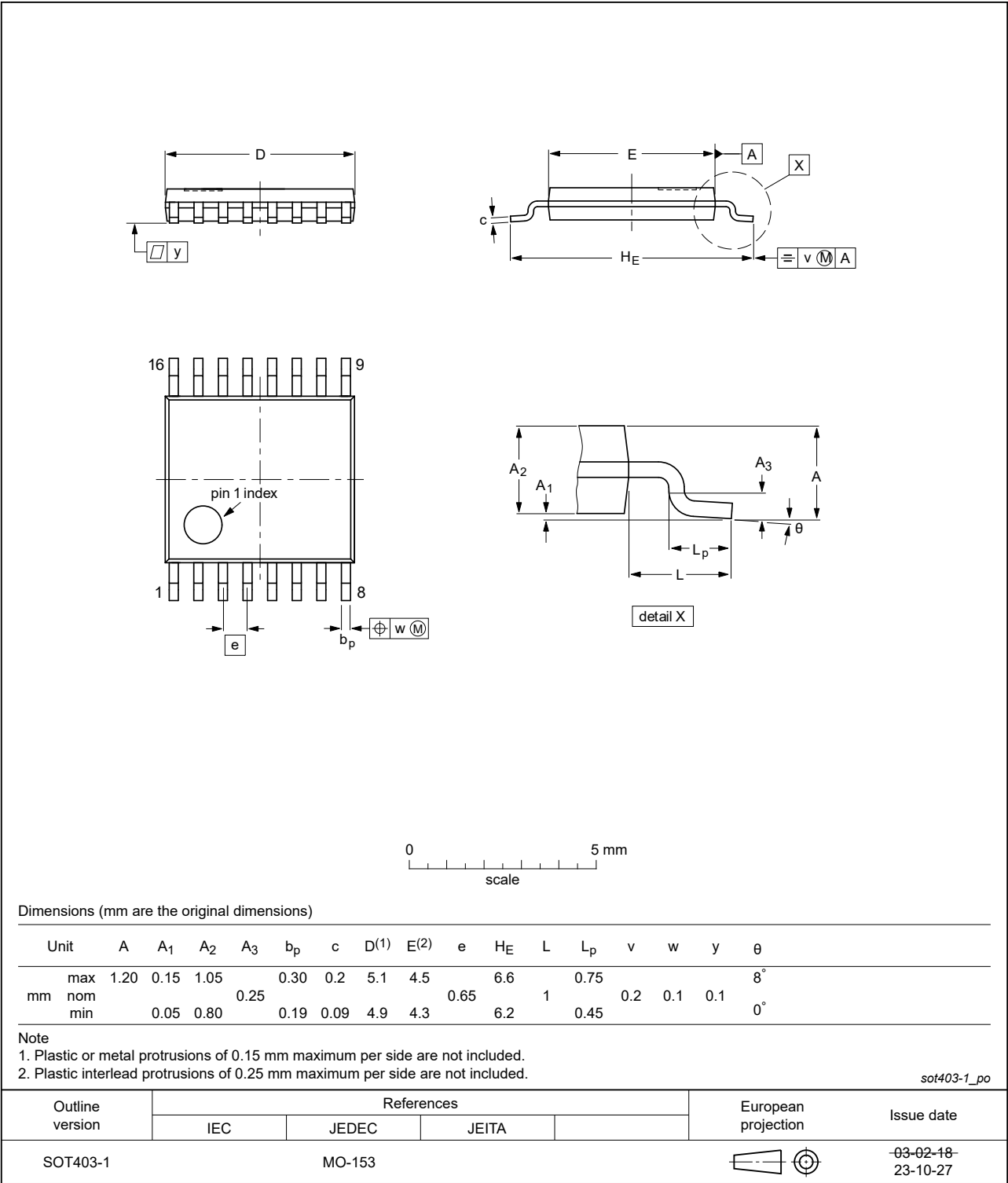


Fig. 14. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4060B v.11	20240903	Product data sheet	-	HEF4060B v.10
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.Fig. 13, Fig. 14: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
HEF4060B v.10	20211108	Product data sheet	-	HEF4060B v.9
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Section 1 and Section 2 updated.			
HEF4060B v.9	20190708	Product data sheet	-	HEF4060B v.8
Modifications:	<ul style="list-style-type: none">Type number HEF4060BTT (SOT403-1/TSSOP16) added.			
HEF4060B v.8	20160325	Product data sheet	-	HEF4060B v.7
Modifications:	<ul style="list-style-type: none">Type number HEF4060BP (SOT38-4) removed.			
HEF4060B v.7	20111116	Product data sheet	-	HEF4060B v.6
Modifications:	<ul style="list-style-type: none">Legal pages updated.Changes in "General description" and "Features and benefits".Section "Applications" removed.			
HEF4060B v.6	20110511	Product data sheet	-	HEF4060B v.5
HEF4060B v.5	20091127	Product data sheet	-	HEF4060B v.4
HEF4060B v.4	20090817	Product data sheet	-	HEF4060B_CNV v.3
HEF4060B_CNV v.3	19950101	Product specification	-	HEF4060B_CNV v.2
HEF4060B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

4. Functional diagram..... 2

5. Pinning information..... 2

5.1. Pinning..... 2

5.2. Pin description..... 3

6. Functional description..... 3

7. Limiting values..... 3

8. Recommended operating conditions..... 4

9. Static characteristics..... 4

10. Dynamic characteristics..... 5

10.1. Waveforms and test circuit..... 6

11. RC oscillator..... 7

11.1. Timing component limitations..... 7

11.2. Typical crystal oscillator circuit..... 8

12. Package outline..... 10

13. Abbreviations..... 12

14. Revision history..... 12

15. Legal information..... 13

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 3 September 2024