12V Synchronous Buck PWM DC-DC

General Description

The RT8101/A are DC/DC synchronous buck PWM controllers with embedded driver support up to 12V+12V boot-strapped voltage for high efficiency power driving. The parts are with full functions of voltage regulation, power monitoring and protection into a single small footprint packages SOP-8 and SOP-8 (Exposed Pad).

The RT8101/A apply a high-gain voltage mode PWM control for simple application design. An internal 0.8V reference allows the output voltage to be precisely regulated to low voltage requirement. The parts are proposed with two type including RT8101 and RT8101A with fixed operating frequency of 300kHz and 600kHz respectively. Based on the features that RT8101/A offered, the parts provide an optimum solution between efficiency, total B.O.M. count, and cost.

Ordering Information

RT8101/A □ □

- Package Type
  - S : SOP-8
  - SP : SOP-8 (Exposed Pad)
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)
- 600kHz
- 300kHz

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

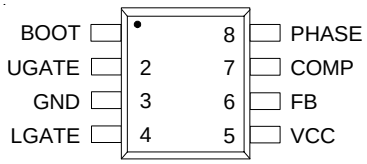
- **Single 12V Bias Supply**
- **Drives All Low Cost N-MOSFETs**
- **High-Gain Voltage Model PWM Control**
- **300kHz/600kHz Fixed Frequency Oscillator**
- **Fast Transient Response :**
  - **High-Speed GM Amplifier**
  - **Full 0 to 100% Duty Ratio**
  - **External Compensation in the Control Loop**
- **Internal Soft-Start**
- **Adaptive Non-Overlapping Gate Driver**
- **Over-Current Fault Monitor on MOSFET, No Current Sense Resistor Required**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

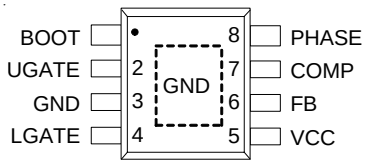
- Graphic Card
- Motherboard, Desktop Servers
- IA Equipments
- Telecomm Equipments
- High Power DC-DC Regulators

Pin Configurations

(TOP VIEW)

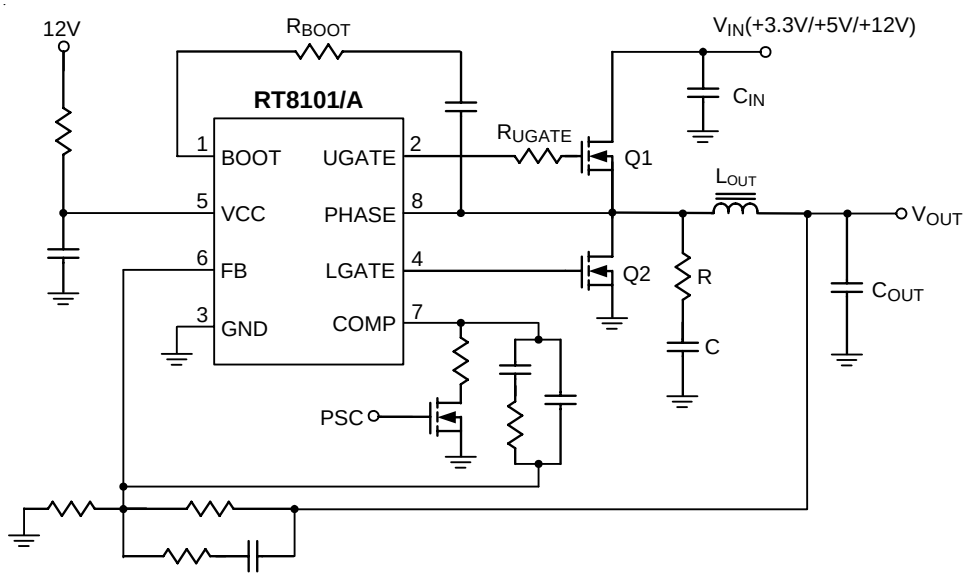


SOP-8



SOP-8(Exposed Pad)

Typical Application Circuit



Functional Pin Description

BOOT (Pin 1)

Bootstrap supply for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

UGATE (Pin 2)

Upper gate driver output. Connect to gate of the high-side power N-Channel MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET is turned off.

GND (Pin 3)

Signal ground for the IC.

LGATE (Pin 4)

Lower gate driver output. Connect to the gate of the low-side power N-Channel MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET is turned off.

VCC (Pin 5)

Connect this pin to a well-decoupled 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.

FB (Pin 6)

Buck converter feedback voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.

COMP (Pin 7)

Buck converter external compensation. This pin is used to compensate the control loop of the buck converter.

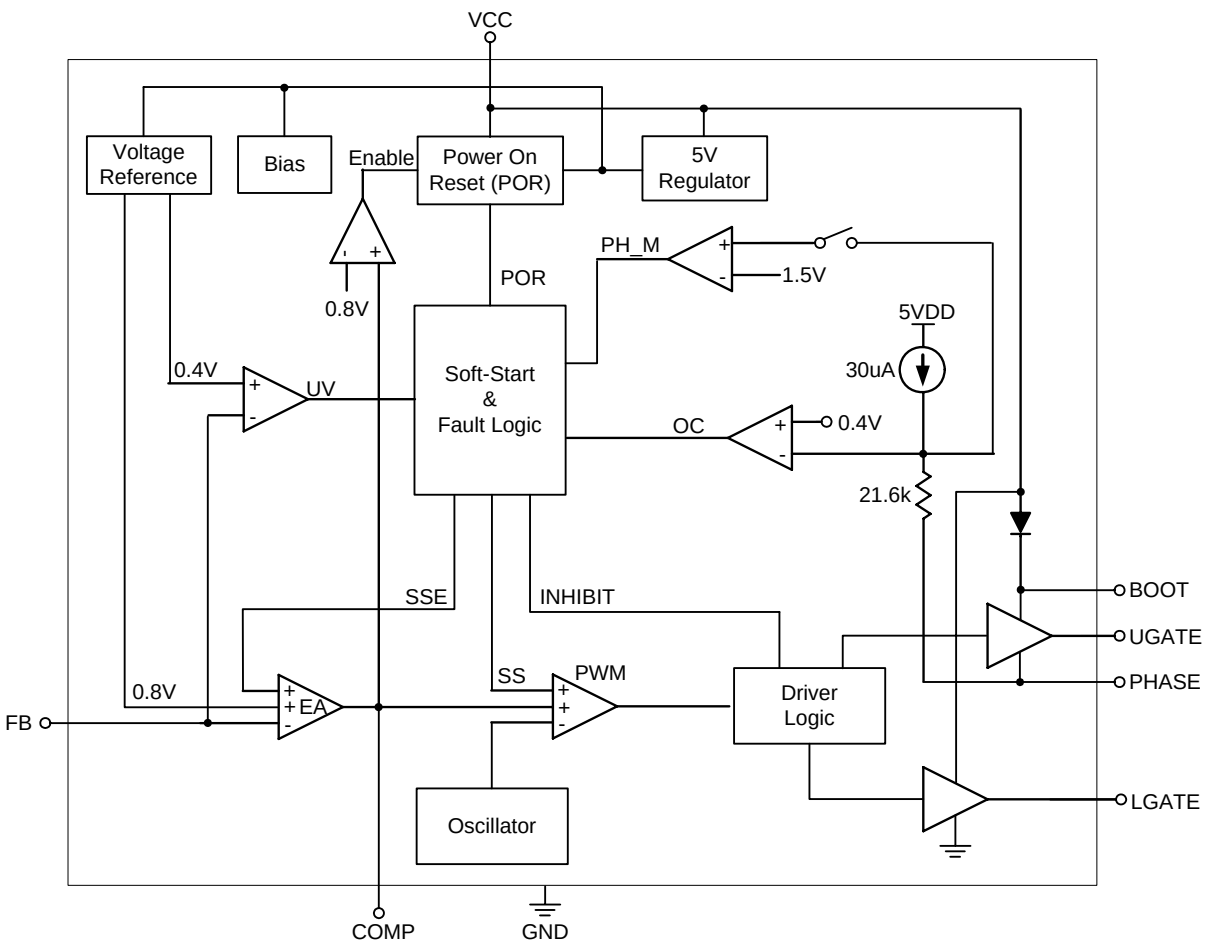
PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET is turned off.

Exposed Pad

Exposed pad should be soldered to PCB board and connected to GND.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 16V
- BOOT, V_{BOOT} - V_{PHASE} ---------- 16V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC}+15V
  - < 200ns ---------- –0.3V to 42V
- UGATE ---------- V_{PHASE} – 0.3V to V_{BOOT} + 0.3V
- LGATE ---------- GND – 0.3V to V_{CC} + 0.3V
- Input, Output or I/O Voltage ---------- GND – 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C (Note 4)
  - SOP-8 ---------- 0.83W
  - SOP-8 (Exposed Pad) ---------- 1.33W
- Package Thermal Resistance
  - SOP-8, θ_{JA} ---------- 120°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}	UGATE and LGATE Open	10.8	12	13.2	V
Supply Current	I_{CC}	V_{CC} = 12V	--	3	--	mA
Power-On Reset						
POR Threshold	V_{CCRTH}		8.8	9.6	10.4	V
POR Hysteresis	V_{CCHYS}		--	0.8	1.6	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC} = 12V, RT8101	250	300	350	kHz
		V_{CC} = 12V, RT8101A	500	600	700	kHz

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	1.5	--	V_{P-P}
Reference Voltage						
PWM Error Amplifier Reference	V_{REF}		0.792	0.8	0.808	V
Error Amplifier						
Open Loop DC Gain	A_O		--	88	--	dB
Gain-Bandwidth Product	GBW		--	15	--	MHz
Slew Rate	SR		--	6	--	V/us
PWM Controller Gate Drivers (V_{CC} = 12V)						
Upper Gate Source	I_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{BOOT} - V_{UGATE}$ = 6V	--	300	--	mA
Upper Gate Source	R_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{BOOT} - V_{UGATE}$ = 1V	--	7	10	Ω
Upper Gate Sink	R_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{UGATE} - V_{PHASE}$ = 1V	--	4	8	Ω
Lower Gate Source	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	--	500	--	mA
Lower Gate Source	R_{LGATE}	$V_{CC} - V_{LGATE}$ = 1V	--	4	6	Ω
Lower Gate Sink	R_{LGATE}	V_{LGATE} = 1V	--	2	4	Ω
Protection						
Under Voltage Protection		Measuring V_{FB}	0.3	0.4	0.5	V
Over Current Threshold	V_{OC}	Measuring V_{PHASE}	–210	–250	–290	mV
Soft-Start Interval	T_{SS}		2	3.2	4.2	ms

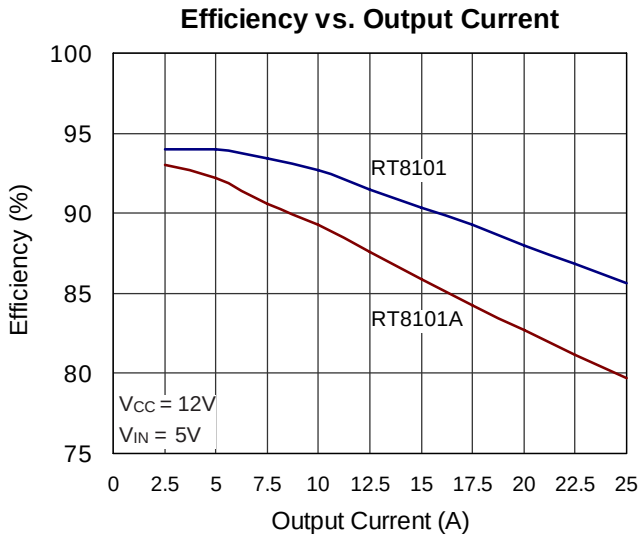
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

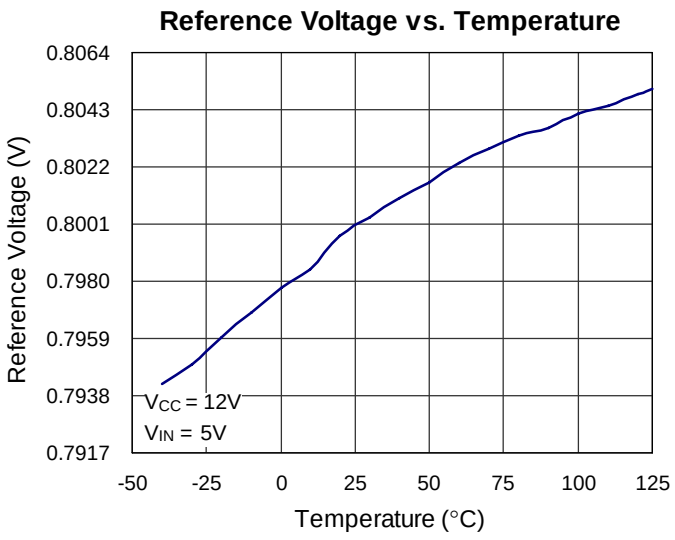
Note 2. Devices are ESD sensitive. Handling precaution recommended.

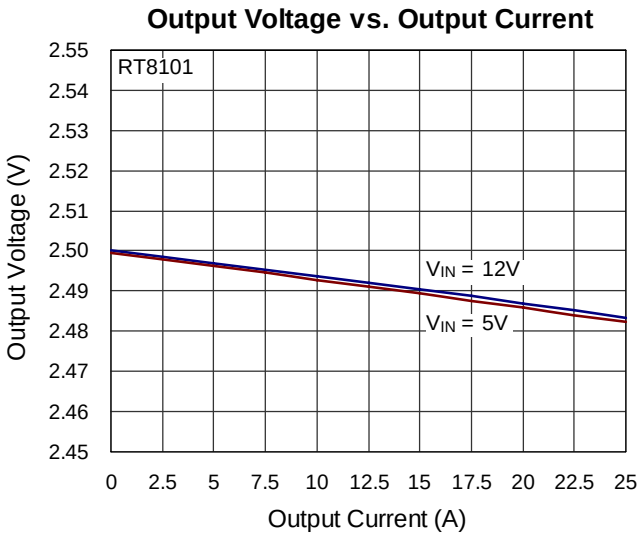
Note 3. The device is not guaranteed to function outside its operating conditions.

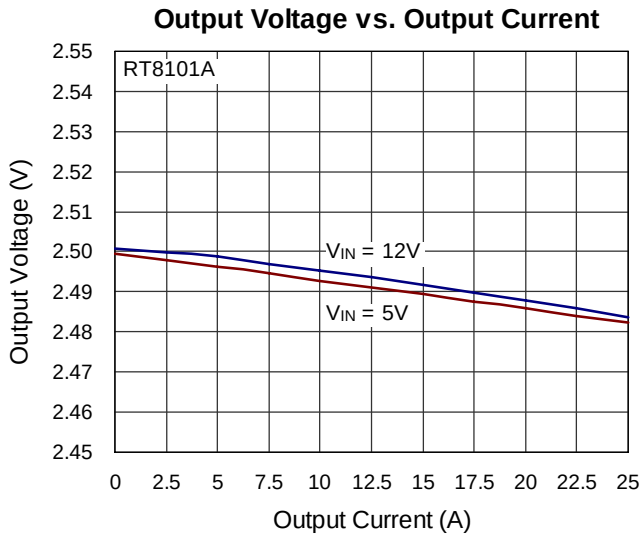
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

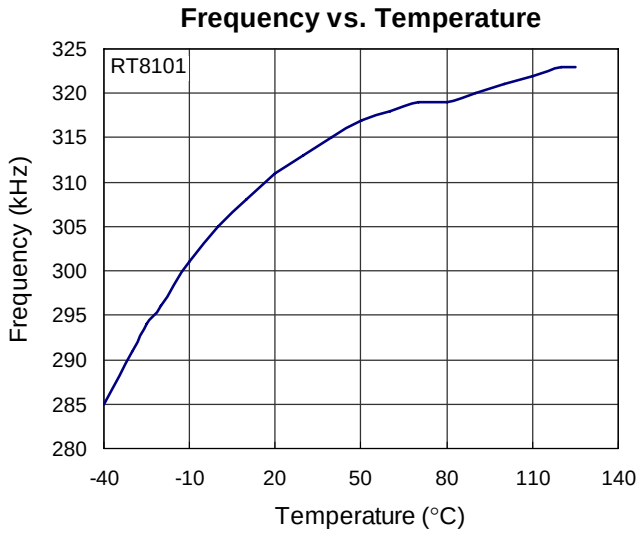
Typical Operating Characteristics

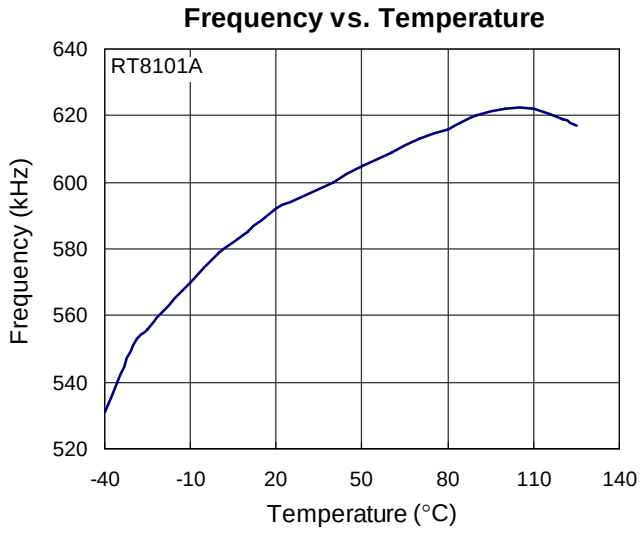




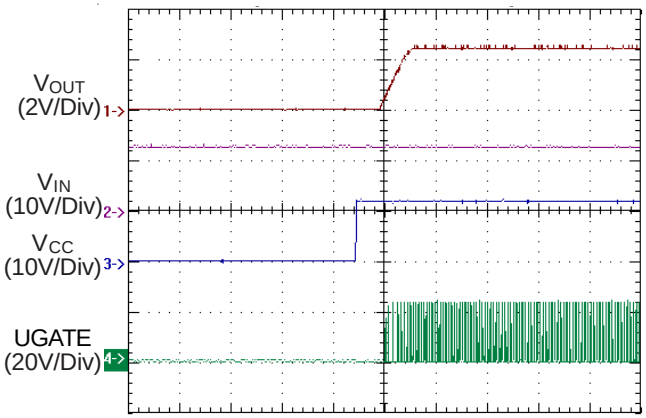




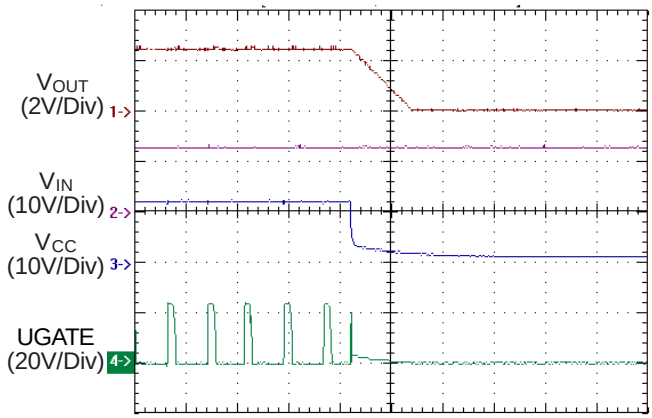




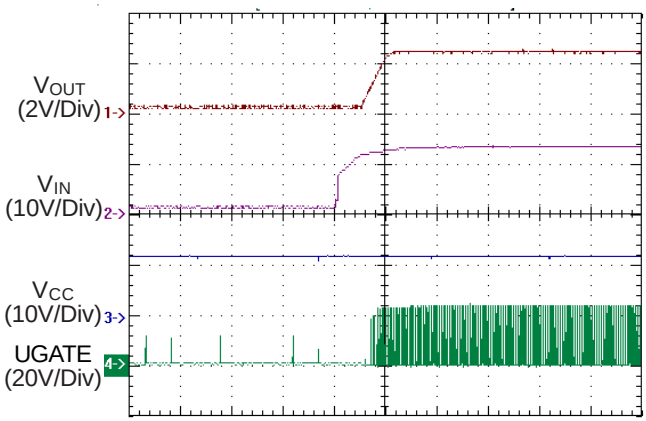
Power On from V_{CC}



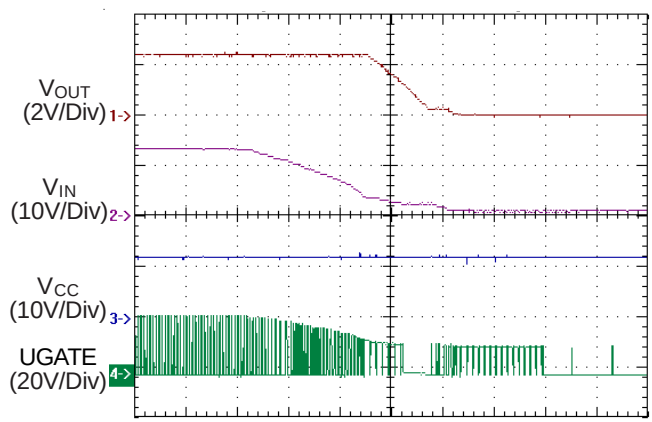
Power Off from V_{CC}



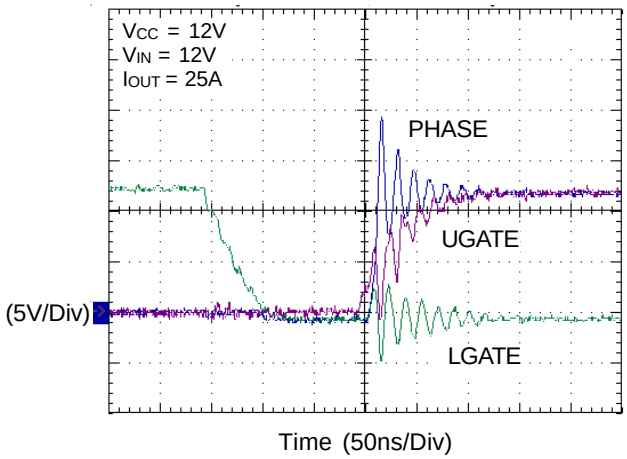
Power On from V_{IN}



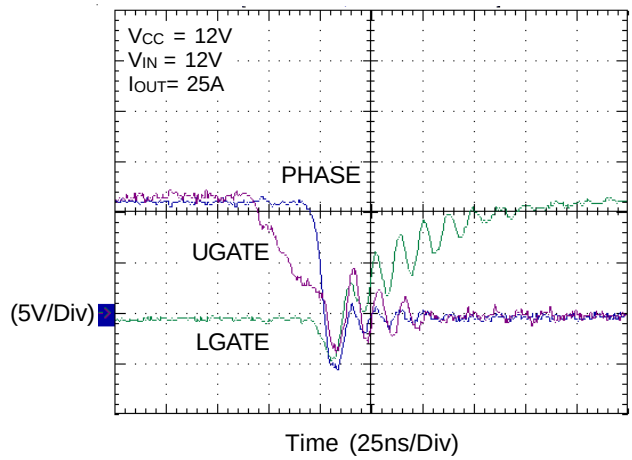
Power On from V_{IN}



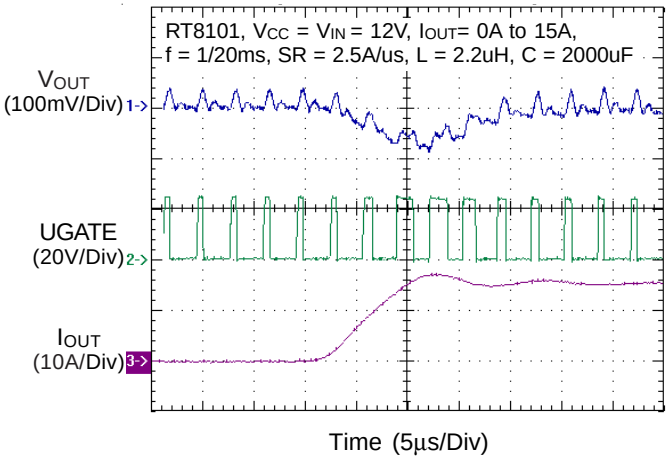
Dead Time (Rising)



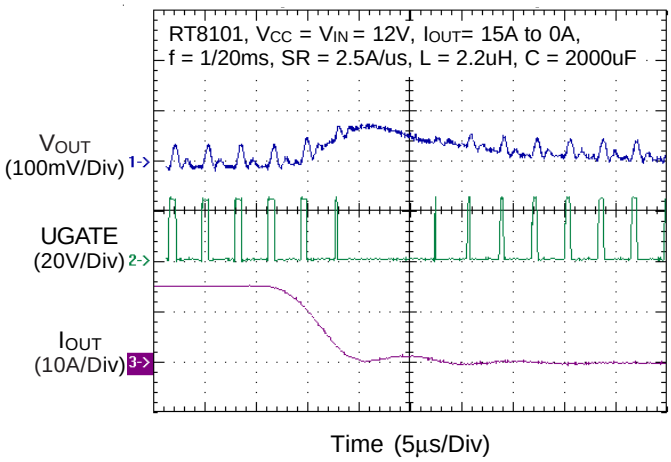
Dead Time (Falling)



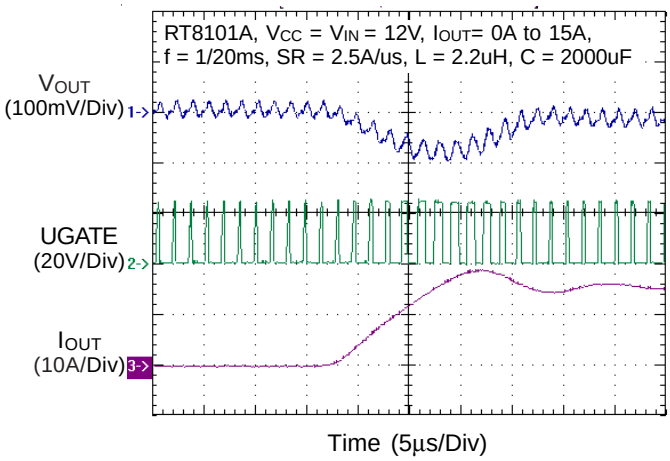
Transient Response (Rising)



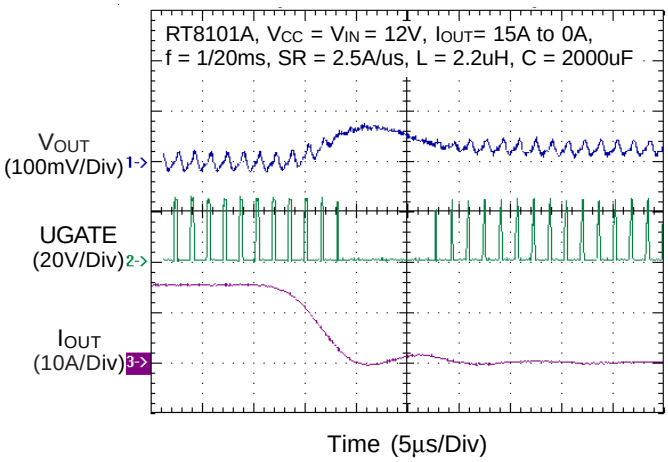
Transient Response (Falling)



Transient Response (Rising)



Transient Response (Falling)



Application Information

Power On Reset

The RT8101/A automatically initializes upon applying of input power V_{CC}. The power on reset function (POR) continually monitors the input bias supply voltage at the VCC pin. The POR trip level is typically 9.6V at VCC rising.

VIN Detection

After POR the RT8101/A continuously generates a 10kHz pulse train with 1μs pulse width to turn on the upper MOSFET for detecting the existence of V_{IN}. RT8101/A keeps monitoring PHASE pin voltage during the detection period.

As soon as the PHASE voltage crosses 1.5V two times, V_{IN} existence is recognized and the RT8101/A initiates its soft start cycle as described in next section.

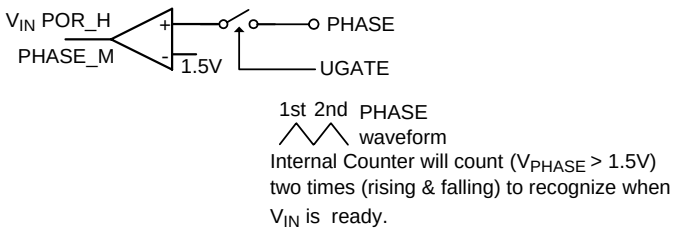


Figure 1

Soft Start

A built-in soft-start is used to prevent surge current from V_{IN} to V_{OUT} during power on. After the existence of V_{IN} is detected, soft-start (SS) begins automatically. The feedback voltage (V_{FB}) is clamped by internal linear ramping up SS voltage, causing PWM pulse width increasing slowly and thus inducing little surge current. Soft-start completes when SS voltage exceeds internal reference voltage (0.8V), the time duration is about 3.2ms.

Over Current Protection

The RT8101/A senses the current flowing through lower MOSFET for over current protection (OCP) by sensing the PHASE pin voltage as shown in the Functional Block Diagram.

A 30μA current source flows through the internal resistor 21.6kΩ to PHASE pin causing 0.65V voltage drop across the resistor. OCP is triggered if the voltage at PHASE pin (drop of lower MOSFET V_{DS}) is lower than –0.25V when low side MOSFET conducting. Accordingly inductor current threshold for OCP is a function of conducting resistance of lower MOSFET $R_{DS(ON)}$ as :

$$I_{OCSET} = \frac{30\mu A \times 21.6k\text{-}0.4V}{R_{DS(ON)}}$$

If MOSFET with $R_{DS(ON)}$ = 10mΩ is used, the OCP threshold current is about 25A. Once OCP is triggered, the RT8101/A enters hiccup mode and re-soft starts again. The RT8101/A shuts down after OCP hiccups twice.

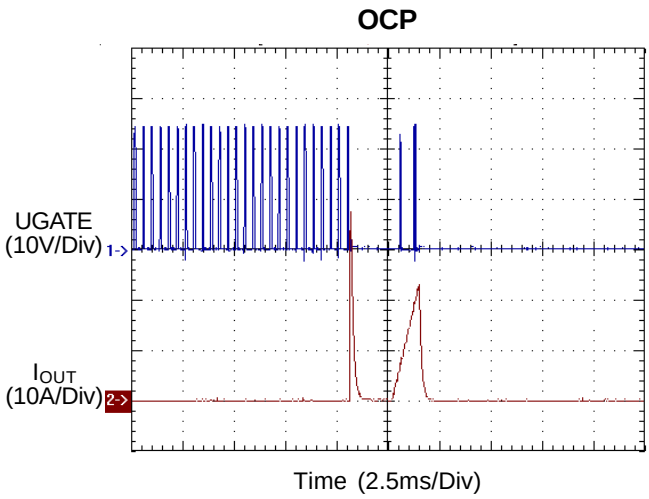


Figure 3. Power On then Shorted

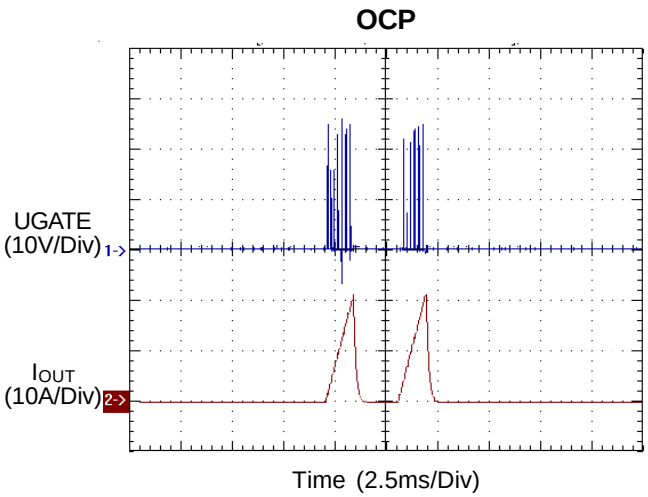


Figure 4. Shorted then Power On

Feedback Compensation

The RT8101/A is a voltage mode controller. The control loop is a single voltage feedback path including a compensator and modulator as shown in Figure 5. The modulator consists of the PWM comparator and power stage. The PWM comparator compares error amplifier EA output (COMP) with oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier. A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability.

In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (greater than 45 degrees) and the highest 0dB crossing frequency. It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of –20dB/dec.

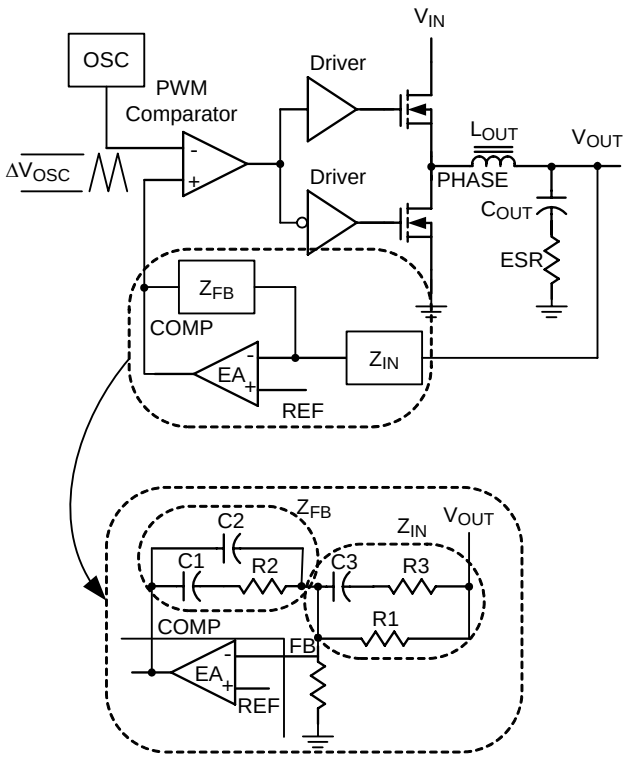


Figure 5. Closed Loop

1) Modulator Frequency Equations

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output. This transfer function is dominated by a DC gain, a double pole, and a zero as shown in Figure 7. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as below:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as follows :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as shown in Figure 6.

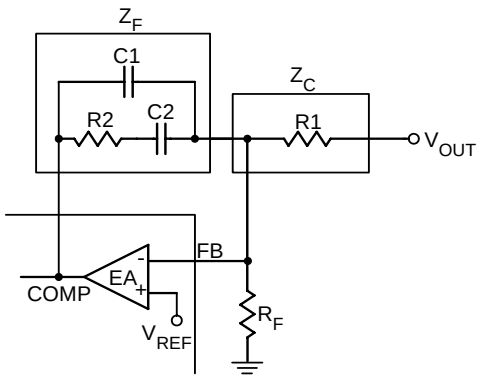


Figure 6. Compensation Loop

$$f_{Z1} = \frac{1}{2\pi \text{ x } R2 \text{ x } C2}$$

$$f_{P1} = \frac{1}{2\pi \text{ x } R2 \text{ x } \frac{C1 \text{ x } C2}{C1 + C2}}$$

Figure 7 shows the DC-DC converter's gain vs. frequency. The compensation gain uses external impedance networks Z_C and Z_F to provide a stable, high bandwidth loop. High crossover frequency is desirable for fast transient response, but it often jeopardizes the system stability. In order to cancel one of the LC filter poles, place the zero before the LC filter resonant frequency. In the experience, place the zero at 75% LC filter resonant frequency. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The second pole is placed at half of the switching frequency.

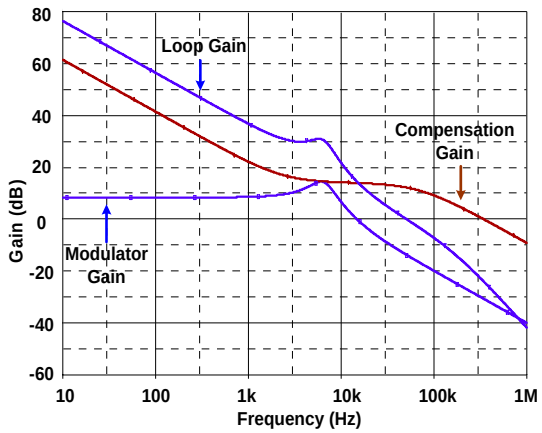
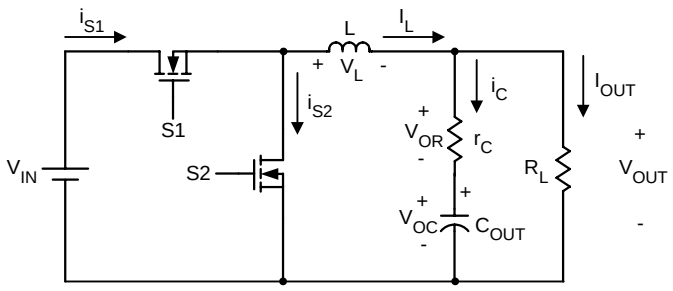


Figure 7. Bode Plot

Component Selection

1) Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. Low inductance value has smaller size, but results in low efficiency, large ripple current and high output ripple voltage. Generally, an inductor that limits the ripple current (ΔI_L) between 20% and 50% of the output current is appropriate. Figure 8 shows the typical topology of synchronous step-down converter and its related waveforms.



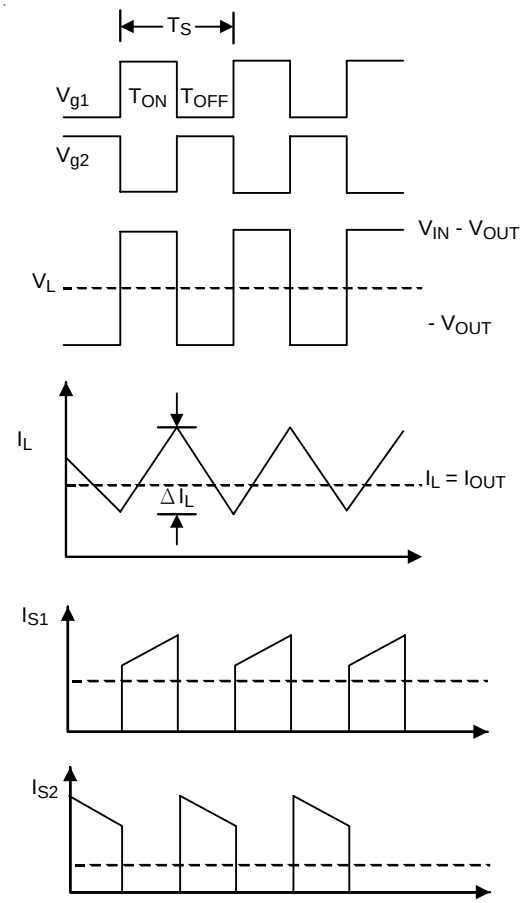


Figure 8. The waveforms of synchronous step-down converter

According to Figure 8 the ripple current of inductor can be calculated as follows :

$$V_{IN} - V_{OUT} = L\frac{\Delta I_L}{\Delta t};\quad \Delta t = \frac{D}{fs};\quad D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times fs \times \Delta I_L} \qquad (1)$$

Where :

V_{IN} = Maximum input voltage

V_{OUT} = Output Voltage

Δt = S1 turn on time

ΔI_L = Inductor current ripple

f_S = Switching frequency

D = Duty Cycle

r_C = Equivalent series resistor of output capacitor

2) Output Capacitor

The selection of output capacitor depends on the output ripple voltage requirement. Practically, the output ripple voltage is a function of both capacitance value and the equivalent series resistance (ESR) r_C. Figure 9 shows the related waveforms of output capacitor.

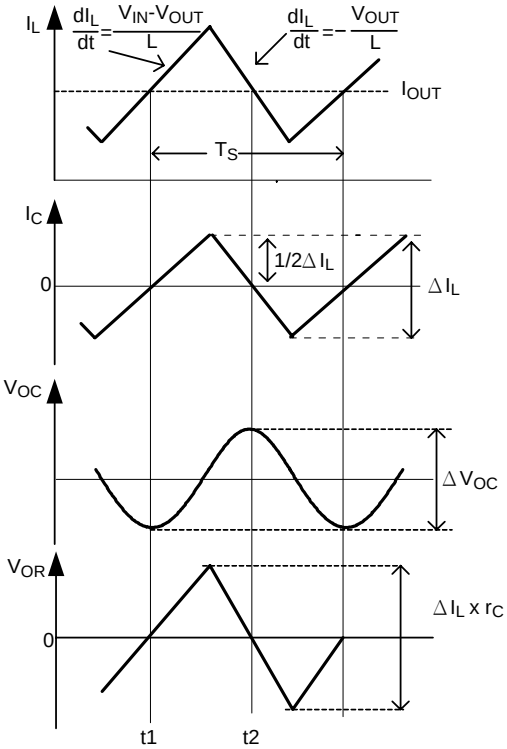


Figure 9. The related waveforms of output capacitor

The AC impedance of output capacitor at operating frequency is quite smaller than the load impedance, so the ripple current (ΔI_L) of the inductor current flows mainly through output capacitor. The output ripple voltage is described as :

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC} \quad (2)$$

$$\Delta V_{OUT} = \Delta I_L \times r_C + \frac{1}{C_O}\int_{t1}^{t2} I_C \, dt \quad (3)$$

$$\Delta V_{OUT} = \Delta I_L \times \Delta I_L \times r_C + \frac{1}{8}\frac{V_{OUT}}{C_{OL}}(1-D)T_S^2 \quad (4)$$

where ΔV_{OR} is caused by ESR and ΔV_{OC} by capacitance. For electrolytic capacitor application, typically 90 to 95% of the output voltage ripple is contributed by the ESR of output capacitor. So Equation (4) could be simplified as :

$$\Delta V_{OUT} = \Delta I_L \times r_C \quad (5)$$

Users could connect capacitors in parallel to get calculated ESR.

3) Input Capacitor

The selection of input capacitor is mainly based on its maximum ripple current capability. The buck converter draws pulsewise current from the input capacitor during the on time of S1 as shown in Figure 8. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{rms} = I_{OUT}\sqrt{D(1-D)} \ \ (A) \quad (6)$$

The input capacitor must be capable of handling this ripple current. Sometimes, for higher efficiency the low ESR capacitor is necessarily.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8101/A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent.

The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (120°C/W) = 0.83W for SOP-8 packages

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.33W for PSOP-8 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8101/A packages, Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

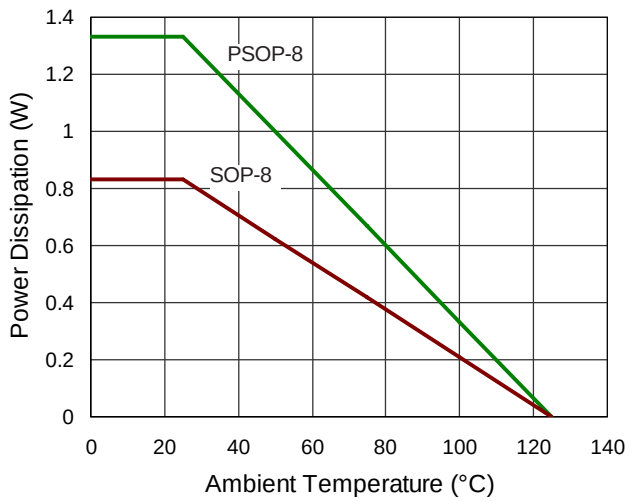


Figure 10. Derating Curves for RT8101/A Packages

PCB Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode.

Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the RT8101/A. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by MOSFETs. A multi-layer printed circuit board is recommended. Figure 11 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each of them represents numerous physical capacitors.

Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but it is not necessary to oversize this particular island. Since the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

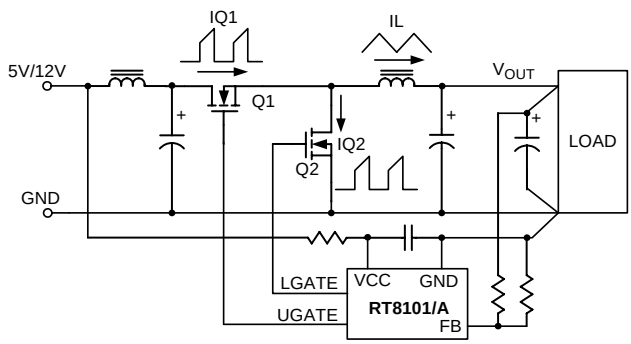
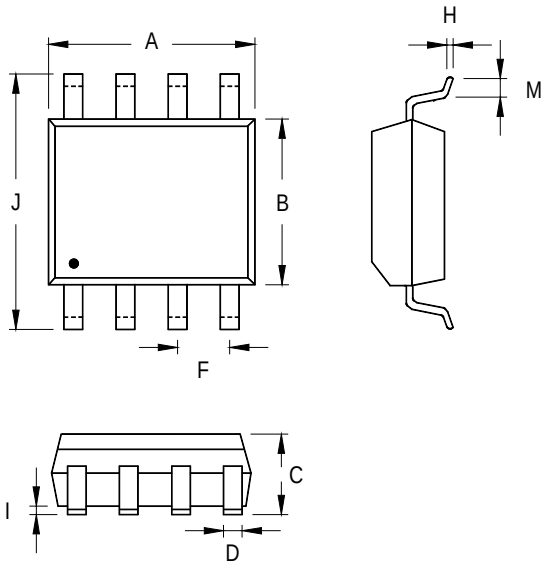


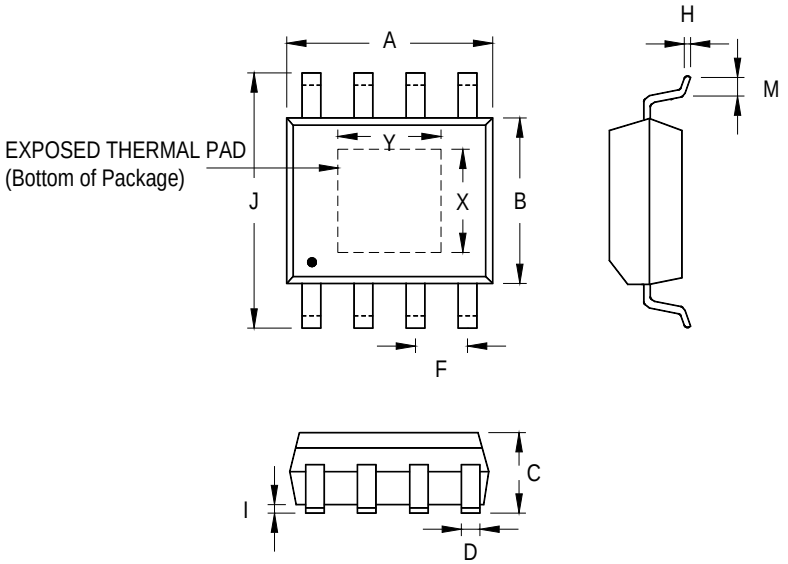
Figure 11. The connections of the critical components in the converter

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	4.000	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.510	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.200	0.228	0.244
M	0.406	1.270	0.016	0.050
X	1.900	2.700	0.075	0.106
Y	1.900	3.600	0.075	0.142

8-Lead SOP (Exposed Pad) Plastic Package

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