JSR364Gxx8Nxx-SU

4Gb DDR3(L) SDRAM

78FBGA & 96FBGA with Lead-Free&Halogen-Free
(RoHS compliant)

Product Ordering Information

Voltage	Organization	DDR3-1866 (13-13-13)	DDR3-2133 (14-14-14)	Package
DDR3 (1.5V)	512M x 8	JSR364G088NHW-SU	JSR364G088NHW-A-SU	78FBGA
DDR3 (1.5V)	256M x 16	JSR364G168NHR-SU	JSR364G168NHR-A-SU	96FBGA
DDR3L (1.35V)	512Mb x 8	JSR364G088NHW-L-SU	JSR364G088NHW-LA-SU	78FBGA
DDR3L (1.35V)	256Mb x 16	JSR364G168NHR-L-SU	JSR364G168NHR-LA-SU	96FBGA

4Gb DDR3(L) SDRAM Specification

Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
  - Supports DDR3L devices to be backward compatible in 1.5V applications
- Differential bidirectional data strobe
- 8*n*-bit prefetcharchitecture
- Differential clock inputs (CK, CKB)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Selfrefreshmode
- T_C of -40°C to + 95°C
  64ms, 8192-cycle refresh at -10°C to +85°C
  32ms at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Writeleveling
- Multipurposeregister
- Outputdrivercalibration

Options

- Configuration
  - 512 Meg x 8
  - 256 Meg x 16
- FBGA package (Pb-free) – x8
  78-ball (7.5mm x 11.0mm)
- FBGA package (Pb-free) – x16
  96-ball (7.5mm x 13.0mm)
- Timing – cycle time
  - 0.938ns @ CL = 14 (DDR3-2133)
  - 1.071ns @ CL = 13 (DDR3-1866)
  - 1.250ns @ CL = 11 (DDR3-1600)
- Operating temperature
  - Industrial (-40°C ≤ T_C ≤ +95°C)

Key Timing Parameters

Speed Grade	Data Rate (MT/s)	^tRCD-^tRP-CL	^tCK (ns)	^tRCD (ns)	^tRP (ns)	CL (ns)
-A 1.2	2133	14-14-14	0.938	13.09	13.09	13.09
- 1	1866	13-13-13	1.071	13.91	13.91	13.91
-	1600	11-11-11	1.25	13.75	13.75	13.75

Notes: 1. Backward compatible to 1600, CL = 11
2. Backward compatible to 1866, CL = 13

Addressing

Parameter	512 Meg x 8	256 Meg x 16
Configuration	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	64K (A[15:0])	32K (A[14:0])
Bank address	8 (BA[2:0])	8 (BA[2:0])
Column address	1K (A[9:0])	1K (A[9:0])
Page size	1KB	2KB

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JSR3 X XX XX X N XX - XX X XX

Suntsu

Temperature Range
Blank : Industrial

Speed
Blank: 933Mhz (1866Mbps, 13-13-13)
A : 1066Mhz (2133Mbps, 14-14-14)

Voltage
Blank : DDR3 (1.5V, 1.5V)
L : DDR3L (1.35V, 1.35V)

Package
HW : 78-Ball FBGA(7.5x11.0)
HR : 96-Ball FBGA(7.5x13.0)

Bank
8 : 8 Banks

Organization
08 : x8 bits
16 : x16 bits

Density
4G : 4Gb

DRAM
6 : DRAM Supplier

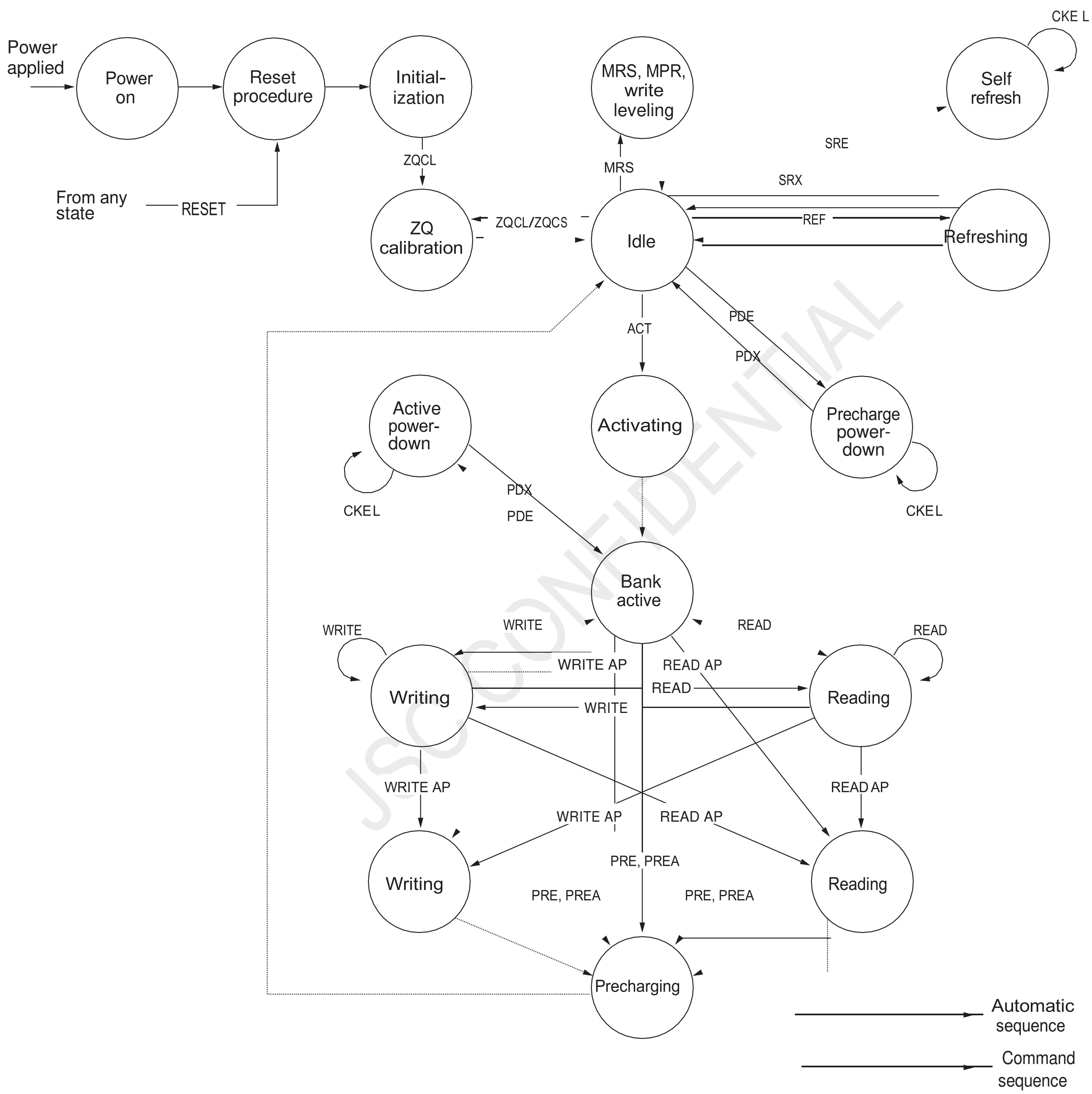
JSC Commodity DDR3

Contents

Revision No	Description	Date
0.0	Initial Release	2019/05/03
1.0	Update POD	2019/11/13
1.1	Update specification of 2133Mbps and Ordering Information	2020/03/13
1.2	Change TYPO : x16 device (A15 → A14)	2021/04/02
1.3	Update operating temperature range	2021/04/22
1.4	Change TYPO	2021/06/23
1.5	Update operating temperature range	2024/04/29

State Diagram

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit PRE
= PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Functional Description

DDR3 SDRAM uses a double data rate architecture to achievehigh-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfertwo data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of asingle 8*n*-bit-wide, four-clock- cycle data transfer at the internal DRAM core and eight corresponding *n*- bit-wide, one- half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3SDRAM operates from a differential clock(CKandCKB). The crossing of CK going HIGH and CKB going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start ata selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function maybe enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high band width by hiding row pre-charge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < -40°C or >95°C.

General Notes

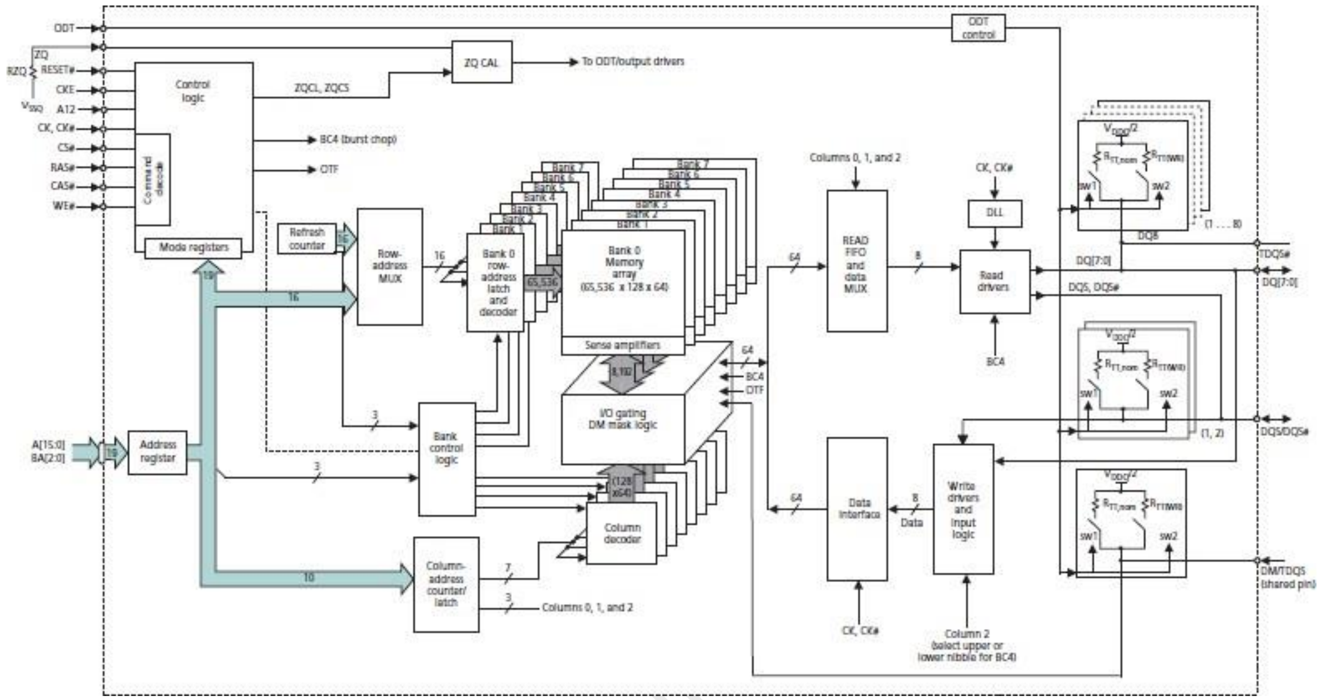
- The functionality and the timing specifications discussed in this data sheet are for the DLLenable mode of operation(normal operation).
- Through out this datasheet,various figures and textrefer to DQsas“DQ.”DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms“DQS”and“CK” found through out this datasheet are to be interpreted as DQS,DQS# andCK, CKB respectively, unless specifically stated otherwise.

- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[n:0]. *For example,* 1Gb: n = 12 (x16); 1Gb: n = 13 (x4, x8); 2Gb: n = 13 (x16) and 2Gb: n = 14 (x4, x8); 4Gb: n = 14 (x16); and 4Gb: n = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus iscomprisedof two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor.
  - Connect UDQS# to V_{DD} via 1kΩ* resistor.
  - Connect UDM to V_{DD} via1kΩ* resistor.
  - Connect DQ[15:8] individually to either V_{SS}, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

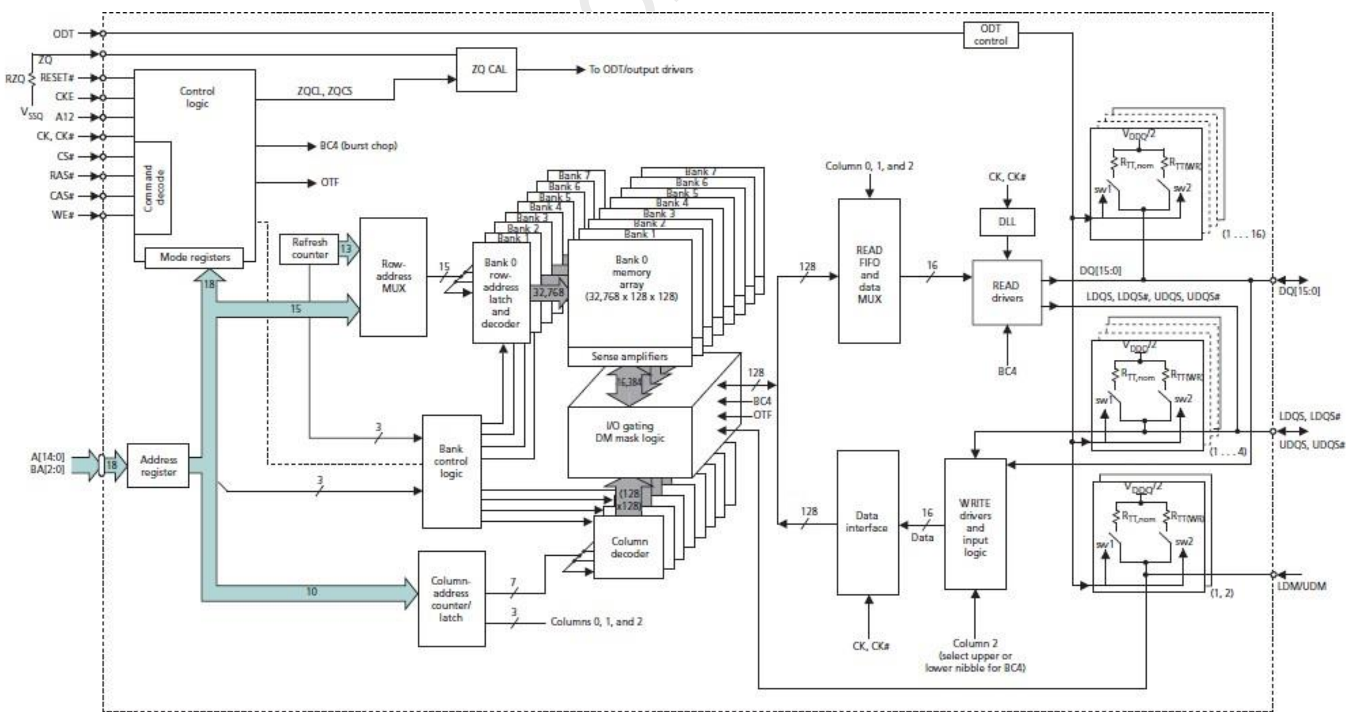
Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

512 Meg x 8 Functional Block Diagram



256 Meg x 16 Functional Block Diagram



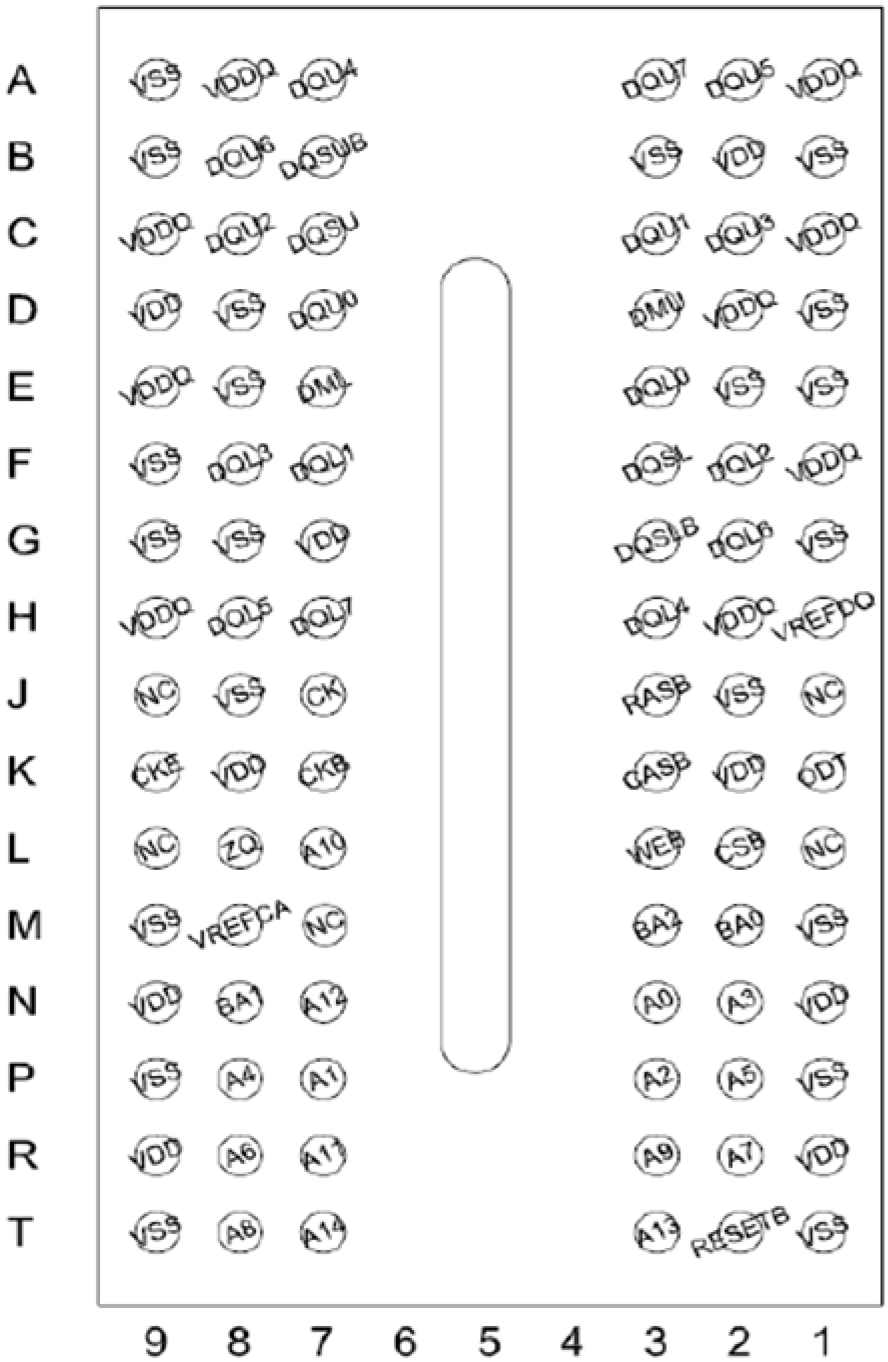
Ball Assignments and Descriptions

78-Ball FBGA – x8 (Bottom View)

	9	8	7	6	5	4	3	2	1
A	VDD	VSS	DMU				NC	VDD	VSS
B	VDDQ	VSS	DML				DQ0	VSS	VSS
C	VSS	DQ3	DQ1				DQS	DQ2	VDDQ
D	VSS	VSS	VDD				DQSB	DQ6	VSS
E	VDDQ	DQ5	DQ7				DQ4	VDDQ	VREF_DQ
F	NC	VSS	CK				RASB	VSS	NC
G	CKE	VDD	CKB				CASB	VDD	ODT
H	NC	ZQ	A10				WEB	CSB	NC
J	VSS	VREF_CA	A15				BA2	BA0	VSS
K	VDD	BA1	A12				A0	A3	VDD
L	VSS	A4	A1				A2	A5	VSS
M	VDD	A6	A11				A9	A7	VDD
N	VSS	A8	A14				A13	RESETB	VSS

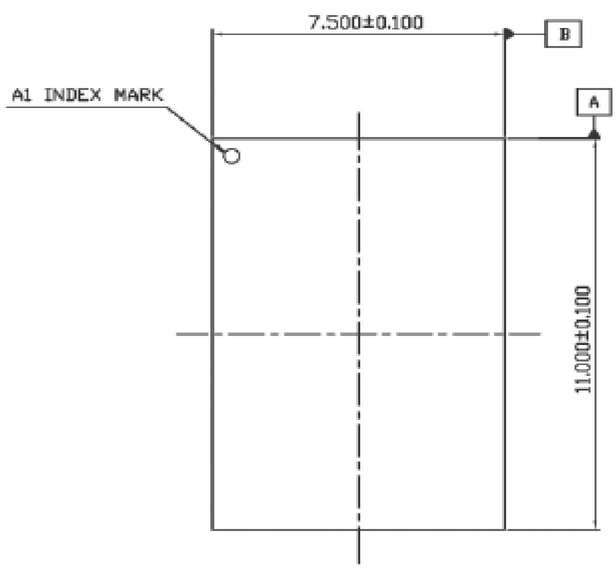
Ball Assignments and Descriptions

96-Ball FBGA – x16 (Bottom View)

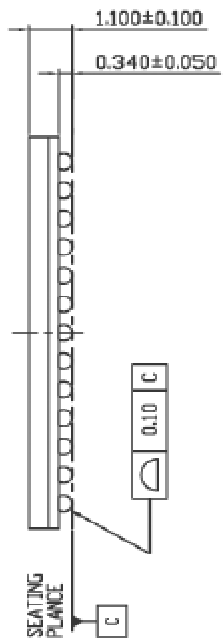


Package Dimensions

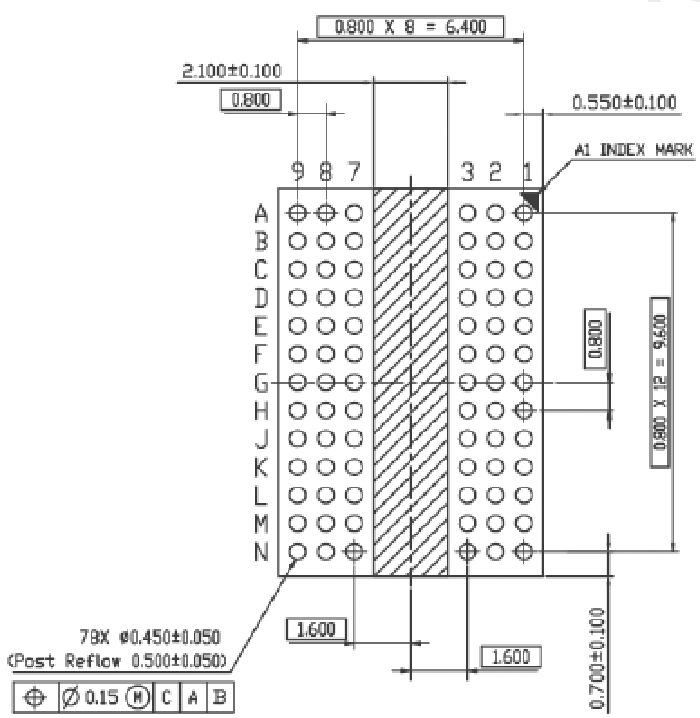
78-Ball FBGA- x8



TOP VIEW

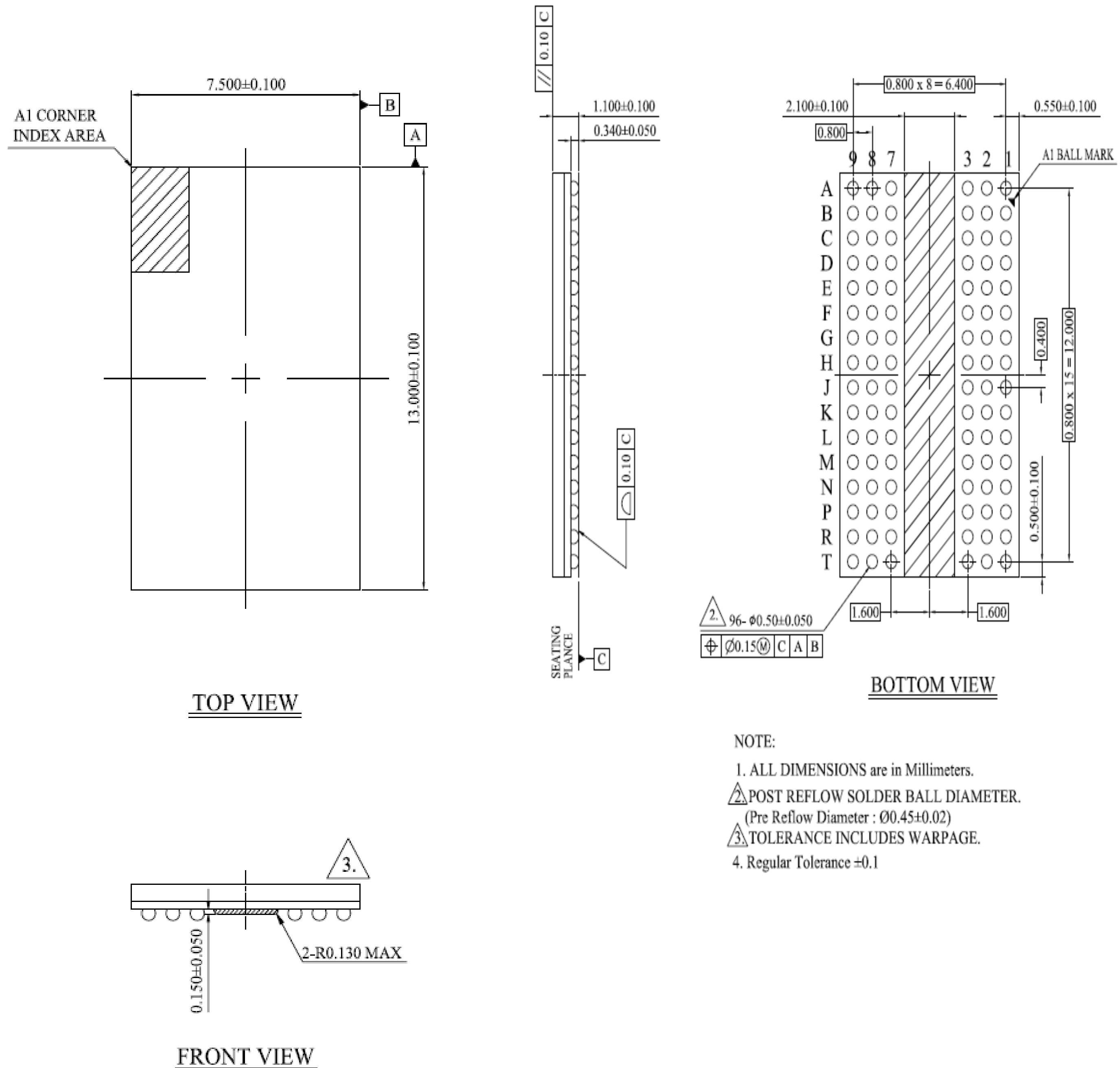


SIDE VIEW



BOTTOM VIEW

96-Ball FBGA-x16



NOTE:

1. ALL DIMENSIONS are in Millimeters.
2. POST REFLOW SOLDER BALL DIAMETER. (Pre Reflow Diameter : Ø0.45±0.02)
3. TOLERANCE INCLUDES WARPAGE.
4. Regular Tolerance ±0.1

78-Ball FBGA – x8 Ball Descriptions

Symbol	Type	Description
A[15:13], A12, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq$ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.

78-Ball FBGA -x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained atalltimes(including selfrefresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

96-Ball FBGA - x16 Ball Descriptions

Symbol	Type	Description
A[14:13], A12, A11, A10, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CKB	Input	**Clock:** CK and CKB are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CKB. Output data strobe (DQS, DQSB) is referenced to the crossings of CK and CKB.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CKB, CKE, RESETB, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESETB) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CSB	Input	**Chip select:** CSB enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CSB is registered HIGH. CSB provides for external rank selection on systems with multiple ranks. CSB is considered part of the command code. CSB is referenced to V_{REFCA}.
DML	Input	**Input data mask:** DML is a lower-byte, input mask signal for write data. Lower-byte input data is masked when DML is sampled HIGH along with the input data during a write access. Although the DML ball is input-only, the DML loading is designed to match that of the DQ and DQS balls. DML is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) Termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQL/DQU[7:0], DQSL, DQSLB, DQSU, DQSUB, DML, and DMU for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RASB, CASB, WEB	Input	**Command inputs:** RASB, CASB, and WEB (along with CSB) define the command being entered and are referenced to V_{REFCA}.
RESETB	Input	**Reset:** RESETB is an active LOW CMOS input referenced to VSS. The RESETB input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESETB assertion and desertion are asynchronous.

96-Ball FBGA -x16 Ball Descriptions (Continued)

Symbol	Type	Description
DMU	Input	**Input data mask:** DMU is an upper-byte, input mask signal for write data. Upperbyte input data is masked when DMU is sampled HIGH along with that input data during a WRITE access. Although the DMU ball is input-only, the DMU loading is designed to match that of the DQ and DQS balls. DMU is referenced to V_{REFDQ}.
DQL[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x16 configuration. DQL[7:0] are referenced to V_{REFDQ}.
DQU[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x16 configuration. DQU[7:0] are referenced to V_{REFDQ}.
DQSL, DQSLB	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
DQSU, DQSUB	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is Center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained atalltimes(including selfrefresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stressrating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature – Industrial	–40	95	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. MAX operating case temperature. T_C is measured in the center of the package.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Input/Output Capacitance

DDR3L Input/Output Capacitance

applies to the entire table

Capacitance Parameters	Sym	DDR3L -1600		DDR3L -1866/2133		Unit	Notes
		Min	Max	Min	Max		
CK and CKB	C_{CK}	0.8	1.4	0.8	1.3	pF	
ΔC: CK to CKB	C_{DCK}	0.0	0.15	0.0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.4	2.2	1.4	2.1	pF	2
Differential I/O: DQS, DQSB	C_{IO}	1.4	2.2	1.4	2.1	pF	3
ΔC: DQS to DQSB	C_{DDQS}	0.0	0.15	0.0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.4	0.2	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.4	0.4	–0.4	0.4	pF	7
ZQ pin capacitance	C_{ZQ}	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	pF	

Notes: 1. V_{DD} = 1.35V (1.283–1.45V), $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).

2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes .C_{DDQS} is for DQS vs. DQS# separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
5. Excludes CK, CKB; CTRL = ODT, CSB, and CKE; CMD = RASB, CASB, and WEB; ADDR = A[*n*:0], BA[2:0].
6. $C_{DI\_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CKB)})$.
7. $C_{DI\_CMD\_ADDR} = C_{I(CMD\_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CKB)})$.

Thermal Characteristics

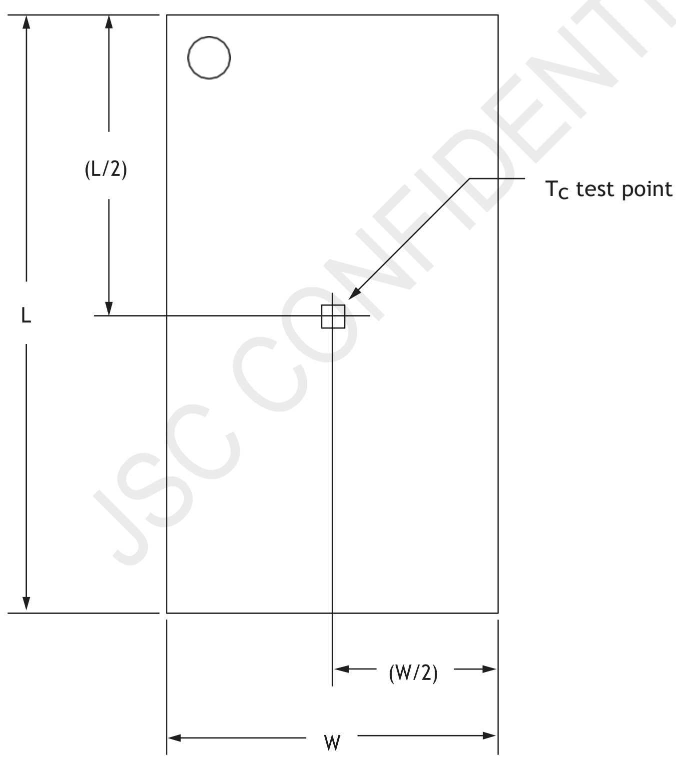
Thermal Characteristics

apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	-40 to 95	°C	4

Notes: 1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), must be enabled.

Thermal Measurement Point



Electrical Specifications – I_{DD} Specifications and Conditions

Within the following I_{DD} measurement tables, the following definitions and conditions are used, unless stated otherwise:

- LOW: $V_{IN} \le V_{IL(AC)max}$; HIGH: $V_{IN} \ge V_{IH(AC)min}$.
- Midlevel: Inputs are $V_{REF} = V_{DD}/2$.
- R_{ON} set to RZQ/7 (34Ω).
- $R_{TT,nom}$ set to RZQ/6 (40Ω).
- $R_{TT(WR)}$ set to RZQ/2 (120Ω).
- Q_{OFF} is enabled in MR1.
- ODT is enabled in MR1($R_{TT,nom}$) and MR2($R_{TT(WR)}$).
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$.
- Burst lengths are BL8 fixed.
- AL equals 0 (except in I_{DD7}).
- I_{DD} specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- Optional ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Timing Parameters Used for I_{DD} Measurements – Clock Units

I_{DD} Parameter		DDR3L -1600		DDR3L -1866	DDR3L - 2133	Unit
		10-10-10	11-11-11	13-13-13	14-14-14	
^tCK (MIN) I_{DD}		1.25		1.07	0.938	ns
CL I_{DD}		10	11	13	14	CK
^tRCD (MIN) I_{DD}		10	11	13	14	CK
^tRC (MIN) I_{DD}		38	39	45	50	CK
^tRAS (MIN) I_{DD}		28	28	32	36	CK
^tRP (MIN)		10	11	13	14	CK
^tFAW	X8	24	24	26	27	CK
^tFAW	X16	32	32	33	38	CK
^tRRD I_{DD}	X8	5	5	5	6	CK
^tRRD I_{DD}	X16	6	6	6	7	CK
^tRFC	1Gb	88	88	103	118	CK
	2Gb	128	128	150	172	CK
	4Gb	208	208	243	279	CK
	8Gb	280	280	328	375	CK

I_{DD0} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC - 1 + *n*RAS -1; truncate if needed												
			*n*RC + *n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until 2 × RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Notes: 1. DQ, DQS, DQSB are midlevel.
2. DM is LOW.
3. Only selected bank (single)active.

I_{DD1} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RCD - 1; truncate if needed												
			*n*RCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RCD - 1; truncate if needed												
			*n*RC + *n*RCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RAS - 1; truncate if needed												
			*n*RC + *n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycle *n*RC + 1 through *n*RC + 4 until 2 × *n*RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Notes: 1. DQ, DQS, DQSB are midlevel unless driven as required by the RD command.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RDcommand.
4. Only selected bank (single) active.

I_{DD} Measurement Conditions for Power-Down Currents

Name	I_{DD2P0} Precharge Power-Down Current (Slow Exit)[1]	I_{DD2P1} Precharge Power-Down Current (Fast Exit)[1]	I_{DD2Q} Precharge Quiet Standby Current	I_{DD3P} Active Power-Down Current
Timing pattern	N/A	N/A	N/A	N/A
CKE	LOW	LOW	HIGH	LOW
External clock	Toggling	Toggling	Toggling	Toggling
^tCK	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}
^tRC	N/A	N/A	N/A	N/A
^tRAS	N/A	N/A	N/A	N/A
^tRCD	N/A	N/A	N/A	N/A
^tRRD	N/A	N/A	N/A	N/A
^tRC	N/A	N/A	N/A	N/A
CL	N/A	N/A	N/A	N/A
AL	N/A	N/A	N/A	N/A
CSB	HIGH	HIGH	HIGH	HIGH
Command inputs	LOW	LOW	LOW	LOW
Row/column addr	LOW	LOW	LOW	LOW
Bank addresses	LOW	LOW	LOW	LOW
DM	LOW	LOW	LOW	LOW
Data I/O	Midlevel	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Enabled	Enabled
ODT[2]	Enabled, off	Enabled, off	Enabled, off	Enabled, off
Burst length	8	8	8	8
Active banks	None	None	None	All
Idle banks	All	All	All	None
Special notes	N/A	N/A	N/A	N/A

Notes: 1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
2. “Enabled, off” means the MR bits are enabled, but the signal is LOW.

I_{DD2N} and I_{DD3N} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7												

Notes: 1. DQ, DQS, DQSB are midlevel.
2. DM is LOW.
3. All banks closed during I_{DD2N}; all banks open during I_{DD3N}.

I_{DD2NT} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1; ODT = 0												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2; ODT = 1												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3; ODT = 1												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4; ODT = 0												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5; ODT = 0												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6; ODT = 1												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7; ODT = 1												

Notes: 1. DQ, DQS, DQSB are midlevel.
2. DM is LOW.
3. All banks closed.

I_{DD4R} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	–
			6	D#	1	1	1	1	0	0	0	0	0	F	0	–
			7	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes: 1. DQ, DQS, DQSB are midlevel when not driving in burst sequence.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RDcommand.
4. All banks open.

I_{DD4W} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	–
			2	D#	1	1	1	1	1	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	0	0	0	0	–
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	–
			6	D#	1	1	1	1	1	0	0	0	0	F	0	–
			7	D#	1	1	1	1	1	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes: 1. DQ, DQS, DQSB are midlevel when not driving in burst sequence.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by theWR command.
4. All banks open.

I_{DD5B} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	–
		1a	1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			4	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1b	5–8	Repeat sub-loop 1a, use BA[2:0] = 1												
		1c	9–12	Repeat sub-loop 1a, use BA[2:0] = 2												
		1d	13–16	Repeat sub-loop 1a, use BA[2:0] = 3												
		1e	17–20	Repeat sub-loop 1a, use BA[2:0] = 4												
		1f	21–24	Repeat sub-loop 1a, use BA[2:0] = 5												
		1g	25–28	Repeat sub-loop 1a, use BA[2:0] = 6												
		1h	29–32	Repeat sub-loop 1a, use BA[2:0] = 7												
		2	33–*n*RFC - 1	Repeat sub-loop 1a through 1h until *n*RFC - 1; truncate if needed												

Notes: 1. DQ, DQS, DQSB are mid level.
2. DM is LOW.

I_{DD} Measurement Conditions for I_{DD6} and I_{DD8}

I_{DD} Test	I_{DD6}: Self Refresh Current Normal Temperature Range T_C = -40°C to +95°C	I_{DD8}: Reset[2]
CKE	LOW	Midlevel
External clock	Off, CK and CKB = LOW	Midlevel
^tCK	N/A	N/A
^tRC	N/A	N/A
^tRAS	N/A	N/A
^tRCD	N/A	N/A
^tRRD	N/A	N/A
^tRC	N/A	N/A
CL	N/A	N/A
AL	N/A	N/A
CSB	Midlevel	Midlevel
Command inputs	Midlevel	Midlevel
Row/column addresses	Midlevel	Midlevel
Bank addresses	Midlevel	Midlevel
Data I/O	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Midlevel
ODT[1]	Enabled, midlevel	Midlevel
Burst length	N/A	N/A
Active banks	N/A	None
Idle banks	N/A	All
SRT	Disabled (normal)	N/A
ASR	Disabled	N/A

Notes: 1. “Enabled, midlevel” means the MR command is enabled, but the signal is midlevel.
2. During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + ^tRFC.

I_{DD7} Measurement Loop

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	Repeat cycle 2 until *n*RRD - 1												
		1	*n*RRD	ACT	0	0	1	1	0	1	0	0	0	F	0	–
			*n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			*n*RRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	–
			*n*RRD + 3	Repeat cycle *n*RRD + 2 until 2 × *n*RRD - 1												
		2	2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 2												
		3	3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 3												
		4	4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	F	0	–
			4 × *n*RRD + 1	Repeat cycle 4 × *n*RRD until *n*FAW - 1, if needed												
		5	*n*FAW	Repeat sub-loop 0, use BA[2:0] = 4												
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BA[2:0] = 5												
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 6												
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 7												
		9	*n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	F	0	–
			*n*FAW + 4 × *n*RRD + 1	Repeat cycle *n*FAW + 4 × *n*RRD until 2 × *n*FAW - 1, if needed												
		10	2 × *n*FAW	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			2 × *n*FAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 × *n*FAW + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			2 × *n*FAW + 3	Repeat cycle 2 × *n*FAW + 2 until 2 × *n*FAW + *n*RRD - 1												
		11	2 × *n*FAW + *n*RRD	ACT	0	0	1	1	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 × *n*FAW + *n*RRD + 2	D	1	0	0	0	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 3	Repeat cycle 2 × *n*FAW + *n*RRD + 2 until 2 × *n*FAW + 2 × *n*RRD - 1												
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 2												
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 3												
		14	2 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	0	0	–
			2 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 2 × *n*FAW + 4 × *n*RRD until 3 × *n*FAW - 1, if needed												
		15	3 × *n*FAW	Repeat sub-loop 10, use BA[2:0] = 4												

I_{DD7} Measurement Loop (Continued)

CK, CKB	CKE	Sub-Loop	Cycle Number	Command	CSB	RASB	CASB	WEB	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	16	3 × *n*FAW + *n*RRD	Repeat sub-loop 11, use BA[2:0] = 5												
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 6												
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 7												
		19	3 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	0	0	–
			3 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 3 × *n*FAW + 4 × *n*RRD until 4 × *n*FAW - 1, if needed												

Notes: 1. DQ, DQS, DQSB are midlevel unless driven as required by the RD command.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RDcommand.
4. AL = CL-1.

Electrical Characteristics – Operating I_{DD} Specifications

I_{DD} Maximum Limits Die for 1.35/1.5V Operation

Speed Bin			DDR3/3L -1600	DDR3/3L -1866	DDR3/3L -2133	Units	Notes
Parameter	Symbol	Width					
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	X8	47	49	51	mA	1, 2
		X16	57	59	61	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	X8	61	64	67	mA	1, 2
		X16	81	84	87	mA	1, 2
Precharge power-down current: Slow exit	I_{DD2P0}	All	8	8	8	mA	1, 2
Precharge power-down current: Fast exit	I_{DD2P1}	All	14	16	18	mA	1, 2
Precharge quiet standby current	I_{DD2Q}	All	24	26	28	mA	1, 2
Precharge standby current	I_{DD2N}	All	24	26	28	mA	1, 2
Precharge standby ODT current	I_{DD2NT}	X8	28	30	32	mA	1, 2
		X16	31	33	35	mA	1, 2
Active power-down current	I_{DD3P}	All	26	28	30	mA	1, 2
Active standby current	I_{DD3N}	X8	30	32	34	mA	1, 2
		X16	38	40	42	mA	1, 2
Burst read operating current	I_{DD4R}	X8	95	105	115	mA	1, 2
		X16	155	165	175	mA	1, 2
Burst write operating current	I_{DD4W}	X8	95	105	115	mA	1, 2
		X16	155	165	175	mA	1, 2
Burst refresh current	I_{DD5B}	All	235	242	245	mA	1, 2
Room temperature self refresh	I_{DD6}	All	12	12	12	mA	1, 2, 3
Extended temperature self refresh	I_{DD6ET}	All	16	16	16	mA	2, 4
All banks interleaved read current	I_{DD7}	X8	130	140	150	mA	1, 2
		X16	190	200	210	mA	1, 2
Reset current	I_{DD8}	All	I_{DD2P} + 2mA	I_{DD2P} + 2mA	I_{DD2P} + 2mA	mA	1, 2

Notes:
1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ +85°C:

   5a. When T_C < 0°C: I_{DD2P0}, I_{DD2P1} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6}, I_{DD6ET} and I_{DD7} must be derated by 7%.

   5b. When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5B} must be derated by 2%; I_{DD2Px} must be derated by 30%.

Electrical Specifications - DC and AC

DC Operating Conditions

DDR3L 1.35V DC Electrical Characteristics and Operating Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1–7
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1–7
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–2	–	2	µA	
V_{REF} supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	I_{VREF}	–1	–	1	µA	8, 9

Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be ≤ V_{DD}. $V_{SS} = V_{SSQ}$.
2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 second).
4. Under these supply voltages, the device operates to this DDR3L specification.
5. If the maximum limit is exceeded, input levels shall be governed by DDR3specifications.
6. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
7. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see VDD Voltage Switching .
8. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
9. V_{REF}.

Input Operating Conditions

DDR3L 1.35V DC Electrical Characteristics and Input Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}	N/A		V	
V_{IN} high; DC/commands/address busses	V_{IH}		N/A	V_{DD}	V	
Input reference voltage command/address bus	$V_{REFCA(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	1, 2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(SR)}$	V_{SS}	$0.5 \times V_{DD}$	V_{DD}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	$0.5 \times V_{DDQ}$	–	V	5

Notes: 1. $V_{REFCA(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFCA} may not exceed $\pm1\% \times V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed $\pm2\%$ of $V_{REFCA(DC)}$.

2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.

3. $V_{REFDQ(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFDQ} maynot exceed $\pm1\% \times V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed $\pm2\%$ of $V_{REFDQ(DC)}$.

4. $V_{REFDQ(DC)}$ may transition to $V_{REFDQ(SR)}$ and back to $V_{REFDQ(DC)}$ when in SELF REFRESH, within restrictions outlined in the SELF REFRESHsection.

5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. Minimum and maximum values are system-dependent.

DDR3L 1.35V Input Switching Conditions – Command and Address

Parameter/Condition	Symbol	DDR3L-1600	DDR3L-1866/2133	Units
Command and Address				
Input high AC voltage: Logic 1	$V_{IH(AC160),min}$ [5]	160	–	mV
	$V_{IH(AC135),min}$ [5]	135	135	mV
	$V_{IH(AC125),min}$ [5]	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90),min}$	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90),min}$	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125),min}$ [5]	–	–125	mV
	$V_{IL(AC135),min}$ [5]	–135	–135	mV
	$V_{IL(AC160),min}$ [5]	–160	–	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC160),min}$ [5]	160	–	mV
	$V_{IH(AC135),min}$ [5]	135	135	mV
	$V_{IH(AC125),min}$ [5]	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90),min}$	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90),min}$	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125),min}$ [5]	–	–130	mV
	$V_{IL(AC135),min}$ [5]	–135	–135	mV
	$V_{IL(AC160),min}$ [5]	–160	–	mV

Notes: 1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.

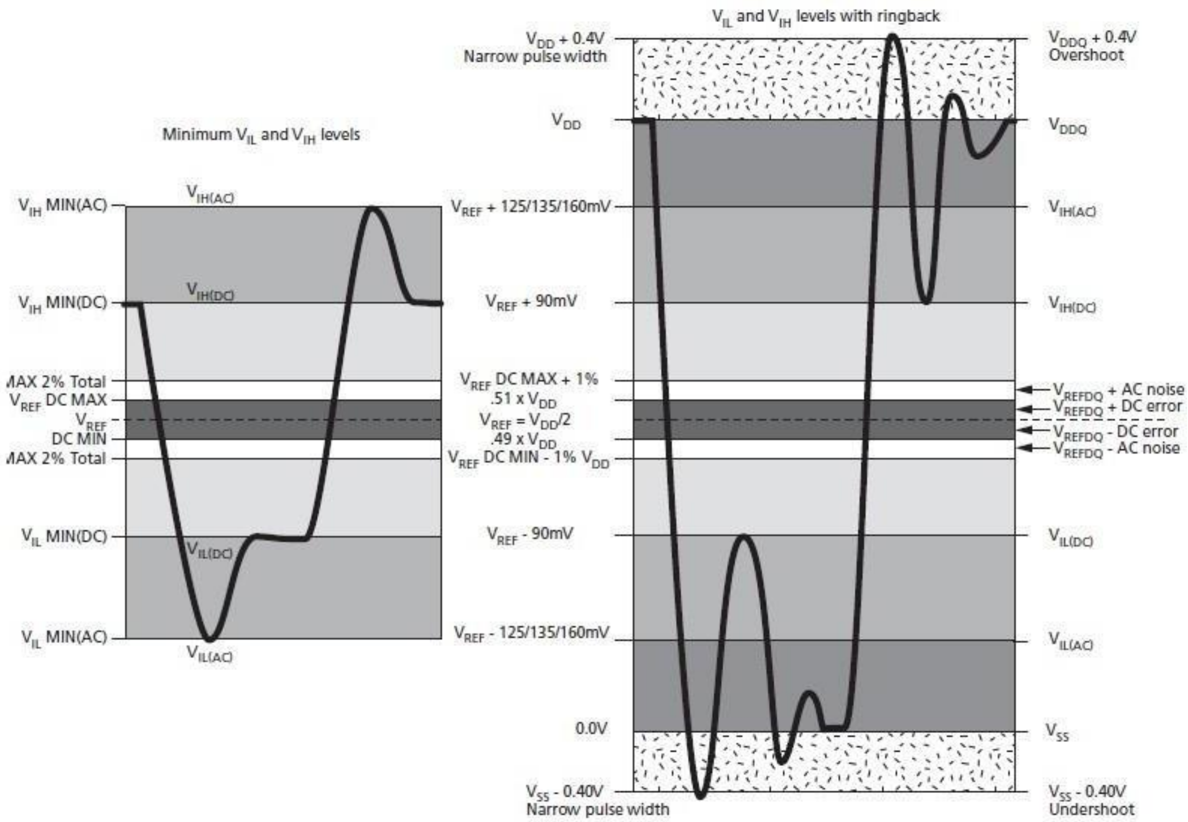
2. Input setup timing parameters (^tIS and ^tDS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (^tIH and ^tDH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
5. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

DDR3L 1.35V Differential Input Operating Conditions (CK, CKB and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV	4
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	–180	mV	4
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DD}/V_{DDQ}	mV	5
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	$2 \times (V_{IL(AC)} - V_{REF})$	mV	6
Differential input crossing voltage relative to $V_{DD}/2$ for DQS, DQS#; CK, CKB	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	5, 7, 9
Differential input crossing voltage relative to $V_{DD}/2$ for CK, CKB	V_{IX} (175)	$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175	mV	5, 7–9
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2$ + 160	V_{DDQ}	mV	5
Single-ended high level for CK, CKB		$V_{DD}/2$ + 160	V_{DD}	mV	5
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2$ - 160	mV	6
Single-ended low level for CK, CKB		V_{SS}	$V_{DD}/2$ - 160	mV	6

Notes:
1. Clock is referenced to V_{DD} and V_{SS}. Data strobe is referenced to V_{DDQ} and V_{SSQ}.
2. Reference is $V_{REFCA(DC)}$ for clock and $V_{REFDQ(DC)}$ forstrobe.
3. Differential input slew rate = 2 V/ns.
4. Defines slew rate reference points, relative to input crossing voltages.
5. Minimum DC limit is relative to single-ended signals; overshoot specifications are appli-cable.
6. Maximum DC limit is relative to single-ended signals; undershoot specifications areap-plicable.
7. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
8. The V_{IX} extended range (±175mV) is allowed only for the clock; this V_{IX} extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing V_{SEL}, V_{SEH} of at least $V_{DD}/2$ ±250mV, and the differential slew rate of CK, CKB is greater than 3 V/ns.
9. V_{IX} must provide 25mV (single-ended) of the voltages separation.

DDR3L 1.35V Input Signal



Note: 1. Numbers in diagrams reflect nominal values.

DDR3L 1.35V AC Overshoot/Undershoot Specification

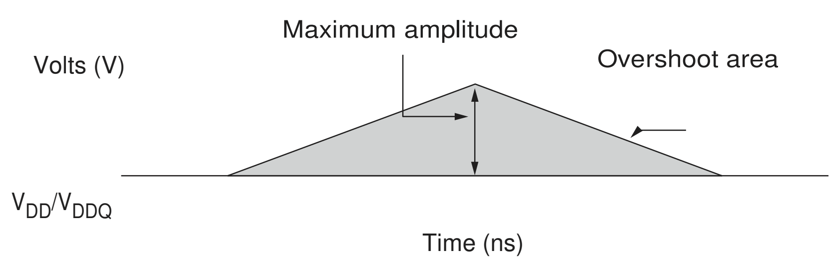
DDR3L Control and Address Pins

Parameter	DDR3L-1600	DDR3L-1866	DDR3L-2133
Maximum peak ampli- tude allowed for over- shoot area	0.4V	0.4V	0.4V
Maximum peak ampli- tude allowed for under- shoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}	0.33 V/ns	0.28 V/ns	0.25 V/ns
Maximum undershoot area below V_{SS}	0.33 V/ns	0.28 V/ns	0.25 V/ns

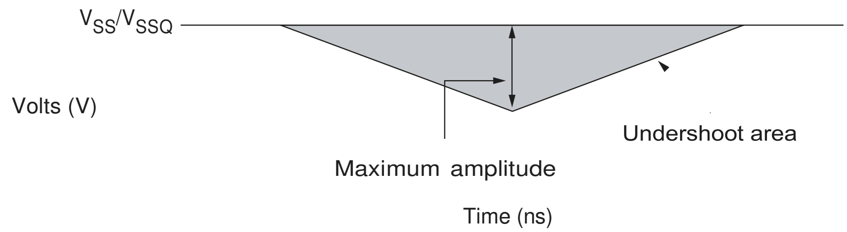
DDR3L 1.35V Clock, Data, Strobe, and Mask Pins

Parameter	DDR3L-1600	DDR3L-1866	DDR3L-2133
Maximum peak ampli- tude allowed for over- shoot area	0.4V	0.4V	0.4V
Maximum peak ampli- tude allowed for under- shoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ}	0.13 V/ns	0.11 V/ns	0.10 V/ns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.13 V/ns	0.11 V/ns	0.10 V/ns

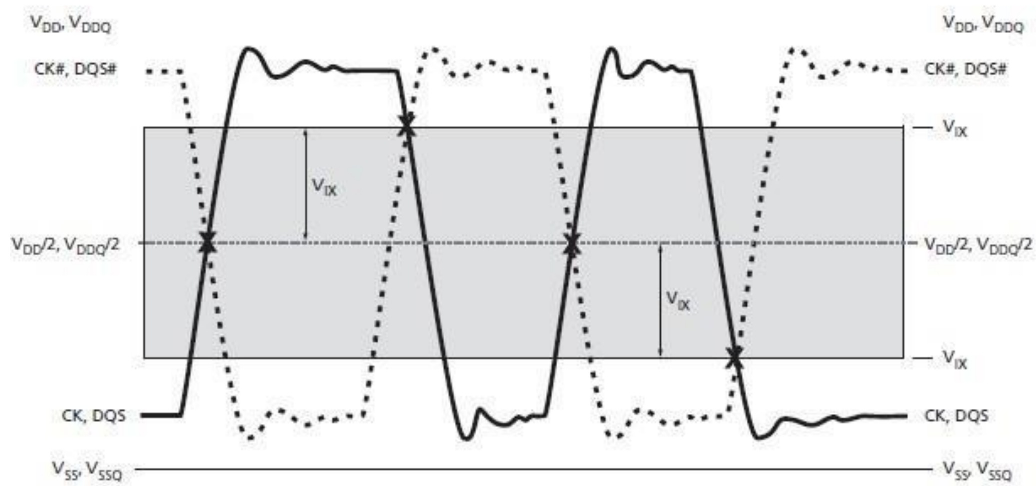
Overshoot



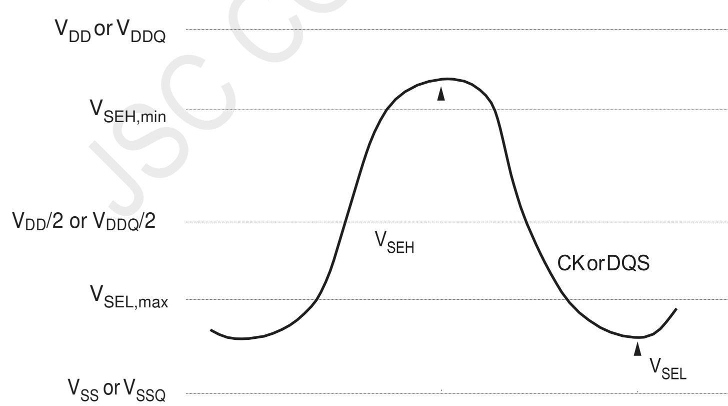
Undershoot



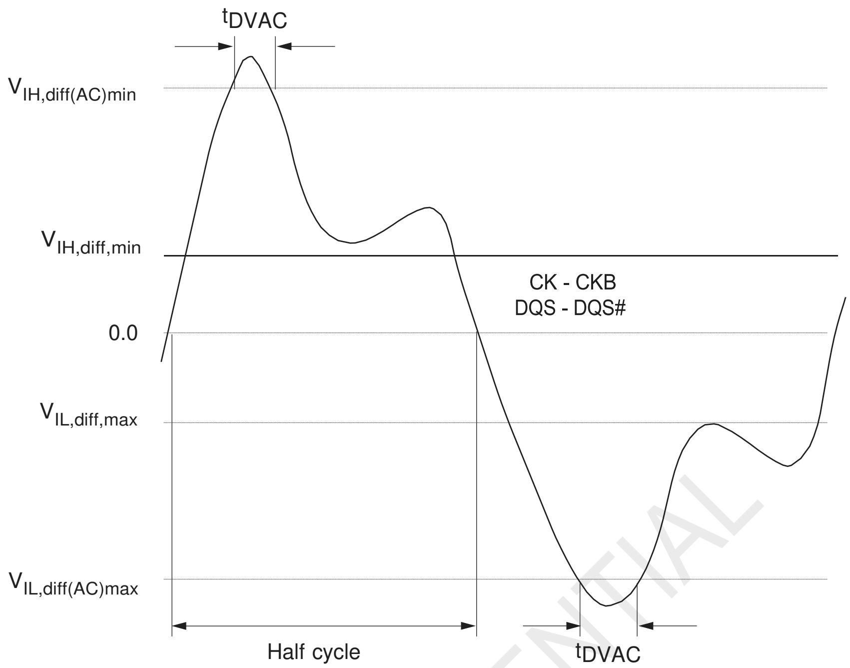
V_{IX} for Differential Signals



Single-Ended Requirements for Differential Signals



Definition of Differential AC-Swing and ᵗDVAC



DDR3L 1.35V – Minimum Required Time ᵗDVAC for CK/CKB, DQS/DQS# Differential for AC Ringback

Slew Rate (V/ns)	DDR3L-1600		DDR3L-1866/2133		
	ᵗDVAC at 320mV (ps)	ᵗDVAC at 270mV (ps)	ᵗDVAC at 270mV (ps)	ᵗDVAC at 250mV (ps)	ᵗDVAC at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note 1	44	5	22	24
1.0	Note 1				
<1.0	Note 1				

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

DDR3L 1.35V Slew Rate Definitions for Single-Ended Input Signals

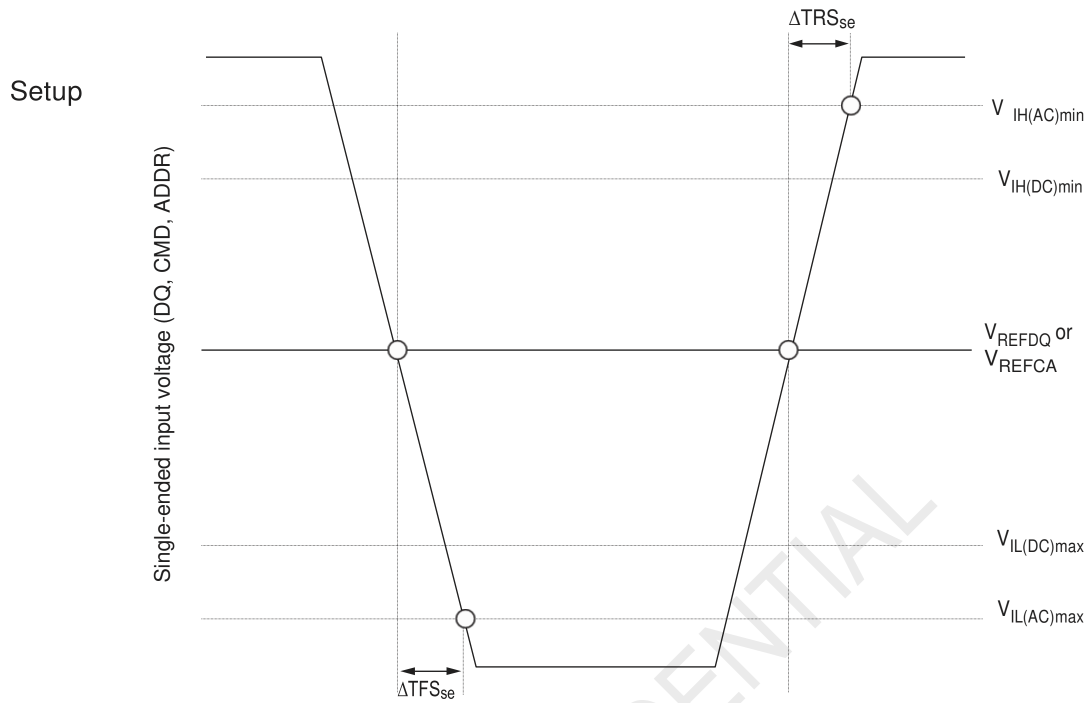
Setup(^{t}IS and^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC)min}$.
Setup(^{t}ISand^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC)max}$.

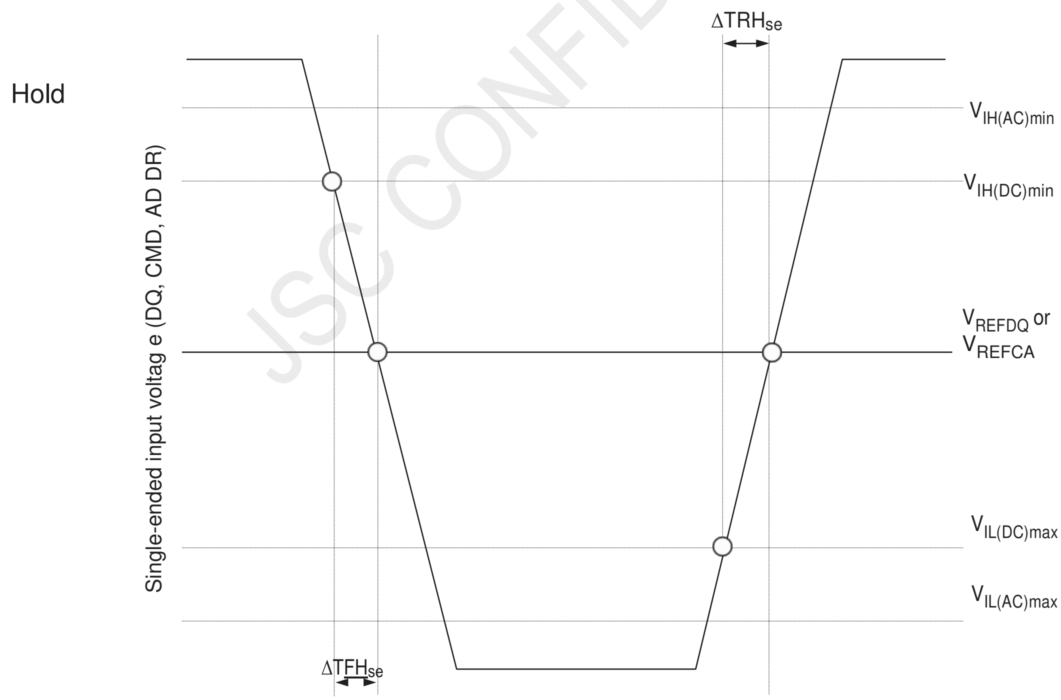
Hold(^{t}IHand^{t}DH) nominal slew rate for arising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of V_{REF}. Hold(^{t}IH and^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of V_{REF}.

Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
Setup	Rising	V_{REF}	$V_{IH(AC),min}$	$\frac{V_{IH(AC),min} - V_{REF}}{\Delta TRS_{se}}$
	Falling	V_{REF}	$V_{IL(AC),max}$	$\frac{V_{REF} - V_{IL(AC),max}}{\Delta TFS_{se}}$
Hold	Rising	$V_{IL(DC),max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC),max}}{\Delta TFH_{se}}$
	Falling	$V_{IH(DC),min}$	V_{REF}	$\frac{V_{IH(DC),min} - V_{REF}}{\Delta TRSH_{se}}$

Nominal Slew Rate Definition for Single-Ended Input Signals





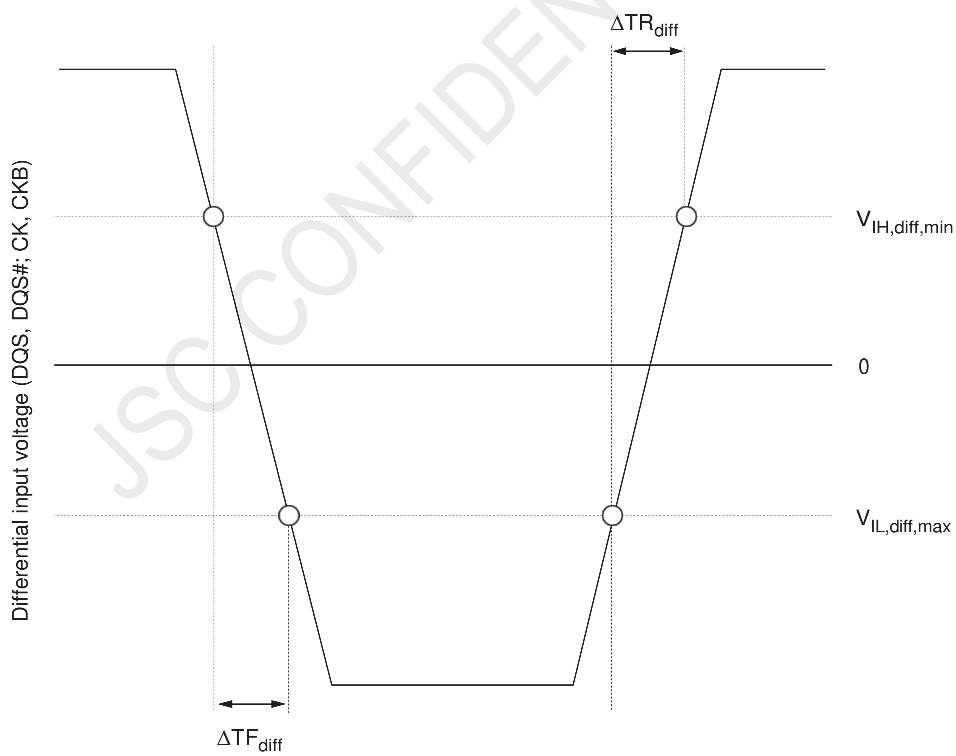
DDR3L 1.35V Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CKB and DQS, DQS#) are defined and measured. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL,diff,max}$ and $V_{IH,diff,min}$. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH,diff,min}$ and $V_{IL,diff,max}$.

DDR3L 1.35V Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
CK and DQS reference	Rising	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TR_{diff}}$
	Falling	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TF_{diff}}$

DDR3L 1.35V Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CKB

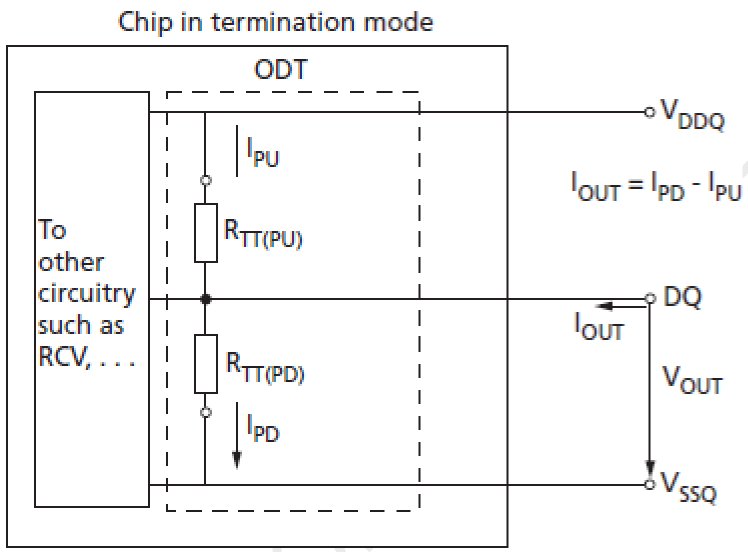


ODT Characteristics

The ODT effective resistance R_{TT} is definedby MR1[9,6, and2]. ODT is applied to the DQ, DM, DQS, DQS#, balls (x8 devices only). The ODT target values and a functional representation are listed. The individual pull-up and pull-down resistors ($R_{TT(PU)}$ and $R_{TT(PD)}$) are defined as follows:

- $R_{TT(PU)} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT(PD)}$ is turned off
- $R_{TT(PD)} = (V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT(PU)}$ is turned off

ODT Levels and I-V Characteristics



On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedance	$R_{TT(EFF)}$					1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	–5		5	%	1, 2, 3

Notes: 1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$). Refer to ODT Sensitivity if either the temperature or voltage changes after calibration.

2. Measurement definition for R_{TT}: Apply $V_{IH(AC)}$ to pin under test and measure current $I[V_{IH(AC)}]$, then apply $V_{IL(AC)}$ to pin under test and measure current $I[V_{IL(AC)}]$:

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100$$

4. For IT and AT devices, the minimum values are derated by 6% when the device operates between –40°C and 0°C(T_C).

1.35 V ODT Resistors

provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements ; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} 120Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$
- R_{TT} 60Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$
- R_{TT} 40Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$
- R_{TT} 30Ω is made up of $R_{TT30(PD60)}$ and $R_{TT30(PU60)}$
- R_{TT} 20Ω is made up of $R_{TT20(PD40)}$ and $R_{TT20(PU40)}$

1.35V R_{TT} Effective Impedance

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	$R_{TT,120PD240}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/1
		$R_{TT,120PU240}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	$R_{TT,60PD120}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/2
		$R_{TT,60PU120}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	$R_{TT,40PD80}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/3
		$R_{TT,40PU80}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	$R_{TT,30PD60}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/4
		$R_{TT,30PU60}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/8

1.35 V R_{TT} Effective Impedance(Continued)

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
1, 0, 0	20Ω	$R_{TT,20PD40}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
		$R_{TT,20PU40}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/12

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, then the tolerance limitslisted can be expected to widen according to list.

ODT Sensitivity Definition

Symbol	Min	Max	Unit
R_{TT}	0.9 - $dR_{TT}dT$ × |DT| - $dR_{TT}dV$ × |DV|	1.6 + $dR_{TT}dT$ × |DT| + $dR_{TT}dV$ × |DV|	RZQ/(2, 4, 6, 8, 12)

Note: 1. ΔT = T - T(@ calibration), ΔV = V_{DDQ} - V_{DDQ}(@ calibration) and V_{DD} = V_{DDQ}.

ODT Temperature and Voltage Sensitivity

Change	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

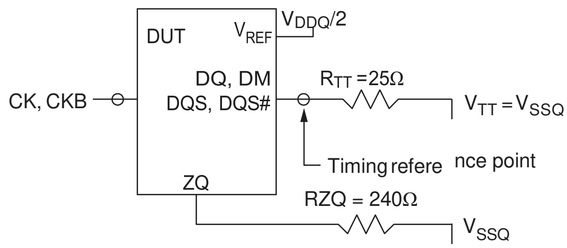
Note: 1. ΔT = T - T(@ calibration), ΔV = V_{DDQ} - V_{DDQ}(@ calibration) and V_{DD} = V_{DDQ}.

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown.Two parameters define when ODT turnsonoroff synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Outline and provide definition and measurement references settings for each parameter.

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on.ODT turn-offtime begins when the output leaves Low-Zand ODT resistance begins to turn off.

ODT Timing Reference Load



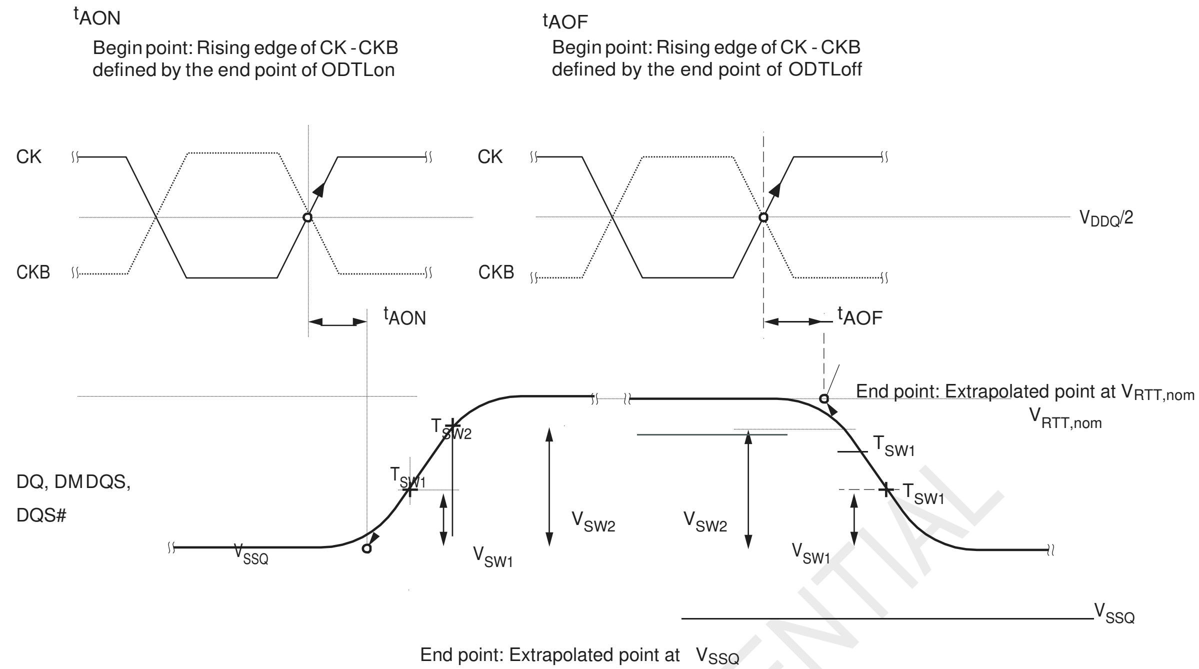
ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition
tAON	Rising edge of CK – CKB defined by the end point of ODTLon	Extrapolated point at V_{SSQ}
tAOF	Rising edge of CK – CKB defined by the end point of ODTLoff	Extrapolated point at $V_{RTT,nom}$
tAONPD	Rising edge of CK – CKB with ODT first being registered HIGH	Extrapolated point at V_{SSQ}
tAOFPD	Rising edge of CK – CKB with ODT first being registered LOW	Extrapolated point at $V_{RTT,nom}$
tADC	Rising edge of CK – CKB defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	Extrapolated points at $V_{RTT(WR)}$ and $V_{RTT,nom}$

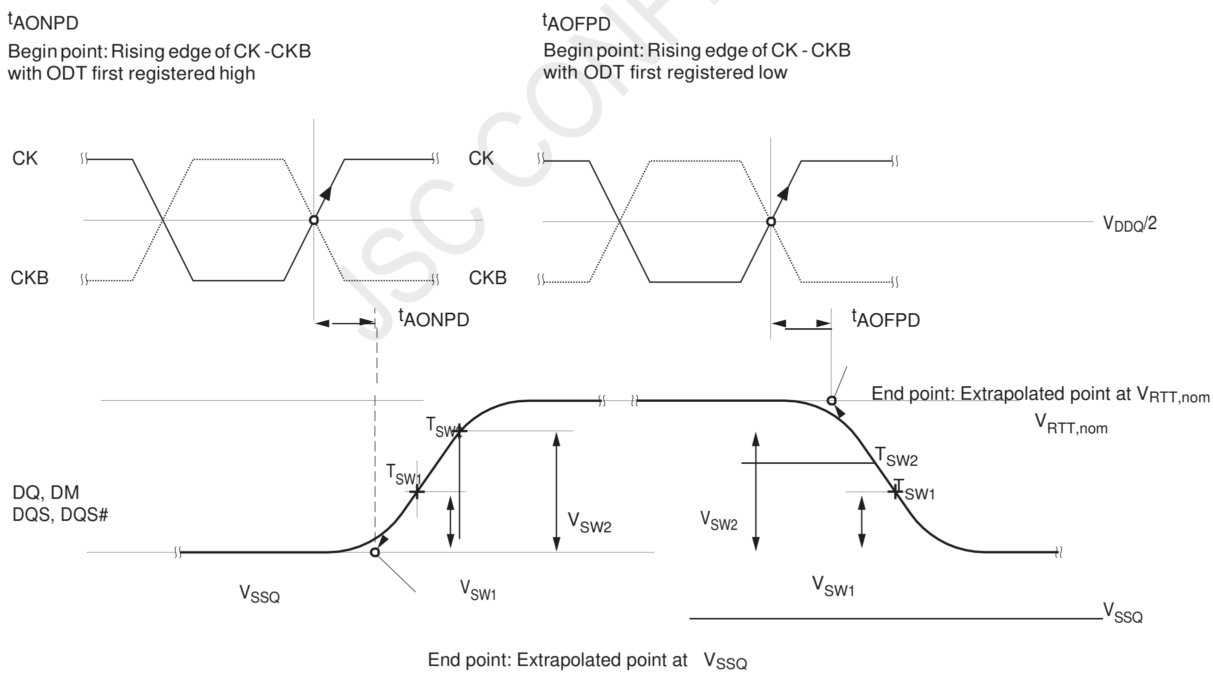
DDR3L(1.35V) Reference Settings for ODT Timing Measurements

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
tAON	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAOF	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAONPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAOFPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tADC	RZQ/12 (20Ω)	RZQ/2 (20Ω)	200mV	250mV

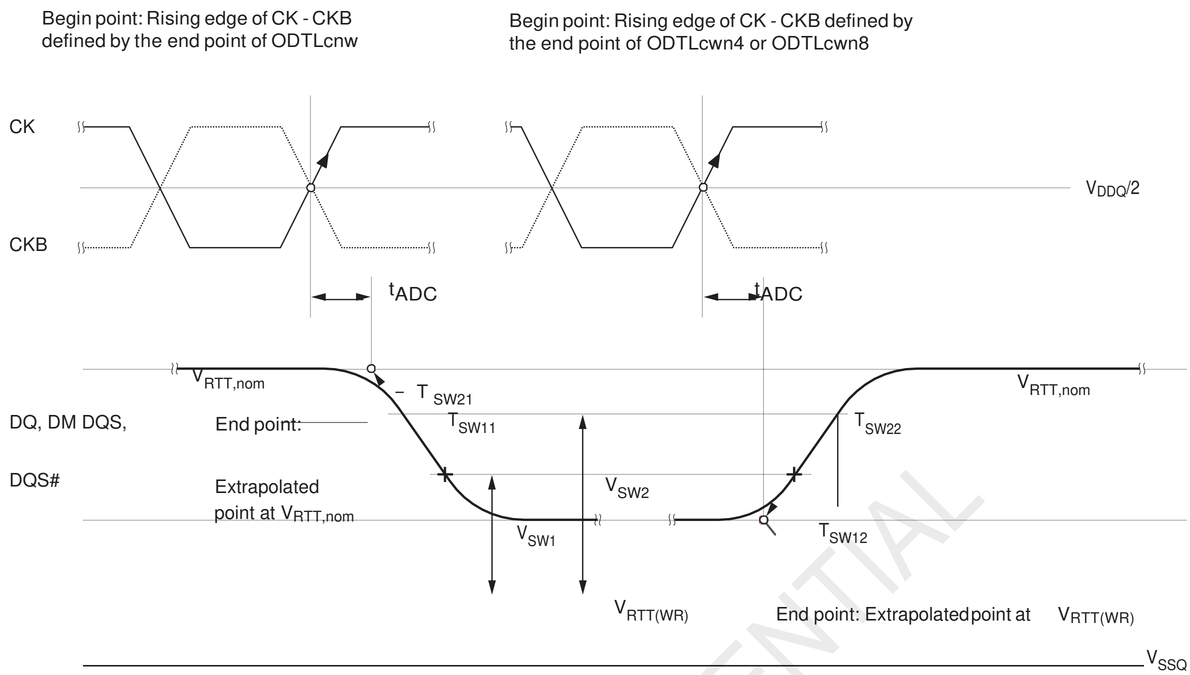
tAON and tAOF Definitions



tAONPD and tAOFPD Definitions



^{t}ADC Definition



Output Driver Impedance

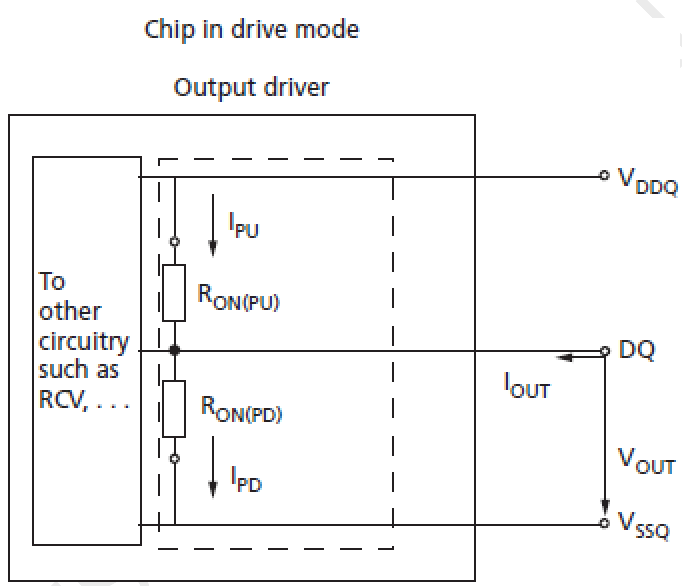
The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight to lerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below. The out put driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

- $R_{ON,x}=RZQ/y$ (with RZQ = 240Ω±1%; x = 34Ω or 40Ω with y = 7 or 6, respectively)

The individual pull-up and pull-downresistors $R_{ON(PU)}$ and $R_{ON(PD)}$ are defined as follows:

- $R_{ON(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, when $R_{ON(PD)}$ is turned off
- $R_{ON(PD)} = (V_{OUT})/|I_{OUT}|$, when $R_{ON(PU)}$ is turned off

Output Driver



34 Ohm Output Driver Impedance

The 34Ω driver(MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed here in apply to the 34Ω driveronly. Its impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows: R_{ON34} = RZQ/7 (with nominal RZQ = 240Ω ±1%) and is actually 34.3Ω ±1%.

DDR3L 34 Ohm Driver Impedance Characteristics

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1	34.3Ω	$R_{ON,34PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
		$R_{ON,34PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Notes: 1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibra- tion has been performed at a stable temperature and voltage: $V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$). Refer to DDR3L 34 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}).Meas- ure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$

3. For IT and AT (1Gb only) devices, the minimum values are derated by 6% when the de- vice operates between –40°C and 0°C (T_C).
A larger maximum limit will result in slightly lower minimum currents.

DDR3L 34 Ohm Driver

The 34Ω driver's current range has been calculated and summarized V_{DD} = 1.35V, V_{DD} =1.45V,V_{DD} = 1.283V.The individual pull-up and pull-down resistors $R_{ON34(PD)}$ and $R_{ON34(PU)}$ are defined as follows:

- $R_{ON34(PD)} = (V_{OUT})/|I_{OUT}|$; $R_{ON34(PU)}$ is turned off
- $R_{ON34(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$; $R_{ON34(PD)}$ is turned off

DDR3L 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}				Min	Nom	Max	Unit
RZQ = 240Ω ±1%				237.6	240	242.4	Ω
RZQ/7 = (240Ω ±1%)/7				33.9	34.3	34.6	Ω
MR1[5,1]	**R_{ON}**	**Resistor**	**V_{OUT}**	**Min**	**Nom**	**Max**	**Unit**
0, 1	34.3Ω	$R_{ON34(PD)}$	0.2 × V_{DDQ}	20.4	34.3	38.1	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	30.5	34.3	48.5	Ω
		$R_{ON34(PU)}$	0.2 × V_{DDQ}	30.5	34.3	48.5	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	20.4	34.3	38.1	Ω

DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: V_{DD} = V_{DDQ} = DDR3L@1.35V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	13.3	7.9	7.1	mA
			I_{OL} @ 0.5 × V_{DDQ}	22.1	19.7	17.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	35.4	31.5	22.3	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	35.4	31.5	22.3	mA
			I_{OH} @ 0.5 × V_{DDQ}	22.1	19.7	17.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	13.3	7.9	7.1	mA

DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: V_{DD} = V_{DDQ} = DDR3L@1.45V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	14.2	8.5	7.6	mA
			I_{OL} @ 0.5 × V_{DDQ}	23.7	21.1	19.0	mA
			I_{OL} @ 0.8 × V_{DDQ}	38.0	33.8	23.9	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	38.0	33.8	23.9	mA
			I_{OH} @ 0.5 × V_{DDQ}	23.7	21.1	19.0	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.2	8.5	7.6	mA

DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.283

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	12.6	7.5	6.7	mA
			I_{OL} @ 0.5 × V_{DDQ}	21.0	18.7	16.8	mA
			I_{OL} @ 0.8 × V_{DDQ}	33.6	29.9	21.2	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	33.6	29.9	21.2	mA
			I_{OH} @ 0.5 × V_{DDQ}	21.0	18.7	16.8	mA
			I_{OH} @ 0.8 × V_{DDQ}	12.6	7.5	6.7	mA

DDR3L 34 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed can be expected to widen according to list.

DDR3L 34 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7

Note: 1. $\Delta T = T - T_{(@CALIBRATION)}$; $\Delta V = V_{DDQ} - V_{DDQ(@CALIBRATION)}$; and $V_{DD} = V_{DDQ}$.

DDR3L 34 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.13	%/mV

DDR3L Alternative 40 Ohm Driver

DDR3L 40 Ohm Driver Impedance Characteristics

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 0	40Ω	$R_{ON,40PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
		$R_{ON,40PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Notes: 1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$). Refer to DDR3L 40 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$

3. For IT and AT (1Gb only) devices, the minimum values are derated by 6% when the device operates between –40°C and 0°C (T_C).
A larger maximum limit will result in slightly lower minimum currents.

DDR3L 40 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after I/O calibration, then the tolerance limits listed can be expected to widen according.

DDR3L 40 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6

Note: 1. $\Delta T = T - T_{(@CALIBRATION)}$, $\Delta V = V_{DDQ} - V_{DDQ(@CALIBRATION)}$; and $V_{DD} = V_{DDQ}$.

40 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	%/mV

Output Characteristics and Operating Conditions

DDR3L Single-Ended Output Driver Characteristics

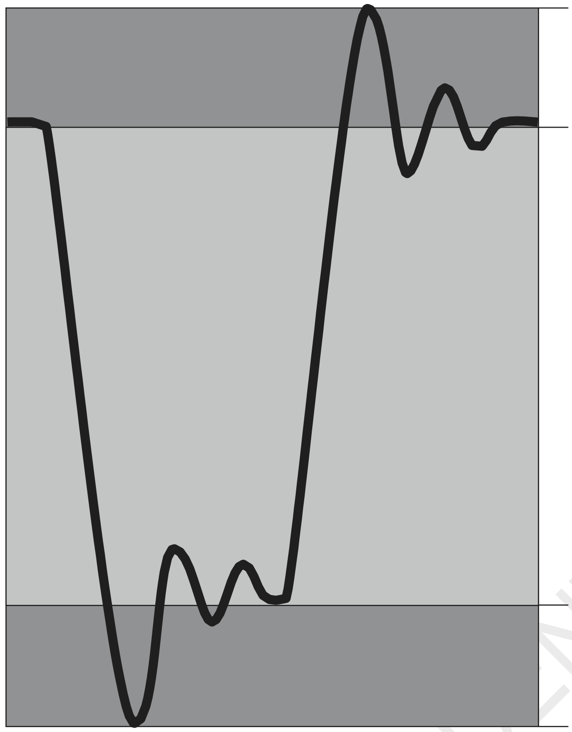
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled ; $0V \le V_{OUT} \le V_{DDQ}$; ODT is disabled ; ODT is HIGH	I_{OZ}	–5	5	μA	1
Output slew rate : Single-ended ; For rising and falling edges , measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns	1, 2, 3, 4
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	$0.5 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 \times V_{DDQ}$		V	1, 2, 5
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 7
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				3

Notes: 1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).

2. $V_{TT} = V_{DDQ}/2$.
3. The test load configuration.
4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
5. LV curve linearity. Do not use AC test load.
6. See Slew Rate Definitions for Single-Ended Output Signals for output slewrate.
7. Additional information.
8. An example of a single-ended output signal.

DQ Output Signal



DDR3L Differential Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	5	µA	1
DDR3L Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$ = –0.18 × V_{DDQ} and $V_{OH,diff(AC)}$ = 0.18 × V_{DDQ}	SRQ_{diff}	3.5	12	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 × V_{DDQ}		V	1, 4
Differential low-level output voltage	$V_{OL,diff(AC)}$	–0.2 × V_{DDQ}		V	1, 4
Delta Ron between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 5
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes:
1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).
2. $V_{REF} = V_{DDQ}/2$; slew rate @ 5 V/ns, interpolate for faster slew rate.
3. The test load configuration.
4. The output slew rate.
5. Additional information.
6. An example of a differential output signal.

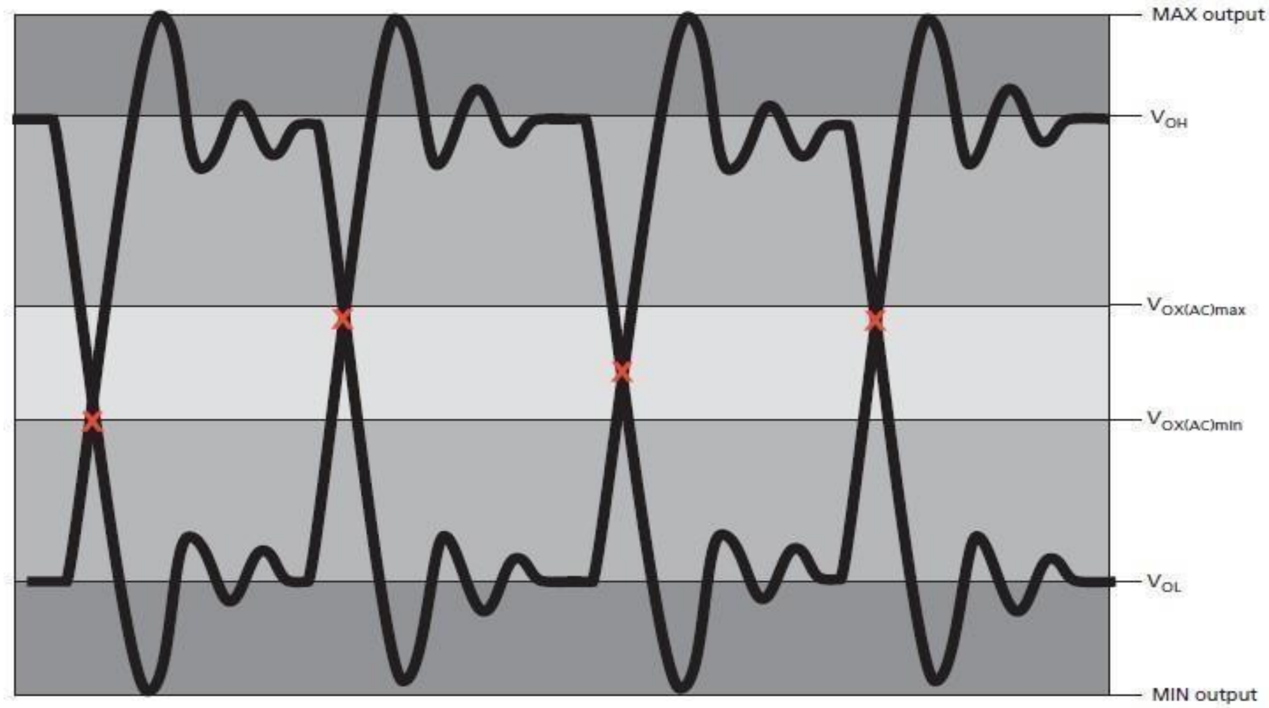
DDR3L Differential Output Driver Characteristics $V_{OX(AC)}$

All voltages are referenced to V_{SS}

Parameter/ Condition	Symbol		DDR3L-1600/1866/2133 DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5v/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Output differential crosspoint voltage	$V_{OX(AC)}$	Max	90	105	135	155	180	205	205	205	205	mV
		Min	–90	–105	–135	–155	–180	–205	–205	–205	–205	mV

Notes:
1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop- er ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).
2. The test load configuration.
3. An example of a differential output signal.
4. For a differential slew rate between the list values, the $V_{OX(AC)}$ value may be obtained by linear interpolation.

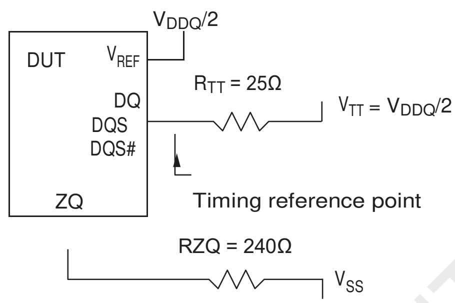
Differential Output Signal



Reference Output Load

Represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODTreference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actualload presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Reference Output Load for AC Timing and Output Slew Rate



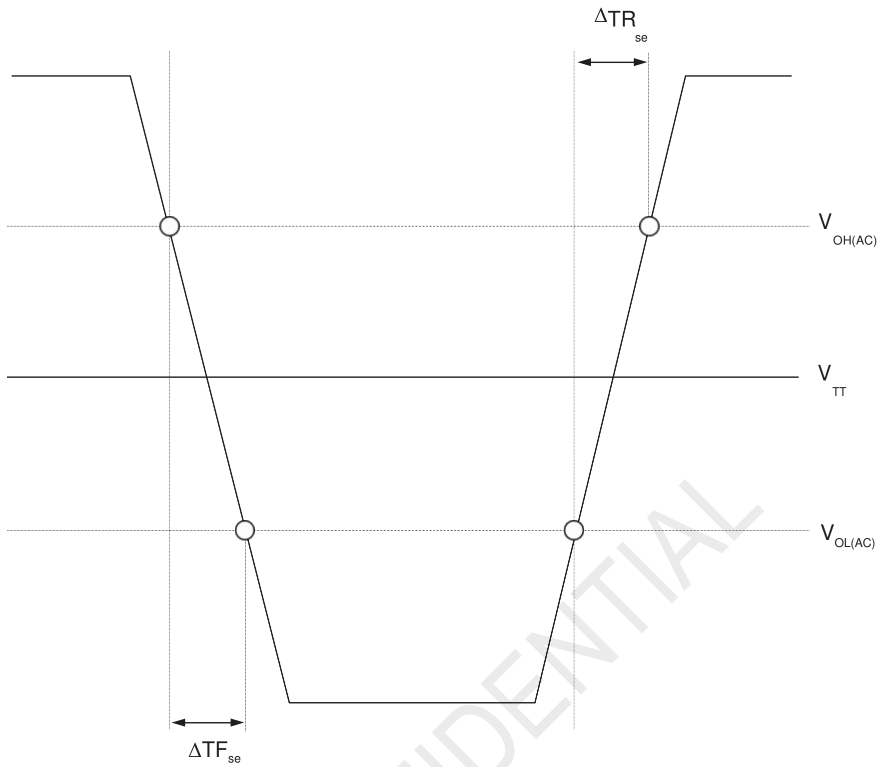
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQ	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR_{se}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TF_{se}}$

Nominal Slew Rate Definition for Single-Ended Output Signals



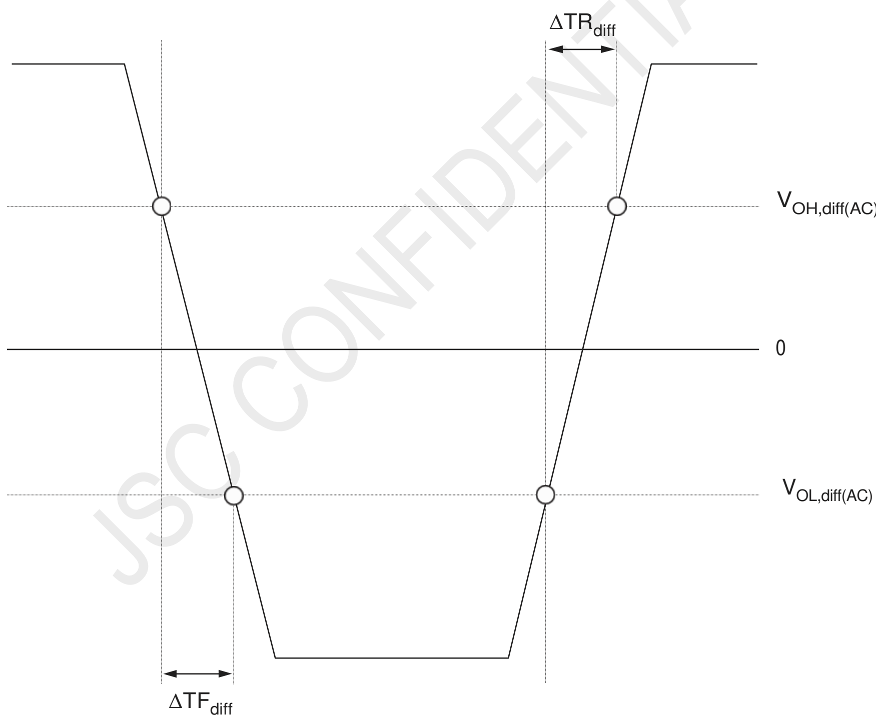
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for differential signals.

Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TR_{diff}}$
	Falling	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TF_{diff}}$

Nominal Differential Output Slew Rate Definition for DQS, DQS#



Speed Bin Tables

DDR3L-1600 Speed Bins

DDR3L-1600 Speed Bin			11-11-11		Unit	Notes
CL-^{t}RCD-^{t}RP						
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.75	–	ns	
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.75	–	ns	
PRECHARGE command period		^{t}RP	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	35	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7, 8	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 10	CWL = 5, 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		CK	

Notes: 1. This speed grade is backward compatible with 1333, CL = 9 and 1066, CL = 7.

DDR3L-1866 Speed Bins

DDR3L-1866 Speed Bin			13-13-13		Unit	Notes
CL-^{t}RCD-^{t}RP						
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.91	20		
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.91	–	ns	
PRECHARGE command period		^{t}RP	13.91	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	47.91	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	34	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	1.07	<1.25	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

Notes: 1. This speed grade is backward compatible with 1600, CL = 11 , 1333, CL= 9 and 1066, CL = 7 .

DDR3L-2133 Speed Bins

DDR3L-2133 Speed Bin			14-14-14		Unit	Notes
CL-^{t}RCD-^{t}RP						
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.09	20		
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.09	–	ns	
PRECHARGE command period		^{t}RP	13.09	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	46.09	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	33	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	1.07	<1.25	ns	3
CL = 14	CWL = 5, 6, 7, 8, 9	^{t}CK (AVG)	Reserved			
	CWL = 10	^{t}CK (AVG)	0.938	<1.07		
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13,14		CK	
Supported CWL settings			5, 6, 7, 8, 9,10		CK	

Notes: 1. The -A speed grade is backward compatible with 1600, CL = 11 , 1333, CL= 9 and 1066, CL = 7 .

Electrical Characteristics and AC Operating Conditions

Electrical Characteristics and AC Operating Conditions
Notes 1-8 apply to the entire table

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
Clock Timing						
Clock period average: DLL disable mode	$T_C \le 85°C$	^{t}CK (DLL_DIS)	8	7800	ns	9, 42
	T_C = >85°C to 95°C		8	3900	ns	42
Clock period average: DLL enable mode		^{t}CK (AVG)			ns	10, 11
High pulse width average		^{t}CH (AVG)	0.47	0.53	CK	12
Low pulse width average		^{t}CL (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	^{t}JITper	–70	70	ps	13
	DLL locking	^{t}JITper,lck	–60	60	ps	13
Clock absolute period		^{t}CK (ABS)	MIN = tCK (AVG) MIN + tJITper MIN; MAX = tCK (AVG) MAX + tJITper		ps	
Clock absolute high pulse width		^{t}CH (ABS)	0.43	–	^{t}CK (AVG)	14
Clock absolute low pulse width		^{t}CL (ABS)	0.43	–	^{t}CK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^{t}JITcc	140		ps	16
	DLL locking	^{t}JITcc,lck	120		ps	16
Cumulative error across	2 cycles	^{t}ERR2per	–103	103	ps	17
	3 cycles	^{t}ERR3per	–122	122	ps	17
	4 cycles	^{t}ERR4per	–136	136	ps	17
	5 cycles	^{t}ERR5per	–147	147	ps	17
	6 cycles	^{t}ERR6per	–155	155	ps	17
	7 cycles	^{t}ERR7per	–163	163	ps	17
	8 cycles	^{t}ERR8per	–169	169	ps	17
	9 cycles	^{t}ERR9per	–175	175	ps	17
	10 cycles	^{t}ERR10per	–180	180	ps	17
	11 cycles	^{t}ERR11per	–184	184	ps	17
	12 cycles	^{t}ERR12per	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	tERRnper MIN = (1 + 0.68ln[n]) × tJITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX		ps	17

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC160)	–	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC135)	25	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	^{t}DH (DC90)	55	–	ps	18, 19
	V_{REF} @ 1 V/ns		145	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	360	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	100	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CKB		^{t}LZDQ	–450	225	ps	22, 23
DQ High-Z time from CK, CKB		^{t}HZDQ	–	225	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CKB rising		^{t}DQSS	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CKB rising		^{t}DSS	0.18	–	CK	25
DQS, DQS# falling hold from CK, CKB rising		^{t}DSH	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3	–	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CKB		^{t}DQSCK	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CKB when DLL is disabled		^{t}DQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		^{t}QSH	0.40	–	CK	21
DQS, DQS# differential output low time		^{t}QSL	0.40	–	CK	21

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
DQS, DQS# Low-Z time (RL - 1)		^{t}LZDQS	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		^{t}HZDQS	–	225	ps	22, 23
DQS, DQS# differential READ preamble		^{t}RPRE	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^{t}RPST	0.3	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		^{t}DLLK	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	^{t}IS (AC160)	60	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	^{t}IS (AC135)	185	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		320	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	^{t}IH (DC90	130	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for tRCD		ns	31
PRECHARGE command period		^{t}RP	See Speed Bin Tables for tRP		ns	31
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for tRAS		ns	31, 32
ACTIVATE-to-ACTIVATE command period		^{t}RC	See Speed Bin Tables for tRC		ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	X8 (1KB page size)	^{t}RRD	MIN = greater of 4CK or 6ns		CK	31
	X16 (2KB page size)		MIN = greater of 4CK or 7.5ns		CK	31
Four ACTIVATE windows	X8 (1KB page size)	^{t}FAW	30	–	ns	31
	X16 (2KB page size)		40		ns	31
Write recovery time		^{t}WR	MIN = 15ns; MAX = N/A		ns	31, 32, 33,34
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
CASB-to-CASB command delay		^{t}CCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	512	–	CK	
	Normal operation	^{t}ZQoper	256	–	CK	
ZQCS command: Short calibration time		^{t}ZQCS	64	–	CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb	MIN = 110; MAX = 70,200		ns	
		^{t}RFC – 2Gb	MIN = 160; MAX = 70,200		ns	
		^{t}RFC – 4Gb	MIN = 260; MAX = 70,200		ns	
		^{t}RFC – 8Gb	MIN = 350; MAX = 70,200		ns	
Maximum refresh period	$T_C \le 85°C$	–	64 (1X)		ms	36
	$T_C > 85°C$		32 (2X)		ms	36
Maximum average periodic refresh	$T_C \le 85°C$	^{t}REFI	7.8 (64ms/8192)		μs	36
	$T_C > 85°C$		3.9 (32ms/8192)		μs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
Exit self refresh to commands requiring a locked DLL		^tXSDLL	MIN = ^tDLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^tCKESR	MIN = ^tCKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		^tCKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^tCKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing						
CKE MIN pulse width		^tCKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay		^tCPDED	MIN = 1; MAX = N/A		CK	
Power-down entry to power-down exit timing		^tPD	MIN = ^tCKE (MIN); MAX = 9 * tREFI		CK	
Begin power-down period prior to CKE registered HIGH		^tANPD	WL - 1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^tANPD or ^tRFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^tANPD + ^tXPDLL		CK	
Power-Down Entry Minimum Timing						
ACTIVATE command to power-down entry		$^tACTPDEN$	MIN = 1		CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^tPRPDEN	MIN = 1		CK	
REFRESH command to power-down entry		$^tREFPDEN$	MIN = 1		CK	37
MRS command to power-down entry		$^tMRSPDEN$	MIN = ^tMOD (MIN)		CK	
READ/READ with auto precharge command to power-down entry		^tRDPDEN	MIN = RL + 4 + 1		CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^tWRPDEN	MIN = WL + 4 + $^tWR/^tCK$ (AVG)		CK	
	BC4MRS	^tWRPDEN	MIN = WL + 2 + $^tWR/^tCK$ (AVG)		CK	

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1600 Min	DDR3L-1600 Max	Unit	Notes
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAP-DEN	MIN = WL + 4 + WR + 1		CK	
	BC4MRS	^{t}WRAP-DEN	MIN = WL + 2 + WR + 1		CK	
Power-Down Exit Timing						
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A		CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A		CK	28
ODT Timing						
R_{TT} synchronous turn-on delay		ODTLon	CWL + AL - 2CK		CK	38
R_{TT} synchronous turn-off delay		ODTLoff	CWL + AL - 2CK		CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5		ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5		ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A		CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing						
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew		ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4		ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8		ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew		^{t}ADC	0.3	0.7	CK	39
Write Leveling Timing						
First DQS, DQS# rising edge		^{t}WLMRD	40	–	CK	
DQS, DQS# delay		^{t}WLDQSEN	25	–	CK	
Write leveling setup from rising CK, CKB crossing to rising DQS, DQS# crossing		^{t}WLS	165	–	ps	

Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3L-1600		Unit	Notes
		Min	Max		
Write leveling hold from rising DQS, DQS# crossing to rising CK, CKB crossing	^{t}WLH	165	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	ns	

Notes: 1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.

2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit ^tCK (AVG) represents the actual ^tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^tIS, ^tIH, ^tDS, and ^tDH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, µs, ms) should use ^tCK (AVG) to determine the correct number of clocks uses CK or ^tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, JSC does not warrant compliance with normal mode timings or functionality.
10. The clock's ^tCK (AVG) is the average clock over any 200 consecutive clocks and ^tCK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^tCK (AVG) MIN.
12. The clock's ^tCH (AVG) and ^tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (^tJITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^tCL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter ^tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error $^tERRnper$, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. ^tDS (base) and ^tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.

19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ MAX, and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).
24. The maximum preamble is bound by ^{t}LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by ^{t}HZDQS(MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.
29. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3L SDRAM device supports $^{t}nPARAM$ (nCK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}nRP (nCK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 5ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for ^{t}WR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.

36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125μs. However, nine REFRESH commands should be asserted at least once every 70.3μs. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings.Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9nsmaximum.
39. Half-clock output parameters must be derated by the actual ^{t}ERR10per and ^{t}JITdty when input clock jitter is present. This results in each parameter becoming larger. Theparame- ters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODT timings .
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

    For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with ^{t}IS(AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

Electrical Characteristics and AC Operating Conditions

Electrical Characteristics and AC Operating Conditions for Speed Extensions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 (2133) Min	DDR3L-1866 (2133) Max	Unit	Notes
Clock Timing						
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^{t}CK (DLL_DIS)	8 (8)	7800(7800)	ns	9, 42
	T_C = >85°C to 95°C		8 (8)	3900(7800)	ns	42
Clock period average: DLL enable mode		^{t}CK (AVG)	See Speed Bin Tables for ^{t}CK range allowed ns			10, 11
High pulse width average		^{t}CH (AVG)	0.47 (0.47)	0.53 (0.53)	CK	12
Low pulse width average		^{t}CL (AVG)	0.47 (0.47)	0.53 (0.53)	CK	12
Clock period jitter	DLL locked	^{t}JITper	–60 (50)	60 (50)	ps	13
	DLL locking	^{t}JITper,lck	–50 (40)	50 (40)	ps	13
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper MAX ps			
Clock absolute high pulse width		^{t}CH (ABS)	0.43 (0.43)	–	^{t}CK (AVG)	14
Clock absolute low pulse width		^{t}CL (ABS)	0.43 (0.43)	–	^{t}CK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^{t}JITcc	120 (120)		ps	16
	DLL locking	^{t}JITcc,lck	100 (100)		ps	16

Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 (2133) Min	DDR3L-1866 (2133) Max	Unit	Notes
Cumulative error across	2 cycles	^{t}ERR2per	–88 (74)	88 (74)	ps	17
	3 cycles	^{t}ERR3per	–105 (87)	105 (87)	ps	17
	4 cycles	^{t}ERR4per	–117 (97)	117 (97)	ps	17
	5 cycles	^{t}ERR5per	–126 (105)	126 (105)	ps	17
	6 cycles	^{t}ERR6per	–133 (111)	133 (111)	ps	17
	7 cycles	^{t}ERR7per	–139 (116)	139 (116)	ps	17
	8 cycles	^{t}ERR8per	–145 (121)	145 (121)	ps	17
	9 cycles	^{t}ERR9per	–150 (125)	150 (125)	ps	17
	10 cycles	^{t}ERR10per	–154 (128)	154 (128)	ps	17
	11 cycles	^{t}ERR11per	–158 (132)	158 (132)	ps	17
	12 cycles	^{t}ERR12per	–161 (134)	161 (134)	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper MAX		ps	17
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DS (AC130)	70(55)	–	ps	18, 19
	V_{REF} @ 2 V/ns		135(120.5)	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DH (DC90)	75(60)	–	ps	18, 19
	V_{REF} @ 2 V/ns		110(105)	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	320(280)	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	85 (75)	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38(0.38)	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CKB		^{t}LZDQ	–390 (360)	195(180)	ps	22, 23
DQ High-Z time from CK, CKB		^{t}HZDQ	–	195(180)	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CKB rising		^{t}DQSS	–0.27(0.27)	0.27(0.27)	CK	25
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45(0.45)	0.55(0.55)	CK	

Table 59: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 (2133) Min	DDR3L-1866 (2133) Max	Unit	Notes
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45(0.45)	0.55(0.55)	CK	
DQS, DQS# falling setup to CK, CKB rising		^{t}DSS	0.18(0.18)	_	CK	25
DQS, DQS# falling hold from CK, CKB rising		^{t}DSH	0.18(0.18)	_	CK	25
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9(0.9)	_	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3(0.3)	_	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CKB		^{t}DQSCK	–195 (180)	195 (180)	ps	23
DQS, DQS# rising to/from rising CK, CKB when DLL is disabled		^{t}DQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		^{t}QSH	0.40 (0.4)	_	CK	21
DQS, DQS# differential output low time		^{t}QSL	0.40 (0.4)	_	CK	21
DQS, DQS# Low-Z time (RL - 1)		^{t}LZDQS	–390(360)	195(180)	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		^{t}HZDQS	–	195(180)	ps	22, 23
DQS, DQS# differential READ preamble		^{t}RPRE	0.9(0.9)	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^{t}RPST	0.3(0.3)	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		^{t}DLLK	512(512)	_	CK	28
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	^{t}IS (AC135)	65(60)	_	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200(195)	_	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	^{t}IS (AC125)	150(135)	_	ps	29, 30, 44
	V_{REF} @ 1 V/ns		275(260)	_	ps	20, 30
CTRL, CMD, ADDR hold from CK,CKB	Base (specification)	^{t}IH (DC90)	110 (95)	_	ps	29, 30
	V_{REF} @ 1 V/ns		200(195)	_	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	535(470)	_	ps	41
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD		ns	31
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP		ns	31
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS		ns	31, 32
ACTIVATE-to-ACTIVATE command period		^{t}RC	See Speed Bin Tables for ^{t}RC		ns	31, 43

Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 (2133)		Unit	Notes
			Min	Max		
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	^{t}RRD	MIN = greater of 4CK or 5ns		CK	31
	2KB page size		MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows	1KB page size	^{t}FAW	27 (25)	-	ns	31
	2KB page size		35 (35)	_	ns	31
Write recovery time		^{t}WR	MIN = 15ns; MAX = N/A		ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32
CASB-to-CASB command delay		^{t}CCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	MIN = N/A MAX = MAX(512nCK, 640ns)		CK	
	Normal operation	^{t}ZQoper	MIN = N/A MAX = max(256nCK, 320ns)		CK	
ZQCS command: Short calibration time			MIN = N/A MAX = max(64nCK, 80ns) ^{t}ZQCS		CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						

Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866(2133) Min	DDR3L-1866(2133) Max	Unit	Notes
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb	MIN = 110; MAX = 70,200		ns	
		^{t}RFC – 2Gb	MIN = 160; MAX = 70,200		ns	
		^{t}RFC – 4Gb	MIN = 260; MAX = 70,200		ns	
		^{t}RFC – 8Gb	MIN = 350; MAX = 70,200		ns	
Maximum refresh period	$T_C \le 85°C$	–	64 (1X)		ms	36
	$T_C > 85°C$		32 (2X)		ms	36
Maximum average periodic refresh	$T_C \le 85°C$	^{t}REFI	7.8 (64ms/8192)		µs	36
	$T_C > 85°C$		3.9 (32ms/8192)		µs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing						
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay		^{t}CPDED	MIN = 2; MAX = N/A		CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 * tREFI		CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL		CK	
Power-Down Entry Minimum Timing						

Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866(2133)				Unit	Notes
			Min		Max			
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 2				CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 2				CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 2				CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)				CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1				CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)				CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)				CK	
WRITE with auto pre-charge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAP-DEN	MIN = WL + 4 + WR + 1				CK	
	BC4MRS	^{t}WRAP-DEN	MIN = WL + 2 + WR + 1				CK	
Power-Down Exit Timing								
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A				CK	28
ODT Timing								
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK				CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK				CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–195(180)		–195(180)		ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5				ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5				ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A				CK	

Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3L-1866(2133)		Unit	Notes
		Min	Max		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing					
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew	^{t}ADC	0.3(0.3)	0.7(0.7)	CK	39
Write Leveling Timing					
First DQS, DQS# rising edge	^{t}WLMRD	40 (40)	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25 (25)	–	CK	
Write leveling setup from rising CK, CKB crossing to rising DQS, DQS# crossing	^{t}WLS	140 (125)	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CKB crossing	^{t}WLH	140 (125)	–	ps	
Write leveling output delay	^{t}WLO	0	7.5(7.0)	ns	
Write leveling output error	^{t}WLOE	0	2 (2)	ns	

Notes: 1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.

2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit ^tCK (AVG) represents the actual ^tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^tIS, ^tIH, ^tDS, and ^tDH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, μs, ms) should use ^tCK (AVG) to determine the correct number of clocks uses CK or ^tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQSdiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, JSC does not warrant compliance with normal mode timings or functionality.
10. The clock's ^tCK (AVG) is the average clock over any 200 consecutive clocks and ^tCK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^tCK (AVG) MIN.
12. The clock's ^tCH (AVG) and ^tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (^tJITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^tCL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter ^tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error $^tERRnper$, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. ^tDS (base) and ^tDH (base) values are for a single-ended 1 V/ns slew rate DQs (DQs are at 2V/ns for DDR3-1866/2133) and 2 V/ns slew rate differential DQS, DQS#; when DQ single- ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.

19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (towhich derating tables apply) to V_{REF} when the slew rate is 1 V/ns (DQs areat 2V/ns for DDR3-1866/2133). These values, witha slew rate of 1 V/ns (DQs are at 2V/ns for DDR3-1866/2133), are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ (MAX), and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).
24. The maximum preamble is bound by ^{t}LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by ^{t}HZDQS(MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.
29. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3L SDRAM device supports $^{t}nPARAM$ (nCK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For exam- ple, the device will support ^{t}nRP (nCK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifi- cations are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 5ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has beensatisfied.
33. When operating in DLL disable mode, the greater of 5CK or 15ns is satisfied for ^{t}WR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles afterWL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles afterWL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in exces- sive current, depending on bus activity.

36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings.Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9nsmaximum.
39. Half-clock output parameters must be derated by the actual ^{t}ERR10per and ^{t}JITdtywhen input clock jitter is present. This results in each parameter becoming larger. Theparameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODTtimings.
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

    For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with ^{t}IS(AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

Command and Address Setup, Hold, and Derating

The total ^{t}IS (setuptime) and ^{t}IH (holdtime) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) values to the Δ^{t}IS and Δ^{t}IH derating values respectively. Example: ^{t}IS (totalsetuptime) = ^{t}IS (base) + Δ^{t}IS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time ^{t}VAC.

Although the total setup time for slow slew rates might be negative (for example,a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$ for input signal requirements). The derating values may be obtained by linear interpolation.

Setup(^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derat- ingvalue.If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal fromthe AC level to the DC level is used for derating value.

Hold(^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold(^{t}IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for derating value .

DDR3L Command and Address Setup and Hold Values 1 V/ns Referenced – AC/DC-Based

Symbol	1600	1866	2133	Unit	Reference
^{t}IS(base, AC160)	60	–	-	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS(base, AC135)	185	65	60	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS(base, AC125)	–	150	135	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IH(base, DC90)	130	110	105	ps	$V_{IH(DC)}/V_{IL(DC)}$

DDR3L-1600 Derating Values for $^tIS/^tIH$ – AC135/DC90-Based

CMD/ADDR Slew Rate V/ns	Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based															
	CK, CKB Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

DDR3L-1866/2133 Derating Values for $^tIS/^tIH$ – AC125/DC90-Based

CMD/ADDR Slew Rate V/ns	Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based															
	CK, CKB Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80

DDR3L-1866/2133 Derating Values for ^{t}IS/^{t}IH – AC125/DC90-Based (Continued)

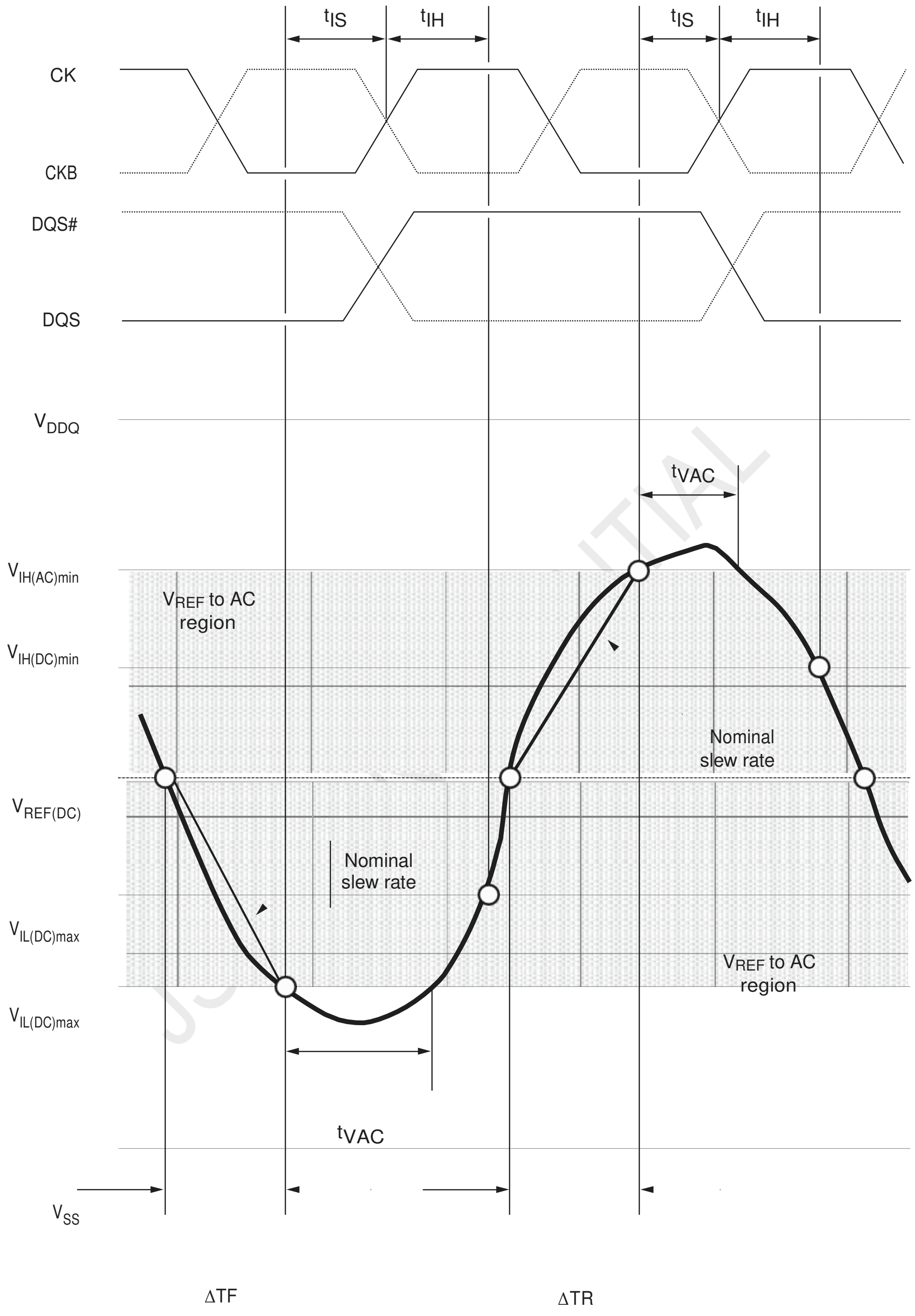
Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CKB Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	3	–3	3	–3	3	–3	11	5	19	13	27	21	35	31	43	47
0.8	6	–8	6	–8	6	–8	14	1	22	9	30	17	38	27	46	43
0.7	10	–13	10	–13	10	–13	18	–5	26	3	34	11	42	21	50	37
0.6	16	–20	16	–20	16	–20	24	–12	32	–4	40	4	48	14	56	30
0.5	15	–30	15	–30	15	–30	23	–22	31	–14	39	–6	47	4	55	20
0.4	13	–45	13	–45	13	–45	21	–37	29	–29	37	–21	45	–11	53	5

DDR3L Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition

Slew Rate (V/ns)	DDR3L-1600		DDR3L-1866/2133	
	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 125mV (ps)
>2.0	200	213	200	205
2.0	200	213	200	205
1.5	173	190	178	184
1.0	120	145	133	143
0.9	102	130	118	129
0.8	80	111	99	111
0.7	51	87	75	89
0.6	13	55	43	59
0.5	Note 1	10	Note 1	18
<0.5	Note 1	10	Note 1	18

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Nominal Slew Rate and tVAC for tIS (Command and Address - Clock)

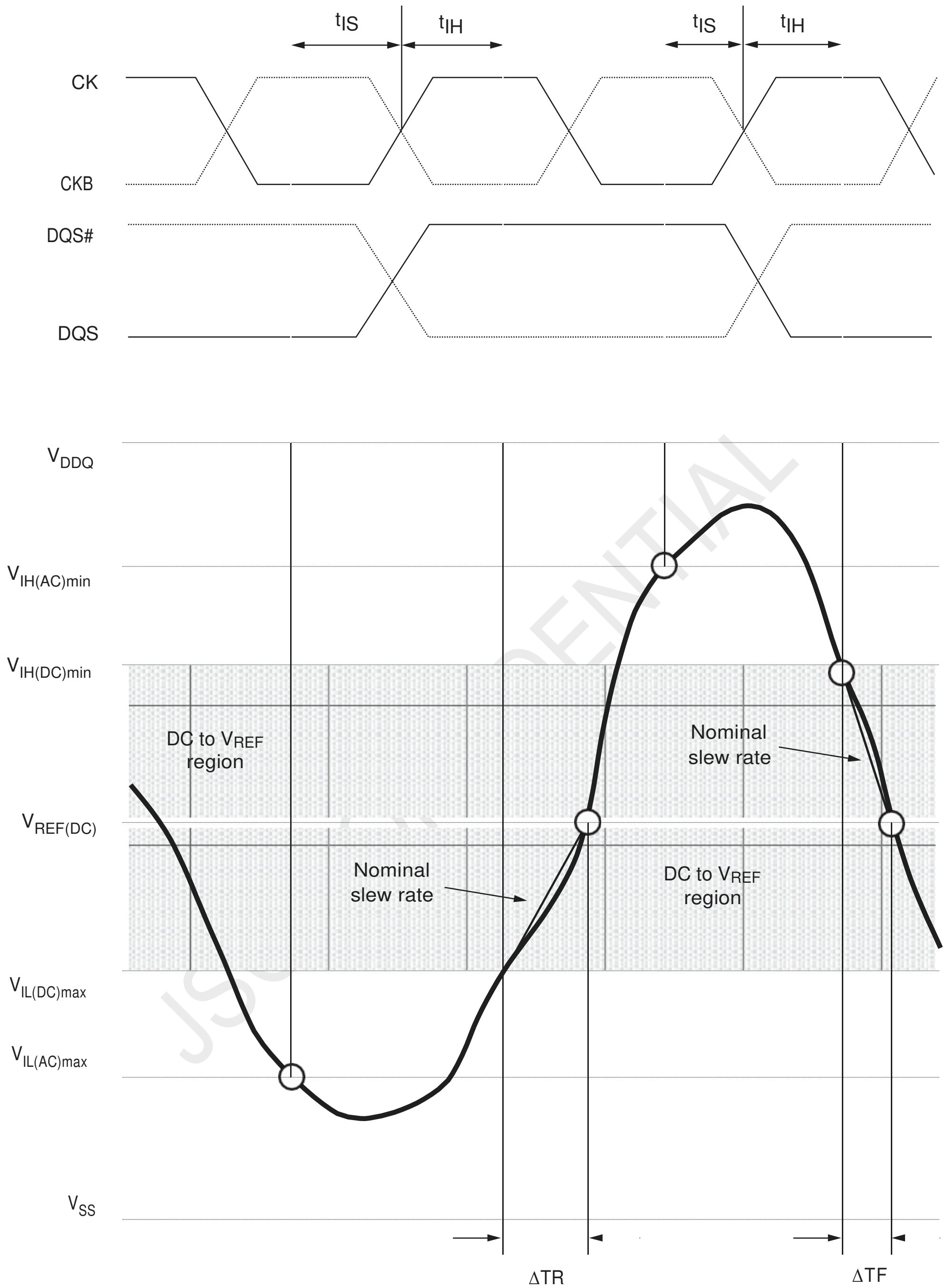


Setup slew rate falling signal = $\frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$

Setup slew rate rising signal = $\frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$

Note: 1. The clock and the strobe are drawn on different time scales.

Nominal Slew Rate for ᵗIH (Command and Address - Clock)

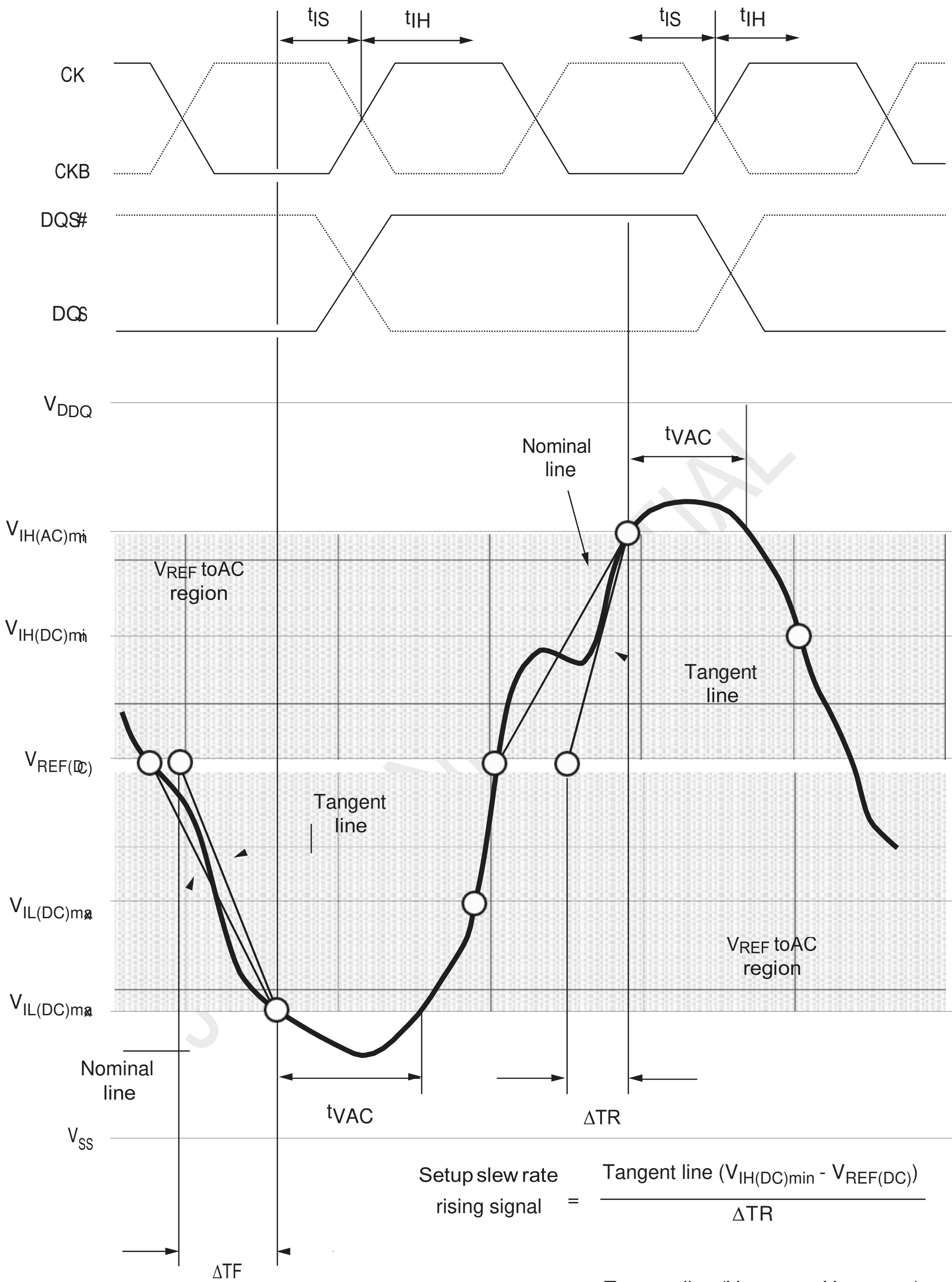


$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Tangent Line for ᵗIS (Command and Address - Clock)

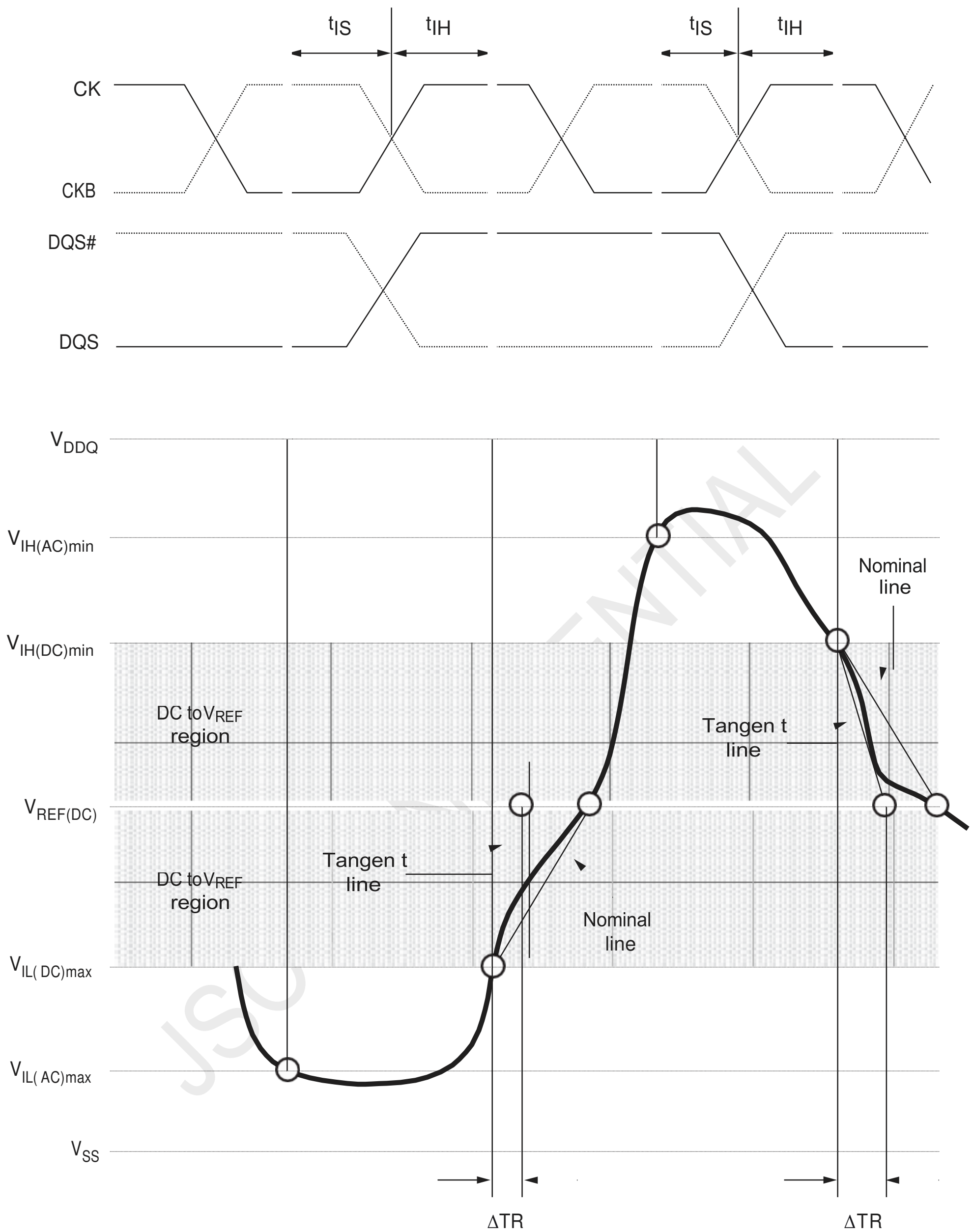


$$\text{Setup slew rate rising signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TR}$$

$$\text{Setup slew rate falling signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(AC)max})}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Tangent Line for tIH (Command and Address - Clock)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(DC)max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Data Setup, Hold, and Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the

tDS and tDH (see Table 77) derating value respectively. Example: tDS (total setup time) = tDS(base) + tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

If the actual signal is always earlier than the nominal slew rate line between shaded ‘VREF(dc) to ac region’, use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ‘VREF(dc) to ac region’, the slew rate of a tangent line to the actual signal from the ac level to VREF(dc) level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

If the actual signal is always later than the nominal slew rate line between shaded ‘dc level to VREF(dc) region’, use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded ‘dc to VREF(dc) region’, the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

DDR3L Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based

Symbol	1600	1866	2133	Unit	Reference
^{t}DS (base) AC160	–	–	-	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DS (base) AC135	25	–	-	ps	
^{t}DS (base) AC130	-	70	55	ps	
^{t}DH (base) DC90	55	–	-	ps	
^{t}DH (base) DC90	–	75	60	ps	
Slew Rate Referenced	1	2	2	V/ns	

DDR3L Derating Values for ${}^{t}DS/{}^{t}DH$ - AC160/DC90-Based

DQ Slew Rate V/ns	ΔtDS, ΔtDH Derating (ps) – AC/DC-Based															
	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–1	–3	–1	–3	7	5	15	13	23	21				
0.8					–3	–8	5	1	13	9	21	17	29	27		
0.7							–3	–5	11	3	19	11	27	21	35	37
0.6									8	–4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													–8	–11	0	5

DDR3L Derating Values for ${}^{t}DS/{}^{t}DH$ - AC135/DC90-Based

DQ Slew Rate V/ns	ΔtDS, ΔtDH Derating (ps) – AC/DC-Based															
	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

DDR3L Derating Values for $^tDS/^tDH$ – AC130/DC90-Based at 2V/ns

Shaded cells indicate slew rate combinations not supported

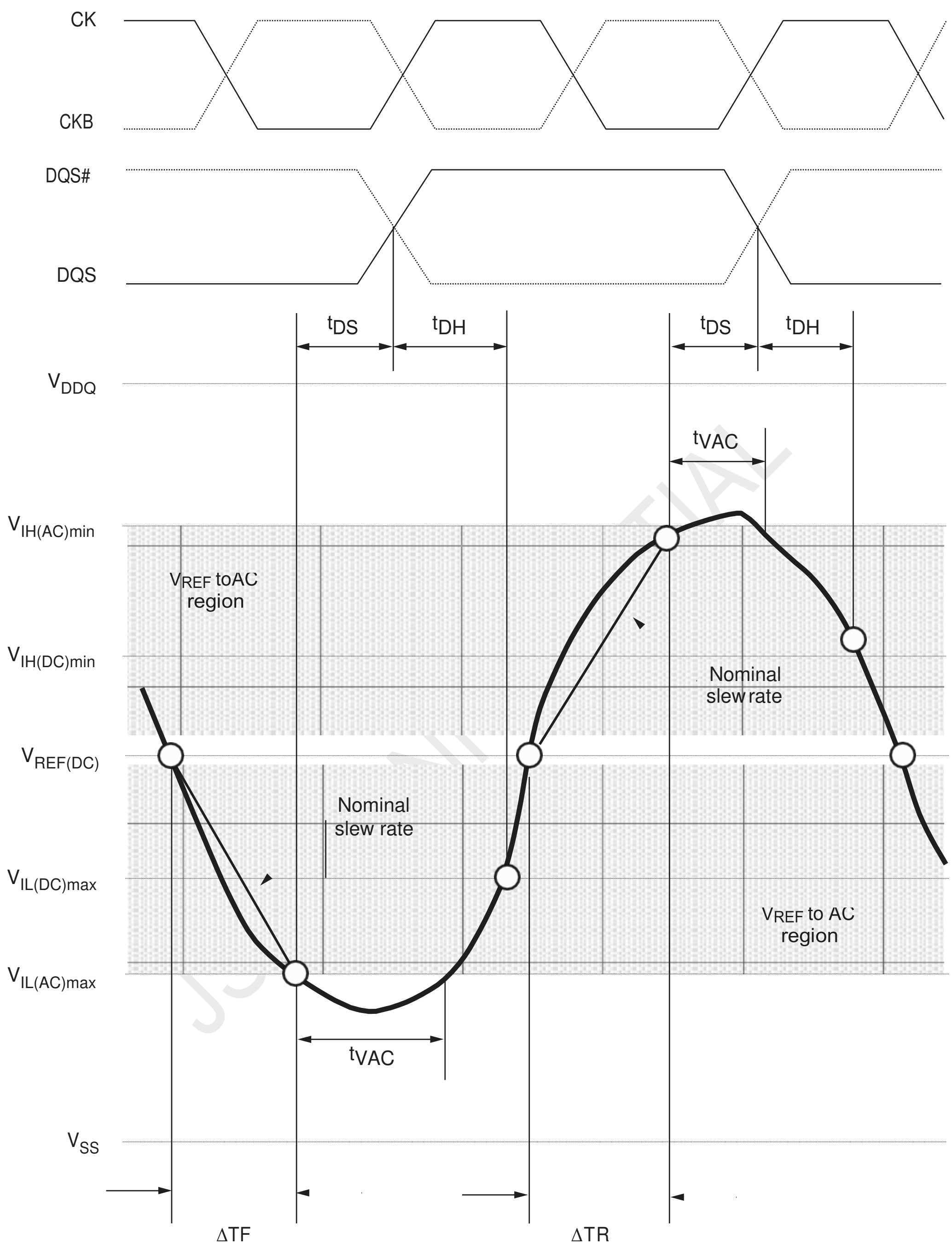
DQ Slew Rate V/ns	Δ^tDS, Δ^tDH Derating (ps) – AC/DC-Based																							
	DQS, DQS# Differential Slew Rate																							
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH	Δ ^tDS	Δ ^tDH
4.0	33	23	33	23	33	23																		
3.5	28	19	28	19	28	19	28	19																
3.0	22	15	22	15	22	15	22	15	22	15														
2.5			13	9	13	9	13	9	13	9	13	9												
2.0					0	0	0	0	0	0	0	0	0	0										
1.5							–22	–15	–22	–15	–22	–15	–22	–15	–14	–7								
1.0									–65	–45	–65	–45	–65	–45	–57	–37	–49	–29						
0.9											–62	–48	–62	–48	–54	–40	–46	–32	–38	–24				
0.8													–61	–53	–53	–45	–45	–37	–37	–29	–29	–19		
0.7															–49	–50	–41	-42	–33	–34	–25	–24	–17	–8
0.6																	–37	–49	–29	–41	–21	–31	–13	–15
0.5																			–31	–51	–23	–41	–15	–25
0.4																					–28	–56	–20	–40

DDR3L Minimum Required Time ᵗVAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition

Slew Rate (V/ns)	DDR3L-1866/2133 130mV (ps) min
>2.0	95
2.0	95
1.5	73
1.0	30
0.9	16
0.8	Note 1
0.7	–
0.6	–
0.5	–
<0.5	–

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Nominal Slew Rate and ^{t}VAC for ^{t}DS (DQ – Strobe)

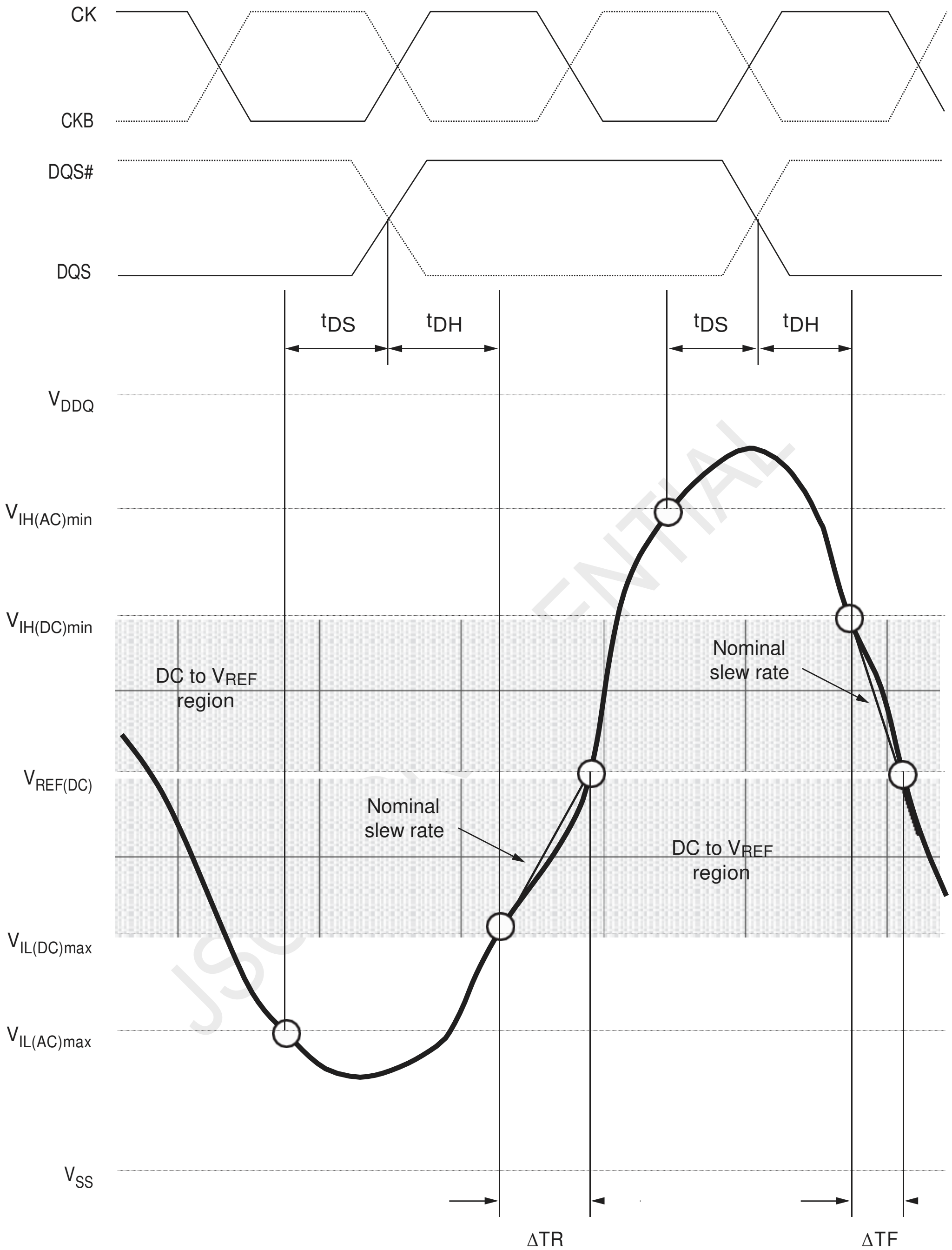


Setup slew rate falling signal $= \dfrac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$

Setup slew rate rising signal $= \dfrac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$

Note: 1. The clock and the strobe are drawn on different time scales.

Nominal Slew Rate for ᵗDH (DQ – Strobe)

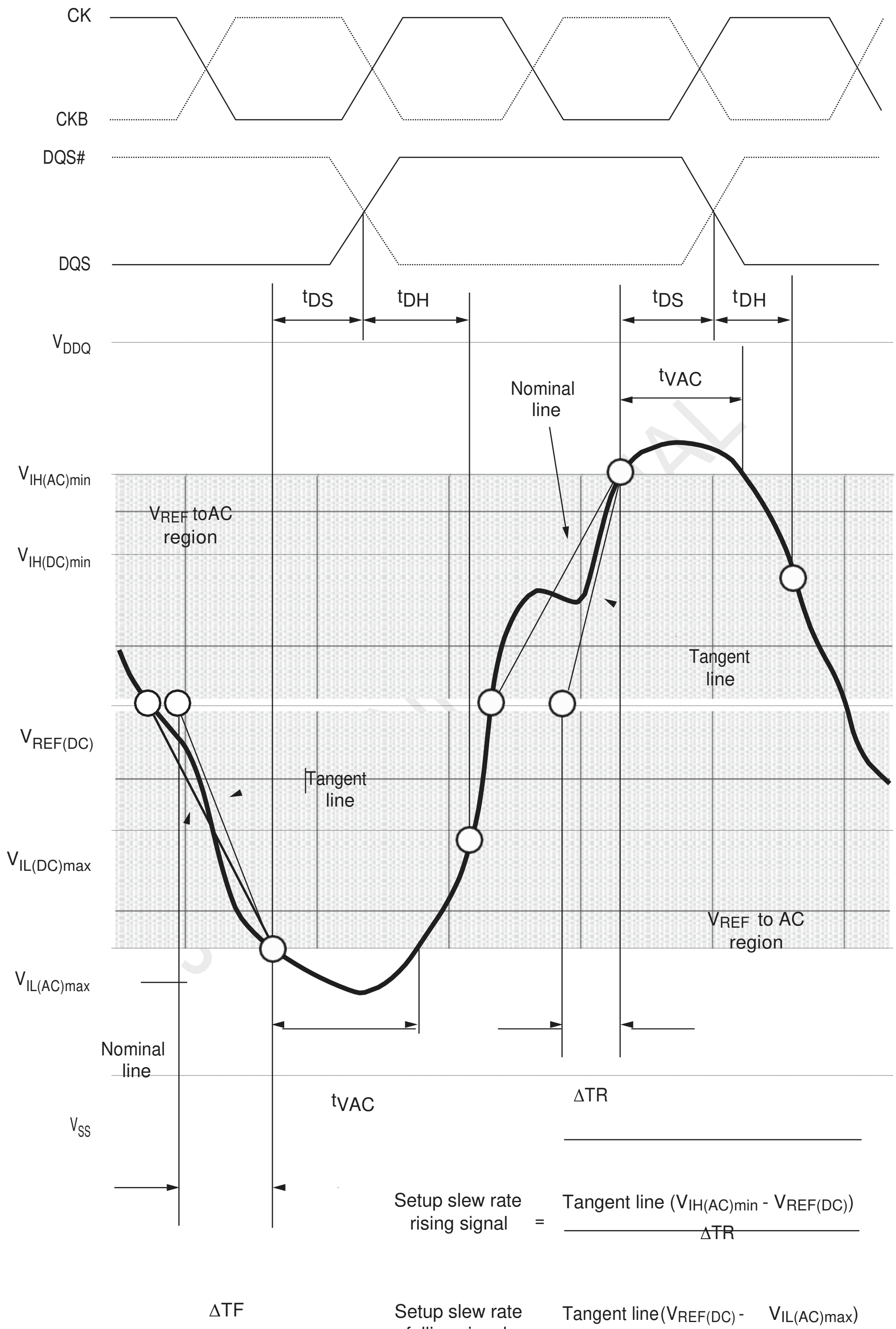


$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IL(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Tangent Line for ^{t}DS (DQ - Strobe)

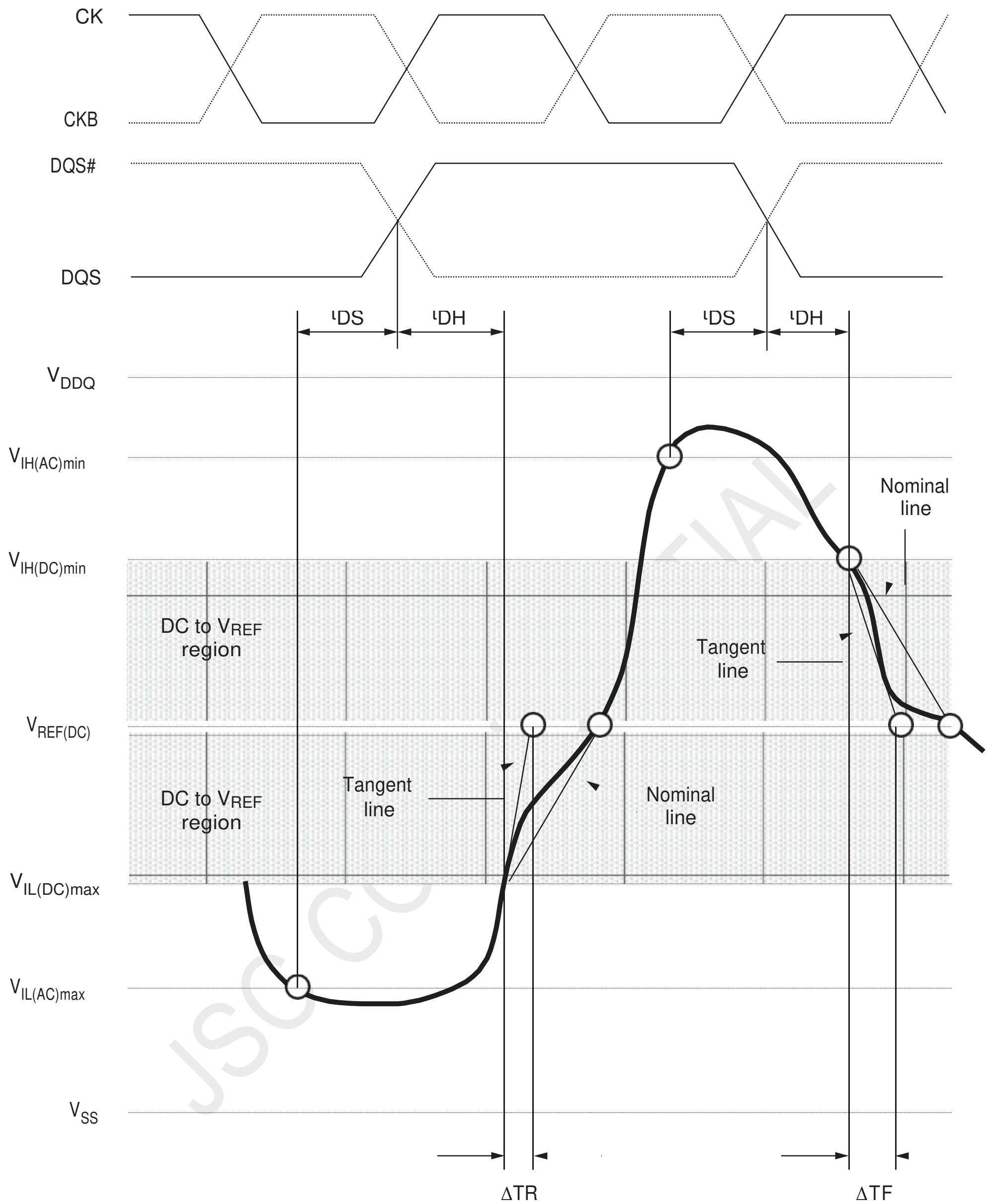


$$\text{Setup slew rate rising signal} = \frac{\text{Tangent line}\,(V_{IH(AC)min} - V_{REF(DC)})}{\Delta TR}$$

$$\text{Setup slew rate falling signal} = \frac{\text{Tangent line}\,(V_{REF(DC)} - V_{IL(AC)max})}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Tangent Line for tDH (DQ - Strobe)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(DC)max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Commands – Truth Tables

Truth Table – Command

Notes 1–5 apply to the entire table

Function		Symbol	CKE		CSB	RASB	CASB	WEB	BA [2:0]	An	A12	A10	A[11, 9:0]	Notes
			Prev. Cycle	Next Cycle										
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6, 7
					L	H	H	H						
Single-bank PRECHARGE		PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	L	H	L	V		V	H	V	
Bank ACTIVATE		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
Power-down exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6, 11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes: 1. Commands are defined by the states of CSB, RASB, CASB, WEB, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configuration-dependent.

2. RESETB is enabled LOW and used only for asynchronous reset. Thus, RESETB must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.
4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. “V” means “H” or “L” (a defined logic level), and “X” means “Don’t Care.”
6. Additional information on CKE transition.
7. Self refresh exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

Truth Table - CKE

Notes 1–2 apply to the entire table; for additional command details

Current State[3]	CKE Previous Cycle[4] (n - 1)	CKE Present Cycle[4] (n)	Command[5] (RASB, CASB, WEB,	Action[5]	Notes
Power-down	L	L	"Don't Care"	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self refresh	L	L	"Don't Care"	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self refresh	

Notes: 1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

2. ^tCKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^tIS + ^tCKE (MIN) + ^tIH.
3. Current state = The state of the DRAM immediately prior to clock edge n.
4. CKE (n) is the logic state of CKE at clock edge n; CKE (n - 1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge. Action is a result of COMMAND. ODT does not affect the states described in this table and is notlisted.
6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

Commands

DESELECT

The DESELT (DES) command (CSB HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NOOPERATION

The NO OPERATION (NOP) command (CSB LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION LONG

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization and reset sequence .
This command may be issued a tany time by the controller,depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated R_{ON} and ODT values.

The DRAM is allowed a timing window defined by either ^{t}ZQ init or ^{t}ZQoper to perform a full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter ^{t}ZQinit must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter ^{t}ZQoper to be satisfied.

ZQ CALIBRATION SHORT

The ZQCALIBRATION SHORT(ZQCS) command is used to perform periodic calibrations to account for small voltage and temperature variations. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter ^{t}ZQCS. A ZQCS command can effectively correct a minimum of 0.5% R_{ON} and R_{TT} impedance error within 64 clock cycles, assuming the maximum sensitivities specified in DDR3L 34 Ohm Output Driver Sensitivity.

ACTIVATE

The ACTIVATE command is used to open(oractivate) a rowin a particular bank for a subsequent access.The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[n:0]selects the row. This row remains open(oractive) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address, depending on the burst length and burst type selected (see Burst Order table for additional information). The value on input A10 determines whether auto precharge is used. If auto precharge is selected,the row being accessed will be precharged attheend of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value oninput A12(ifenabledinthe moderegister) when the READcommand is issued determines whether BC4(chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted.

READ Command Summary

Function		Symbol	CKE Prev. Cycle	CKE Next Cycle	CSB	RASB	CASB	WEB	BA [2:0]	A*n*	A12	A10	A[11, 9:0]
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether auto precharge is used. The value on input A12(ifenabledinthe MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory.If the DM signal is registered HIGH, the corresponding data inputs will be ignored an da WRITE will not be executed to that byte/column location.

WRITE Command Summary

Function		Symbol	CKE Prev. Cycle	CKE Next Cycle	CSB	RASB	CASB	WEB	BA [2:0]	A*n*	A12	A10	A[11, 9:0]
WRITE	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

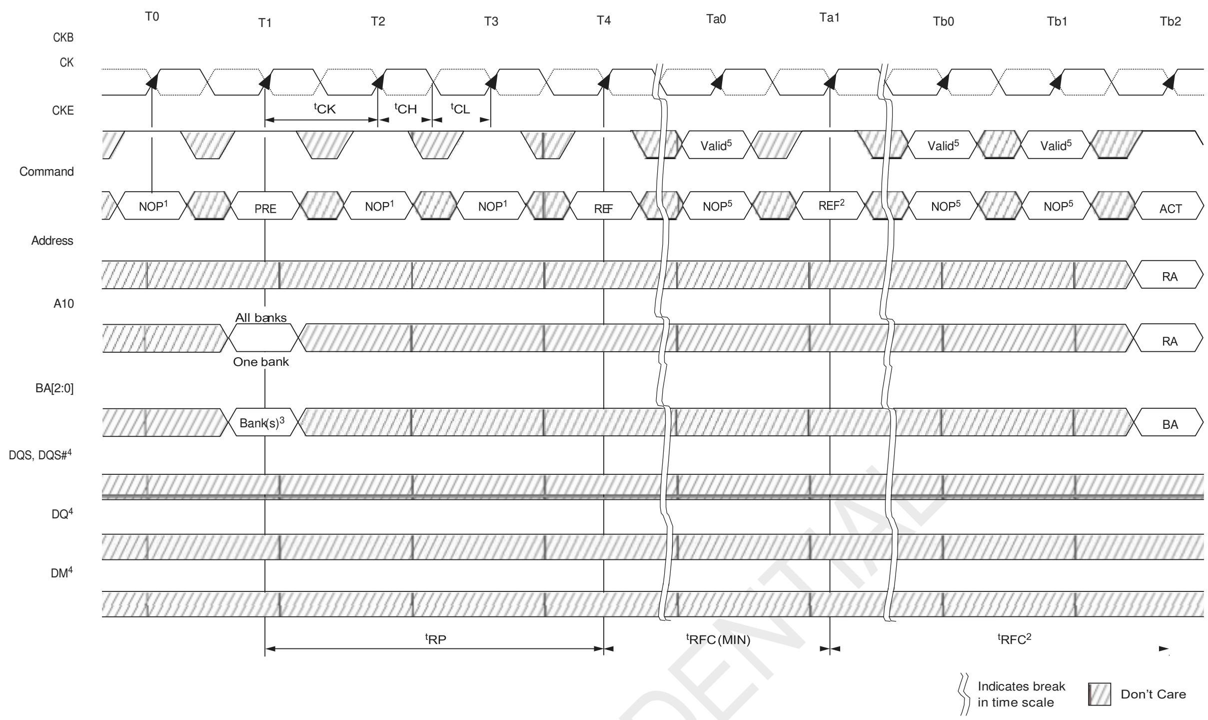
REFRESH

The REFRESH command is used during normal operation of the DRAM and is an alogous to CASB-before-RASB (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command. The DRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when $T_C \leq$ 85°C or 3.9µs maximum when $T_C \leq$ 95°C). The REFRESH period begins when the REFRESH command is registered and ends ^tRFC (MIN) later.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and then ext REFRESH command is nine times the maximum average interval refresh rate. Self refresh may be entered with up to eight REFRESH commands being posted. After exiting self refresh (when entered with posted REFRESH commands), additional posting of REFRESH commands is allowed to the extent that the maximum number of cumulative posted REFRESH commands (both pre- and post-self refresh) does not exceed eight REFRESH commands.

At any given time, a maximum of 16 REFRESH commands can be issued within 2x^tREFI.

Refresh Mode



Notes: 1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see Power-Down Mode..

2. The second REFRESH is not required, but two back-to-back REFRESH commands are shown.
3. "Don't Care" if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all "Don't Care"/High-Z.
5. Only NOP and DES commands are allowed after a REFRESH command and until ^{t}RFC (MIN) issatisfied.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in self refresh mode, the DRAM retains data without external clocking. Self refresh mode is also ac onvenient method used to enable/disable the DLL as well as to change the clock frequency within the allowed synchronous operatingrange (see Input Clock Frequency Change. All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. V_{REFDQ} may float or not driveV_{DDQ}/2while inself refresh mode under the following conditions:

- $V_{SS} < V_{REFDQ} < V_{DD}$ is maintained
- V_{REFDQ} is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after V_{REFDQ} is valid
- All other self refresh mode exit timing requirements are met

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0]can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode, with a few not able exceptions:

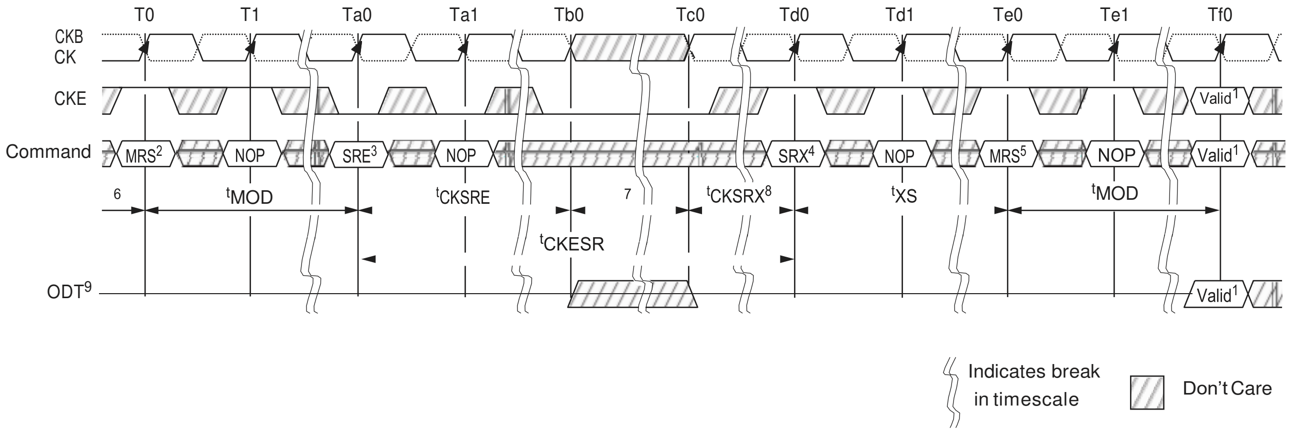
- The DRAM supports only one value of CAS latency(CL=6) and one value of CAS WRITE latency (CWL = 6).
- DLL disable mode affects there add at a clock-to-data strobe relationship (^{t}DQSCK), but not the read data-to-datastrobe relationship (^{t}DQSQ,^{t}QH). Specialattentionis required to line up the read data with the controller time domain when the DLL is disabled.
- In normal operation (DLLon), ^{t}DQSCK starts from the rising clock edge AL+ CL cycles after the READ command. In DLL disable mode,^{t}DQSCK starts AL+CL-1cycles after the READ command. Additionally, with the DLL disabled, the value of ^{t}DQSCK could be larger than ^{t}CK.

The ODT feature (including dynamic ODT) is not supported during DLL disable mode. The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming $R_{TT,nom}$ MR1[9,6,2] and $R_{TT(WR)}$ MR2[10,9] to0 while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes (^{t}CK[AVG] MAX and ^{t}CK[DLL_DIS] MIN,respectively).The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh:

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and $R_{TT,nom}$ and $R_{TT(WR)}$ are High-Z), set MR1[0] to 1 to disable the DLL.
2. Enter self refresh mode after ^{t}MOD has been satisfied.
3. After ^{t}CKSRE is satisfied, change the frequency to the desired clock rate.
4. Self refresh maybe exited when the clock is stable with the new frequency for ^{t}CKSRX. After ^{t}XS is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of ^{t}MRDor ^{t}MOD has been satisfied. AZQCL command should be issued with appropriate timings met.

DLL Enable Mode to DLL Disable Mode

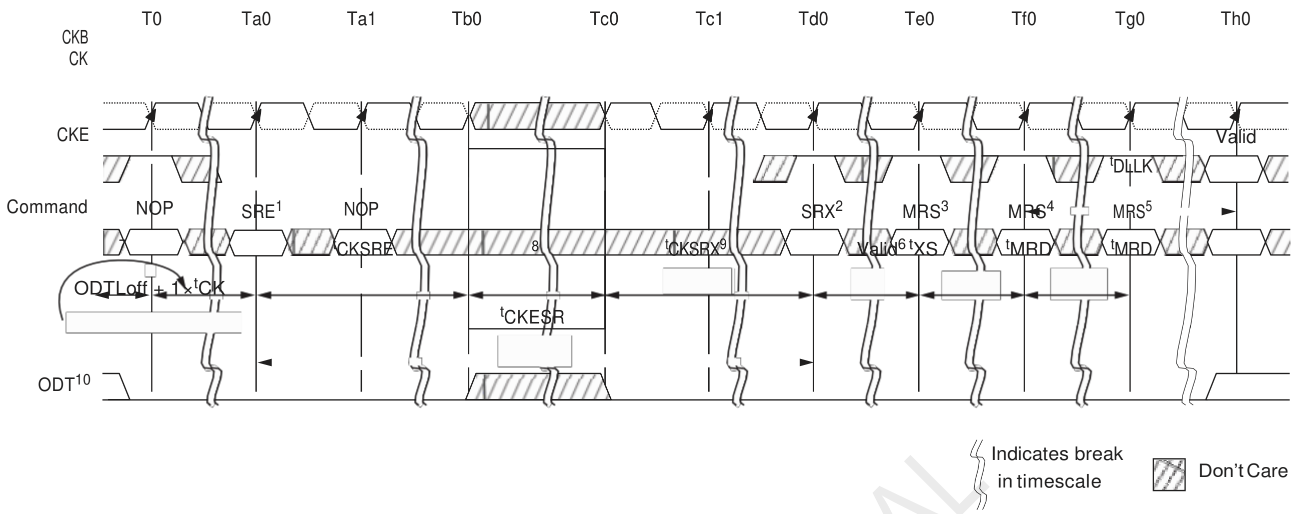


Notes: 1. Any valid command.
2. Disable DLL by setting MR1[0] to 1.
3. Enter SELFREFRESH.
4. Exit SELFREFRESH.
5. Update the mode registers with the DLL disable parameters setting.
6. Starting with the idle state, R_{TT} is in the High-Z state.
7. Change frequency.
8. Clock must be stable tCKSRX.
9. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

Asimilarprocedure isrequiredforswitching fromthe DLLdisable mode backto the DLL enable mode. This also requires changing the frequency during self refresh mode .Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off,and $R_{TT,nom}$ and $R_{TT(WR)}$ areHigh-Z),enter self refresh mode.

1. After tCKSRE is satisfied, change the frequency to the new clock rate.
2. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0]to 0 to enable the DLL. Wait tMRD, then set MR0[8] to 1 to enable DLL RESET.
3. After another tMRD delay is satisfied, update the remaining mode registers with the appropriate values.
4. The DRAMwill be ready for its next command in the DLL enable mode after the greater of tMRD or tMOD has been satisfied. However, before applying any command or function requiring a locked DLL,a delay of tDLLKafter DLLRESET must be satisfied. A ZQCL command should be issued with the appropriate timings met.

DLL Disable Mode to DLL Enable Mode



Notes:
1. Enter SELF REFRESH.
2. Exit SELFREFRESH.
3. Wait tXS, then set MR1[0] to 0 to enable DLL.
4. Wait tMRD, then set MR0[8] to 1 to begin DLL RESET.
5. Wait tMRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait tMOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least tCKSRX.
10. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

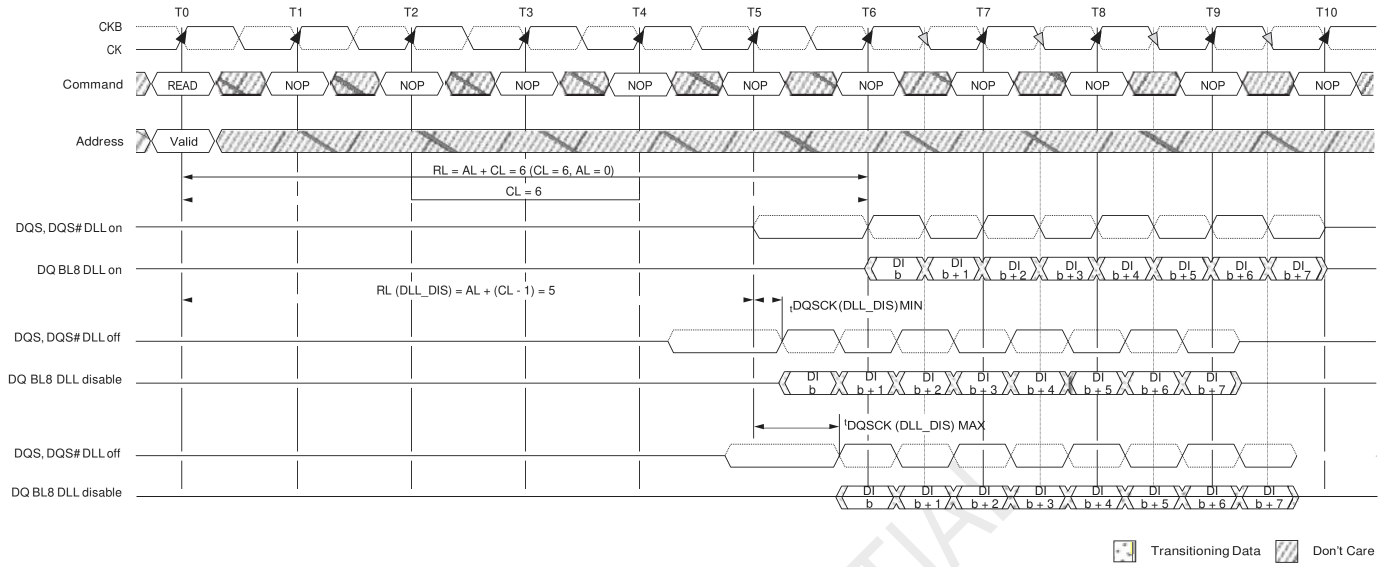
The clock frequency range for the DLL disable mode is specified by the parameter tCK (DLL_DIS).Due to latency counter and timing restrictions,only CL=6 and CWL=6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (tDQSCK) but not the data strobe to data relationship (tDQSQ, tQH). Special at tention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where tDQSCK starts from the rising clock edge AL+CL cycles after the READ command, the DLL disable mode tDQSCK starts AL+ CL-1 cycles after the READ command.

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

DLL Disable ^{t}DQSCK



READ Electrical Characteristics, DLL Disable Mode

Parameter	Symbol	Min	Max	Unit
Access window of DQS from CK, CKB	^{t}DQSCK (DLL_DIS)	1	10	ns

Input Clock Frequency Change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

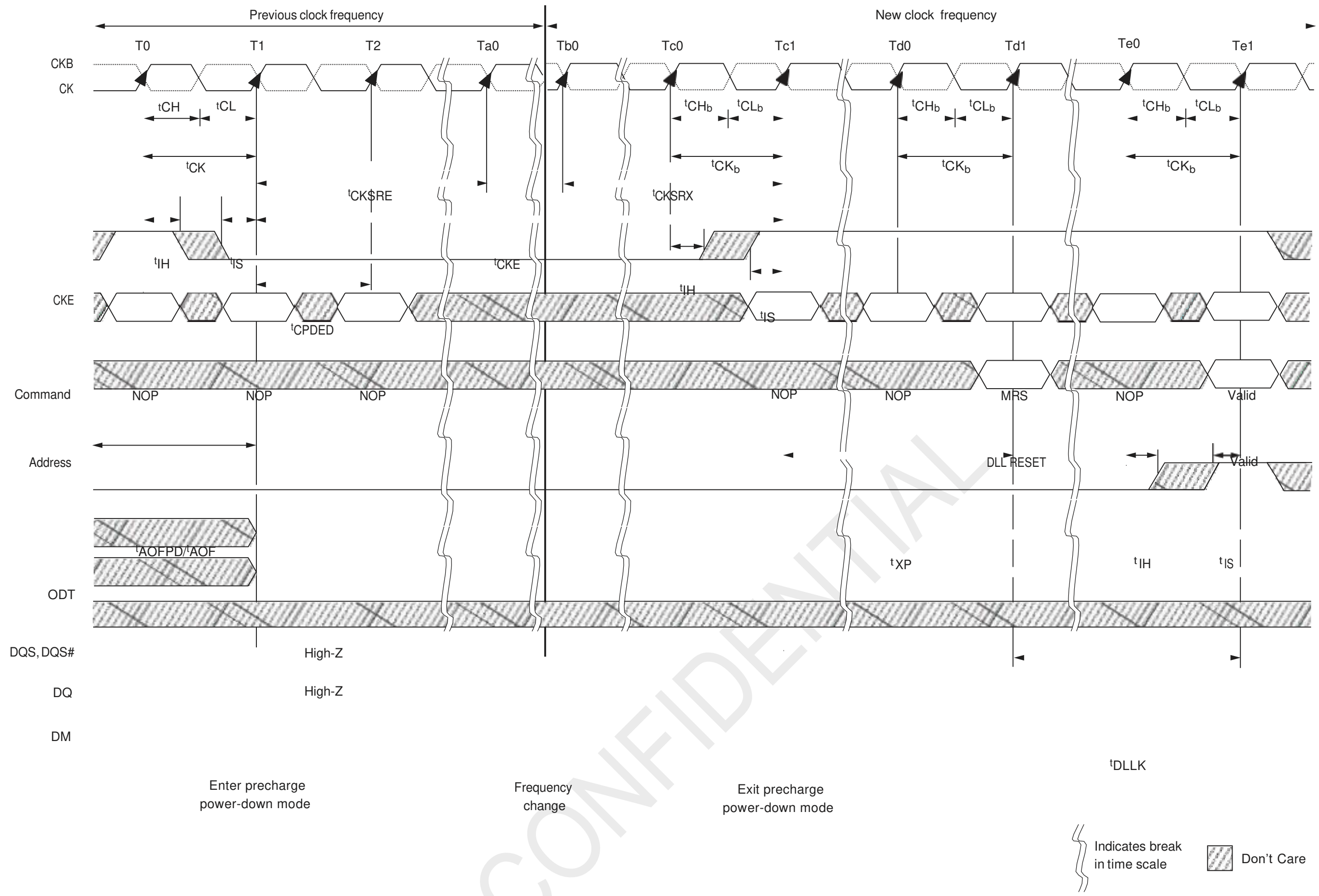
For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined.

The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure".

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state.

If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

Change Frequency During Precharge Power-Down



Notes: 1. Applicable for both SLOW-EXIT and FAST-EXIT precharge power-down modes.

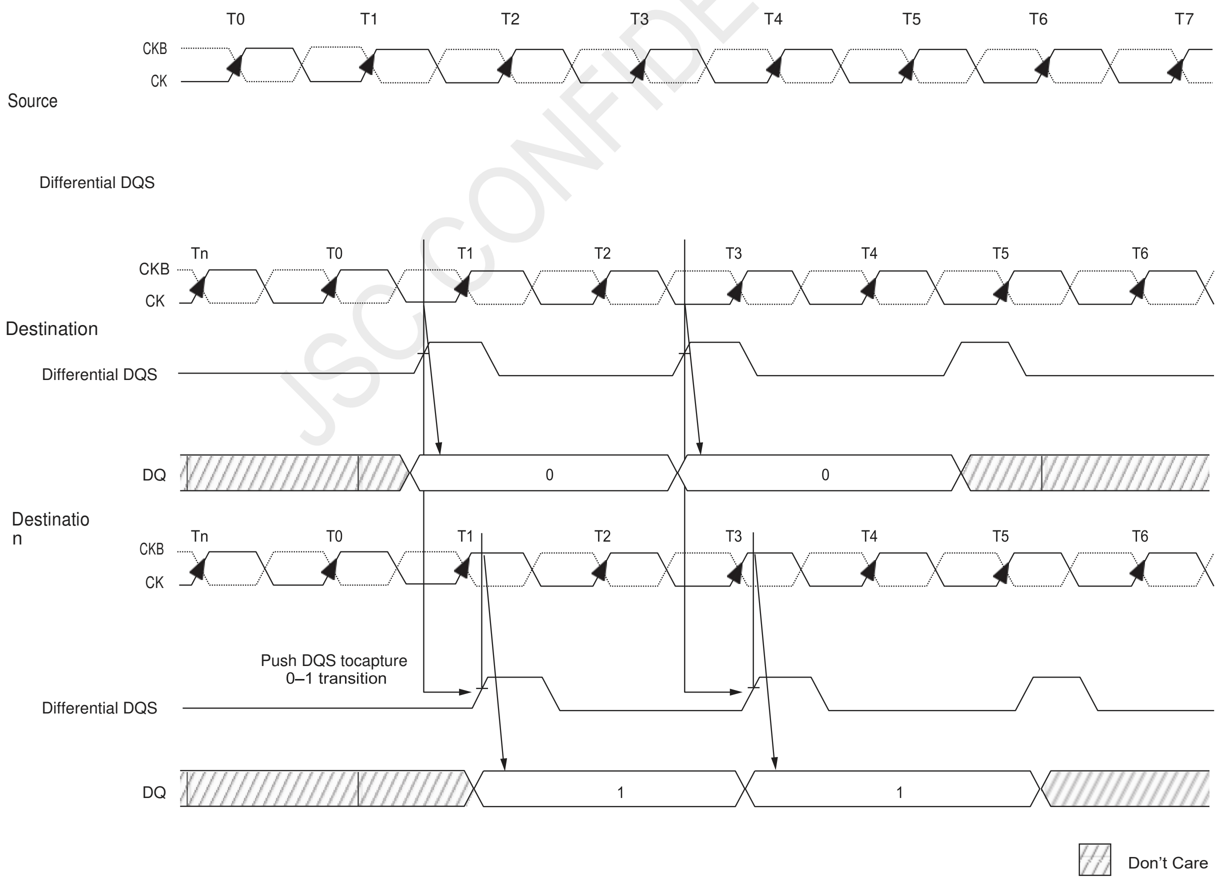
2. tAOFPD and tAOF must be satisfied and outputs High-Z prior to T1 (see On-Die Termination (ODT) for exactrequirements).

3. If the $R_{TT,nom}$ feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW, ensuring R_{TT} is in an off state. If the $R_{TT,nom}$ feature was disabled in the mode register prior to entering precharge power-down mode, R_{TT} will remain in the off state. The ODT signal can be registered LOW or HIGH in this case.

Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM.
This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS -DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals.
Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification.

Write Leveling Concept



DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship..

Write Leveling Matrix

Note 1 applies to the entire table

MR1[7]	MR1[12]	MR1[2, 6, 9]		DRAM $R_{TT,nom}$				
Write Leveling	**Output Buffers**	**$R_{TT,nom}$ Value**	**DRAM ODT Ball**	**DQS**	**DQ**	**DRAM State**	**Case**	**Notes**
Disabled	See normal operations					Write leveling not enabled	0	
Enabled (1)	Disabled (1)	n/a	Low	Off	Off	DQS not receiving: not terminated Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	1	2
		20Ω, 30Ω, 40Ω, 60Ω, or 120Ω	High	On		DQS not receiving: terminated by R_{TT} Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	2	
	Enabled (0)	n/a	Low	Off		DQS receiving: not terminated Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	3	3
		40Ω, 60Ω, or 120Ω	High	On		DQS receiving: terminated by R_{TT} Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	4	

Notes: 1. Expected usage if used during write leveling: Case 1 may be used when DRAM are on a dual-rank module and on the rank not being leveled or on any rank of a module not being leveled on a multislot system. Case 2 may be used when DRAM are on any rank of a module not being leveled on a multislot system. Case 3 is generally not used. Case 4 is generally used when DRAM are on the rank that is being leveled.

2. Since the DRAM DQS is not being driven (MR1[12] = 1), DQS ignores the input strobe, and all $R_{TT,nom}$ values are allowed. This simulates a normal standby state to DQS.
3. Since the DRAM DQS is being driven (MR1[12] = 0), DQS captures the input strobe, and only some $R_{TT,nom}$ values are allowed. This simulates a normal write state to DQS.

Write Leveling Procedure

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5, and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller.

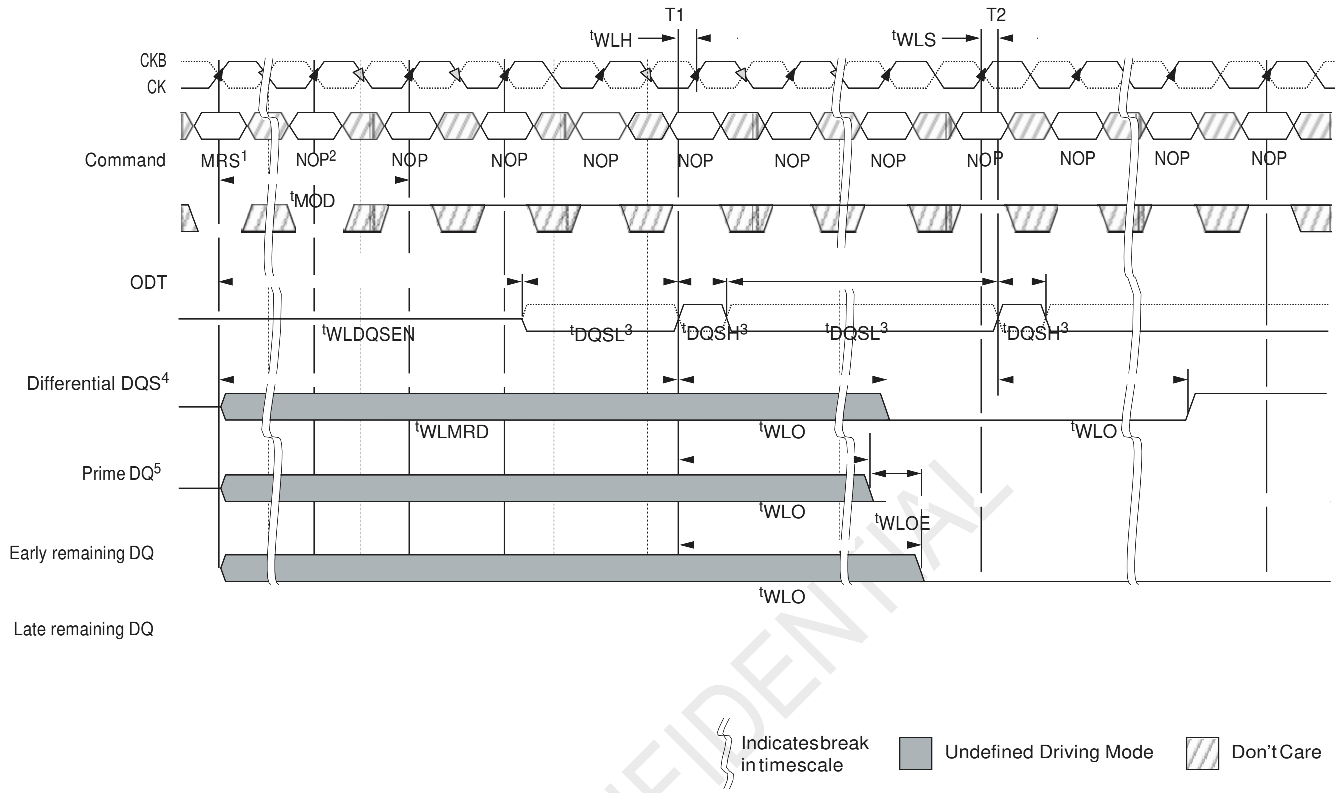
tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after tWLO timing. Either one or all data bits ("prime DQ bit(s)") provide the leveling feedback. The DRAM's remaining DQ bits are driven Low statically after the first sampling procedure.

There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Following describes the timing diagram and

parameters for the overall Write Leveling procedure

Write Leveling Sequence



Notes: 1. MRS: Load MR1 to enter write leveling mode.

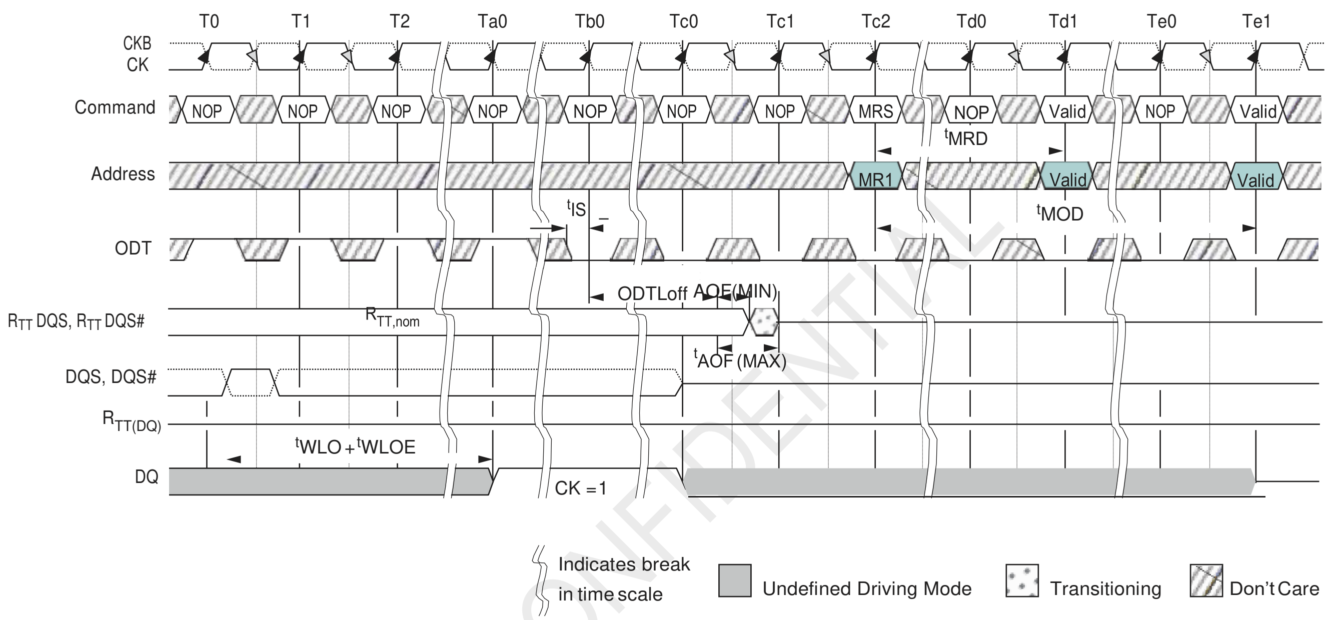
2. NOP: NOP or DES.
3. DQS, DQS# needs to fulfill minimum pulse width requirements ^{t}DQSH (MIN) and ^{t}DQSL (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
5. DRAM drives leveling feedback on a prime DQ (DQ0 for x4 and x8). The remaining DQ are driven LOW and remain in this state throughout the leveling procedure.

Write Leveling Mode Exit Procedure

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

Write Leveling Exit Procedure



Note: 1. The DQ result, = 1, between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

Initialization

The following sequence is required for power-up and initialization, as shown ;

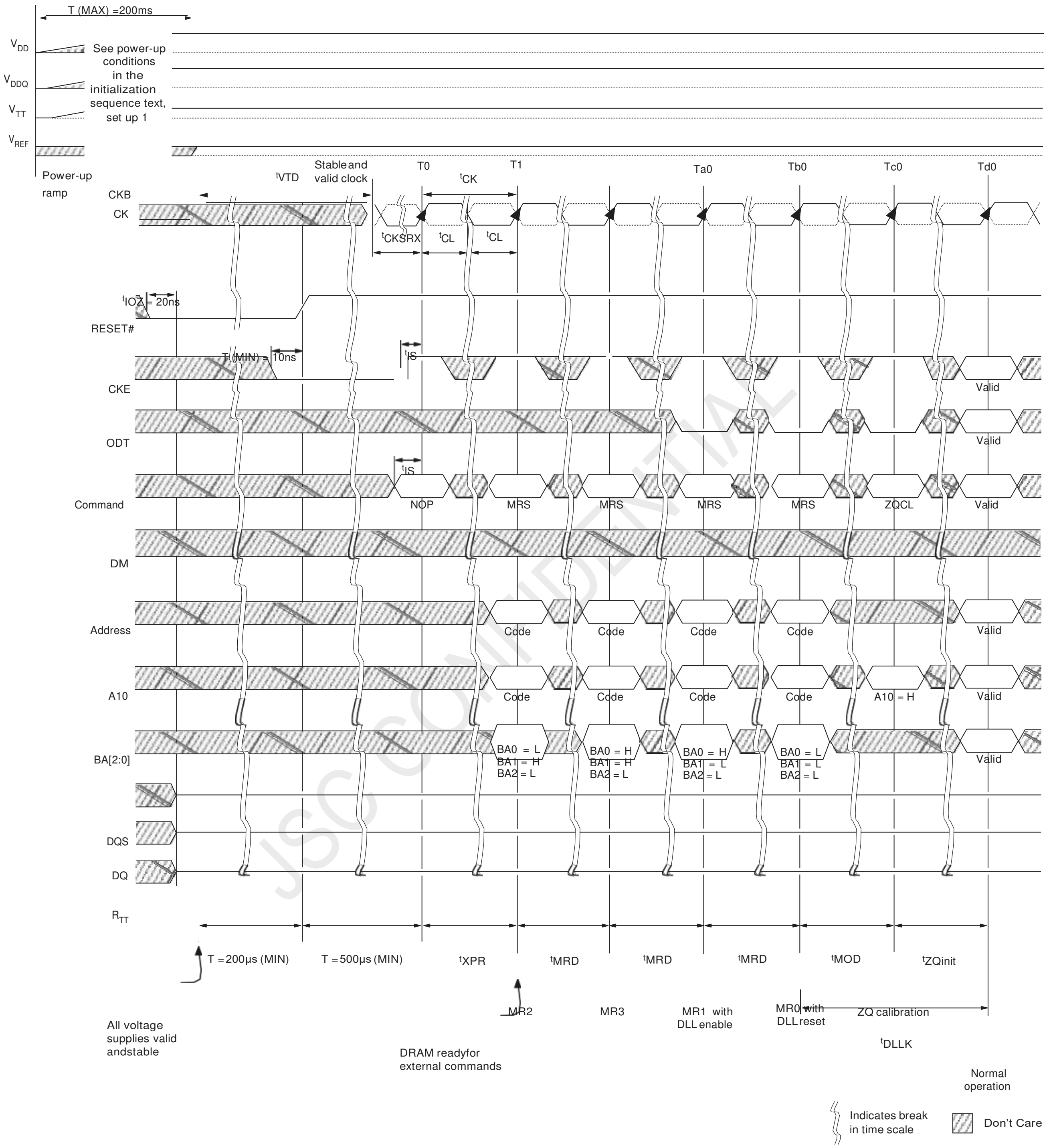
1. Apply power. RESET# is recommended to be below $0.2 \times V_{DDQ}$ during power ramp toensuretheoutputsremaindisabled(High-Z) andODToff(R_{TT} isalso High-Z). All other inputs, including ODT, may be undefined.

During power-up, either of the following conditions may exist and must be met:

- Condition A:
  - V_{DD} and V_{DDQ} are driven from a single-power converter output and are ramped with a maximum delta voltage between them of $\Delta V \leq 300mV$. Slope reversal of any power supply signal is allowed. The voltage levels on all ball so the rathanV_{DD},V_{DDQ},V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side,and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
  - Both V_{DD} and V_{DDQ} power supplies ramp to $V_{DD,min}$ and $V_{DDQ,min}$ within $^{t}V_{DDPR}$ = 200ms.
  - V_{REFDQ} tracks $V_{DD} \times 0.5$,V_{REFCA} tracks$V_{DD} \times 0.5$.
  - V_{TT} is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however,^{t}VTD should be greater than or equal to 0 to avoid device latch up.
- Condition B:
  - V_{DD} may be applied before or at the same time as V_{DDQ}.
  - V_{DDQ} may be applied before or at the same time asV_{TT}, V_{REFDQ},and V_{REFCA}.
  - No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200μs to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.
3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.
4. After RESET# transitions HIGH, wait 500μs (minus one clock) with CKE LOW.
5. After the CKE LOW time,CKE may be brought HIGH(synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns(and a minimum offive clocks) and ODT must be driven LOW at least
   ^{t}ISprior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
6. After CKE is registered HIGH and after ^{t}XPR has been satisfied, MRS commands maybe issued. Issue an MRS(LOADMODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
7. Issue an MRS command to MR3 with the applicable settings.
8. Issue an MRS command to MR1 with the applicable settings,including enabling the DLL and configuring ODT.
9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. ^{t}DLLK (512) cycles of clock input are required to lock the DLL.
10. Issue a ZQCL command to calibrate R_{TT} and R_{ON} values for the process voltage temperature (PVT). Prior to normal operation, ^{t}ZQinit must be satisfied.
11. When ^{t}DLLK and ^{t}ZQinit have been satisfied, the DDR3 SDRAM will be ready for normal operation.

Initialization Sequence



Voltage Initialization / Change

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided the following conditions are met:

- Just prior to increasing the 1.35V operating voltages, no further commands areissued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPsorCOMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

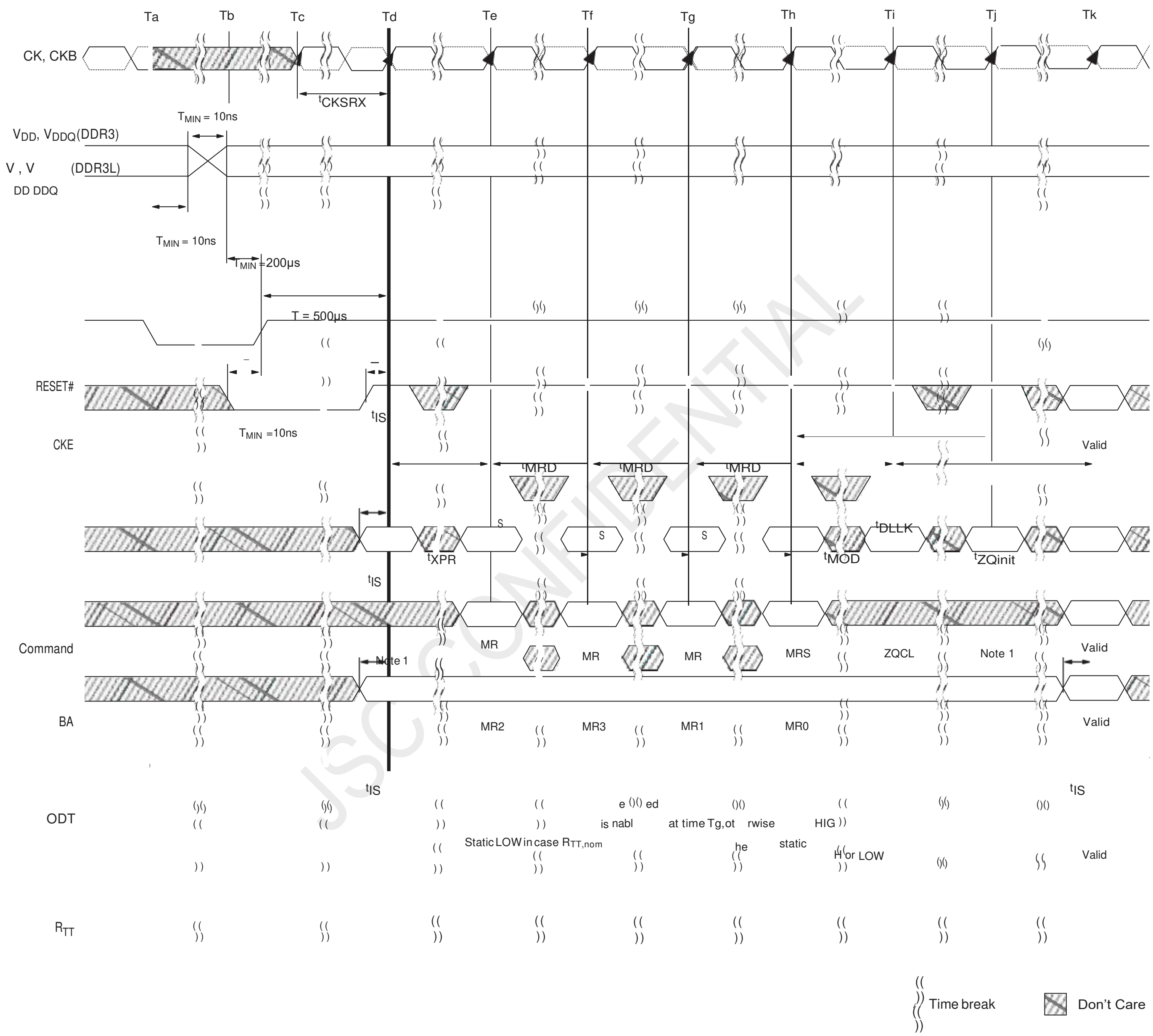
If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage canbe reduced to the 1.35V operation range provided the following conditions are met :

- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPsorCOMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

V_{DD} Voltage Switching

After the DDR3L DRAM is powered up and initialized, the power supply can be altered between the DR3Land DDR3 levels, provided the sequence in is maintained.

V_{DD} Voltage Switching



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

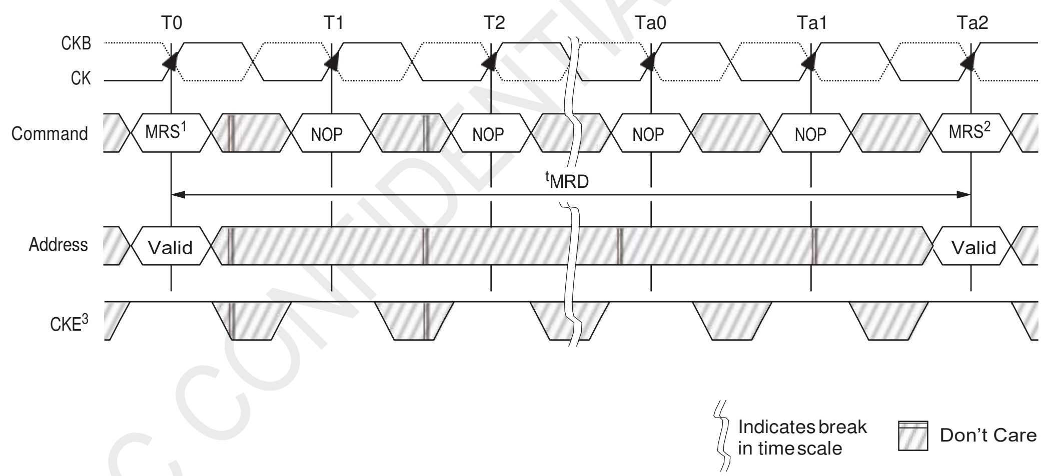
Mode Registers

Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3SDRAM. A mode register is programmed via the mode register set (MRS) command during initialization, and it retains the stored information (except for MR0[8], which is self-clearing) until it is reprogrammed, RESET# goes LOW, the device loses power.

Contents of a mode register can be altered by reexecuting the MRS command. Even if the user wants to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued(or re-issued) when all banks are idle and in the precharged state (^tRP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: ^tMRD and ^tMOD. The controller must wait ^tMRD before initiating any subsequent MRS commands.

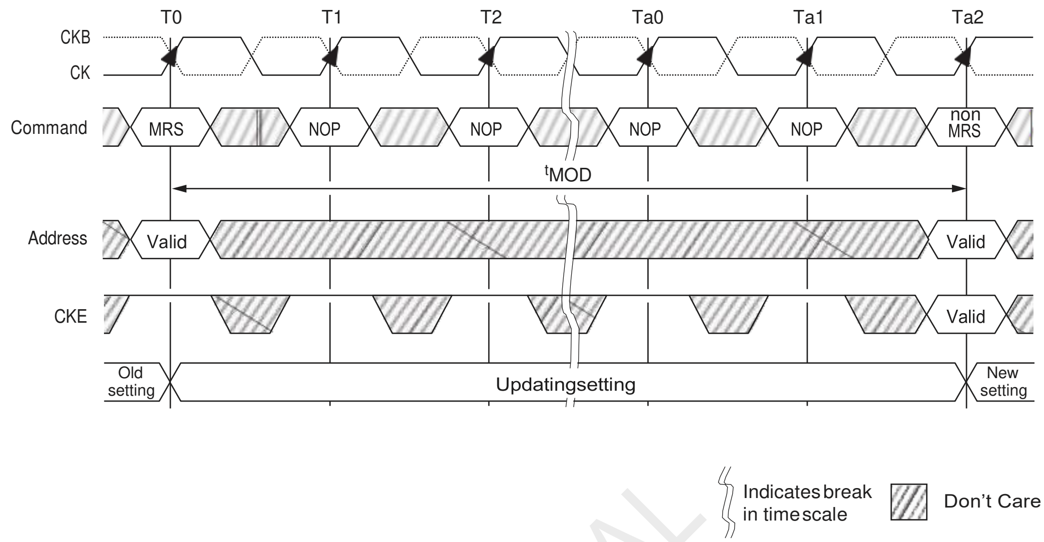
MRS to MRS Command Timing (^tMRD)



Notes: 1. Prior to issuing the MRS command, all banks must be idle and precharged, ^tRP (MIN) must be satisfied, and no data bursts can be in progress.
2. ^tMRD specifies the MRS to MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until $^tMRSPDEN$ (MIN) (see Power-Down Mode).
4. For a CAS latency change, ^tXPDLL timing must be met before any non-MRS command.

The controller must also wait ^tMOD before initiating any non-MRS commands (excluding NOP and DES). The DRAM requires ^tMOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until ^tMOD has been satisfied, the updated features are to be assumed unavailable.

MRS to nonMRS Command Timing (^{t}MOD)



Notes: 1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, ^{t}RP must be satisfied, and no data bursts can be in progress).

2. Prior to Ta2when ^{t}MOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If R_{TT} was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until ^{t}MODmin is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until ^{t}MRSPDEN (MIN), at which time power-down may occur (see Power-Down Mode.

Mode Register 0 (MR0)

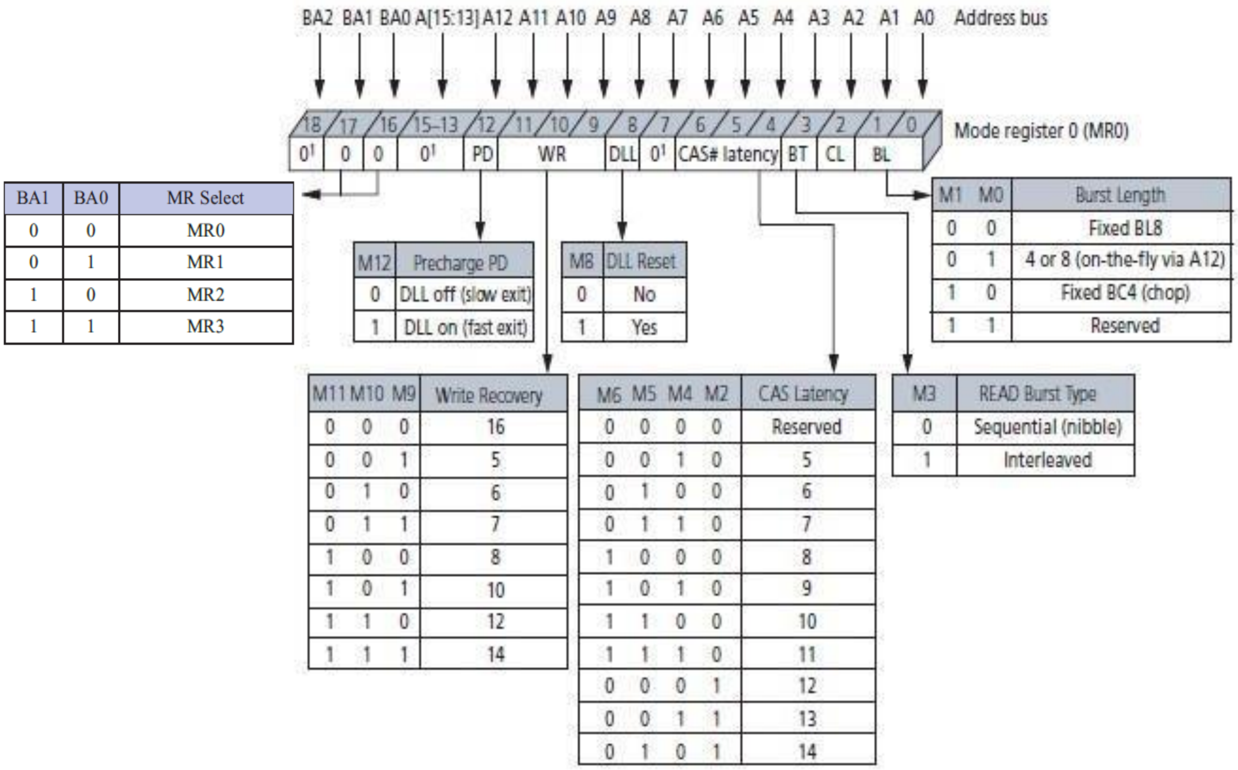
The base register, mode register 0 (MR0), is used to define various DDR3 SDRAM modes of operation. These definitions include the selection of a burst length,burst type,CAS latency, operating mode, DLL RESET, write recovery, and pre charge power-down mode.

Burst Length

Burst length is defined by MR0[1:0]. Read and write accesses to the DDR3 SDRAM are burst-oriented,with the burst length being programmable to 4(chop) mode,8(fixed) mode, or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to 01 during a READ/WRITE command,if A12=0, then BC4 mode is selected. If A12=1, then BL8 mode is selected. Specific timing diagrams, and turn around between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[*i*:2] when the burst length is set to 4 and by A[*i*:3] when the burst length is set to 8,where A*i* is the most significant column address bit for a given configuration. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Mode Register 0 (MR0) Definitions



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

M12	Precharge PD
0	DLL off (slow exit)
1	DLL on (fast exit)

M8	DLL Reset
0	No
1	Yes

M1	M0	Burst Length
0	0	Fixed BL8
0	1	4 or 8 (on-the-fly via A12)
1	0	Fixed BC4 (chop)
1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

M6	M5	M4	M2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

M3	READ Burst Type
0	Sequential (nibble)
1	Interleaved

Burst Type

Accesses with in a given burst can be programmed to either a sequential or aninter-leaved order. The burst type isselectedviaMR0[3].The ordering of accesses with in a burst is determined by the burst length, the burst type, and the starting column address. DDR3 only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word(BL8) boundaries.

Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4 (chop)	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8 (fixed)	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

Notes: 1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tri-state.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = “Don’t Care.”

DLL RESET

DLL RESET is defined by MR0[8]. Programming MR0[8] to 1 activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated.

Anytime the DLLRESET function is initiated, CKE must be HIGH and the clock held stable for 512(^{t}DLLK) clock cycles before a READ command can be issued.This is to allow time for the internal clock to be synchronized with the external clock. Failingto wait for synchronization can result in invalid output timing specifications, such as ^{t}DQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9]. Write recovery values of 5, 6, 7, 8, 10, or 12 can be used by programming MR0[11:9]. The user is required to program the correct value of write recovery, which is calculated by dividing ^tWR(ns) by ^tCK(ns) and rounding up a non integer value to the next integer:
WR (cycles) = roundup (^tWR (ns)/^tCK (ns)).

Precharge Power-Down (Precharge PD)

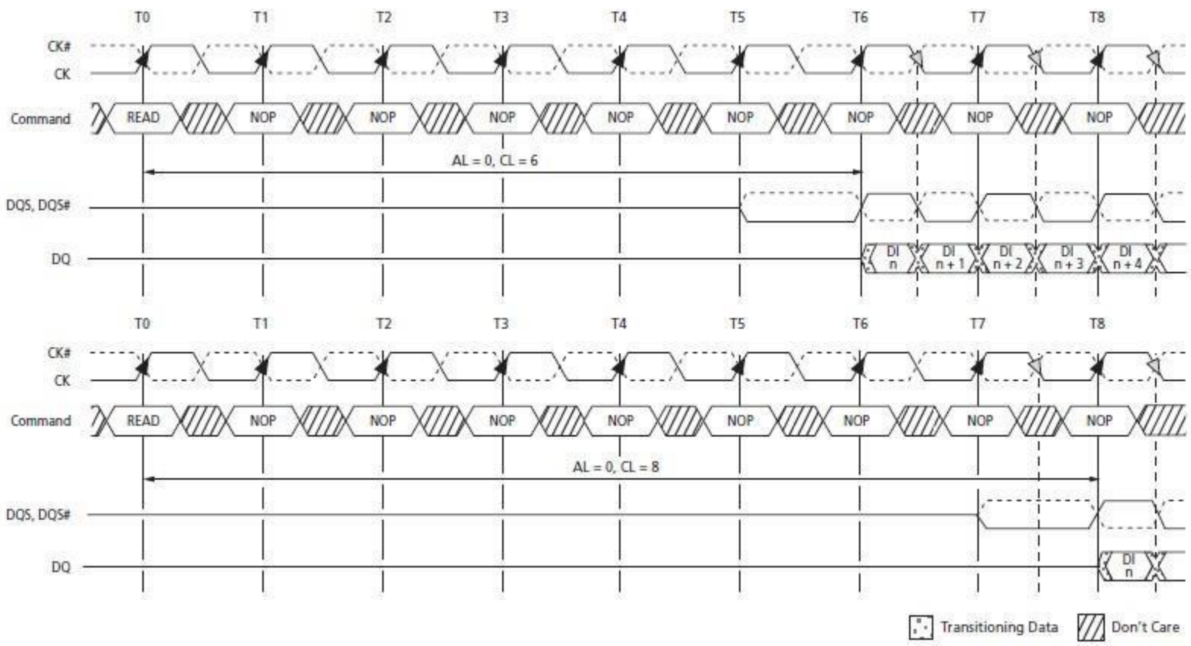
The precharge power-down (precharge PD) bit applies only when precharge power-down mode is being used. When MR0[12] is set to 0, the DLL is off during precharge power-down, providing a lower standby current mode; however, ^tXPDLL must be satisfied when exiting. When MR0[12] is set to 1 , the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode ; however, ^tXP must be satisfied when exiting (see Power-DownMode).

CAS Latency (CL)

CAS latency(CL) is defined by MR0[6:4], as shown. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. CL can be set to 5 through 14. DDR3SDRAM do not support half-clock latencies.

Examples of CL=6 and CL=8 are shown below. If an internal READ command is registered at clock edge *n*, and the CAS latency is *m* clocks, the data will be available nominally coincident with clock edge *n* +*m*. See Speed Bin Tables for the CLs supported at various operating frequencies.

READ Latency

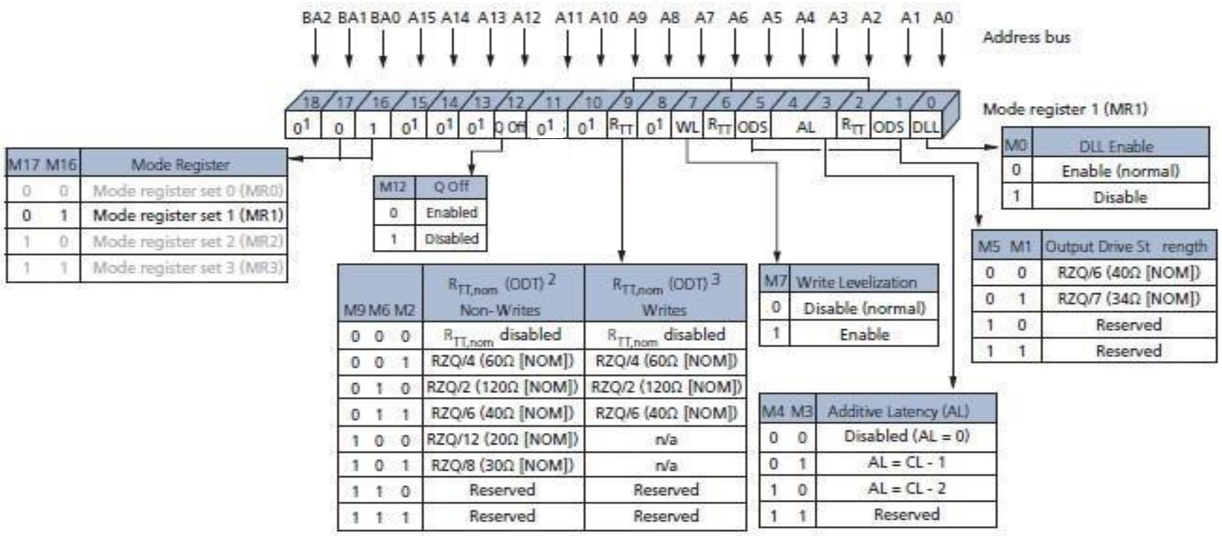


Notes: 1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
2. Shown with nominal ^{t}DQSCK and nominal ^{t}DSDQ.

Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nomimpedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to below table.

Mode Register 1 (MR1) Definition



Notes: 1. MR1[18, 15:13, 11, 10, 8] are reserved for future use and must be programmed to 0.
2. During write leveling, if MR1[7] and MR1[12] are 1, then all $R_{TT,nom}$ values are available for use.
3. During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only $R_{TT,nom}$ write values are available for use.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode”.
The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.
The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

Output Drive Strength

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3SDRAM devices.To calibrate the output drive rimpedance, an external precision resistor(RZQ) is connected between the ZQ ball and V_{SSQ}. The value of the resistor must be 240Ω ±1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all datasheet timing sand current specifica- tions are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up,the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined byMR1[12],as shown. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation.When disabled (MR1[12] =1),all DDR3SDRAM outputs (DQ and DQS, DQS#) are tristated. The output disable feature is intended to be used during I_{DD} characterization of the READ current and during ^{t}DQSS margining (write leveling) only.

On-Die Termination

ODT resistance $R_{TT,nom}$ is defined byMR1[9,6,2]. The R_{TT} termination value applies to the DQ, DM, DQS, DQS# balls. DDR3 supports multiple R_{TT} termination values based on RZQ/n where n canbe2, 4,6, 8,or 12 and RZQ is 240Ω.

Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. $R_{TT,nom}$ termination is allowed anytime after the DRAM is initialized, calibrated, and not performing read access, or when it is not in selfrefresh mode.
Additionally, write accesses with dynamic ODT ($R_{TT(WR)}$) enabled temporarily replaces $R_{TT,nom}$ with $R_{TT(WR)}$.

The actual effective termination, $R_{TT(EFF)}$, maybe different from the R_{TT} targeted due to non linearity of the termination. For $R_{TT(EFF)}$ values and calculations (see On-Die Termi- nation(ODT).

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on / off ODT for any or all devices. The ODT input control pin is used to determine when R_{TT} is turned on(ODTLon) and off (ODTL off), assuming ODT has been enabled via MR1 [9,6,2].

Timings for ODT are detailed in On-Die Termination (ODT).

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown. Write leveling is used (during in itialization) to de skew the DQS strobe to clock off set as are sultofflyby topology designs. For better signal integrity, DDR3SDRAM memory modules adopted fly-bytopology for the commands, addresses, control signals, and clocks.

The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining ^{t}DQSS,^{t}DSS,and^{t}DSH specifications without supporting write leveling in systems which use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in Write Leveling.

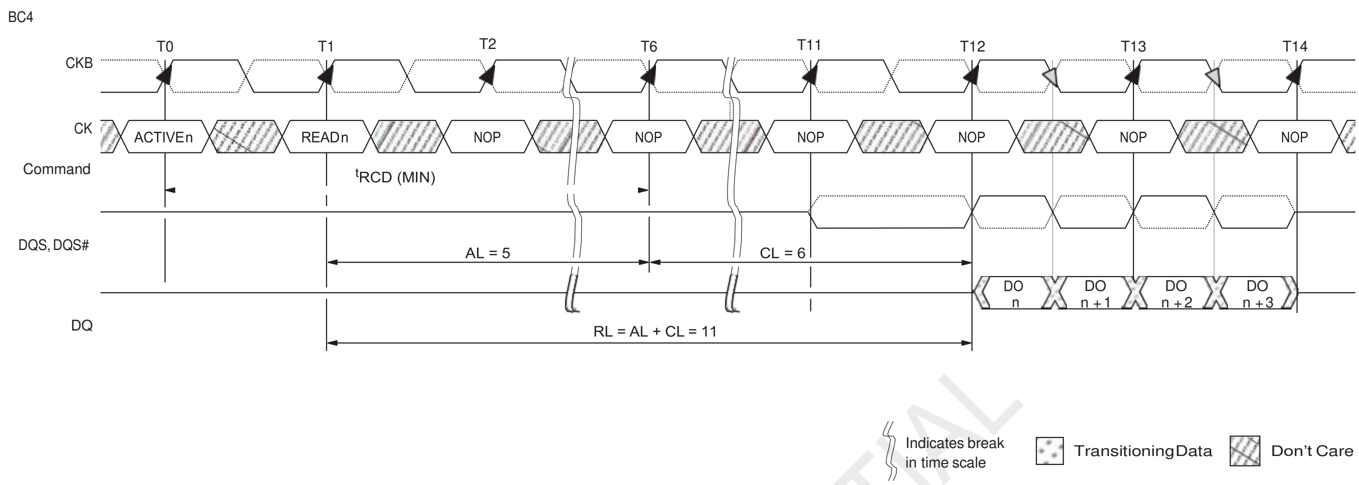
POSTED CAS ADDITIVE Latency

POSTEDCAS ADDITIVE latency(AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4,3] define the value of AL, as shown. MR1[4, 3] enable the user to program the DDR3 SDRAM with AL = 0, CL -1, or CL -2.

With this feature, the DDR3SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to ^{t}RCD(MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ ^{t}RCD(MIN) must be satisfied. Assuming ^{t}RCD (MIN)= CL, a typical application using this feature sets AL= CL- 1^{t}CK= ^{t}RCD(MIN) - 1 ^{t}CK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency(CL), RL=AL+CL. WRITE latency (WL) is the sum of CAS

WRITE latency and AL, WL= AL + CWL (see Mode Register2(MR2). Examples of READ and WRITE latencies are shown.

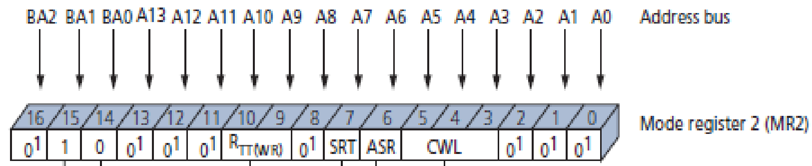
READ Latency (AL = 5, CL = 6)



Mode Register 2 (MR2)

The mode register2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH(ASR), SELF REFRESH TEMPERATURE(SRT), and DYNAMIC ODT ($R_{TT(WR)}$). These functionsare controlledviathe bits shown. The MR2 is programmed vi athe MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

Mode Register 2 (MR2) Definition



M15	M14	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (0°C to 95°C)

M5	M4	M3	CAS Write Latency (CWL)
0	0	0	5 CK ($^tCK \geq 2.5ns$)
0	0	1	6 CK ($2.5ns > {}^tCK \geq 1.875ns$)
0	1	0	7 CK ($1.875ns > {}^tCK \geq 1.5ns$)
0	1	1	8 CK ($1.5ns > {}^tCK \geq 1.25ns$)
1	0	0	9 CK ($1.25ns > {}^tCK \geq 1.07ns$)
1	0	1	10 CK ($1.07ns > {}^tCK \geq 0.938ns$)
1	1	0	Reserved
1	1	1	Reserved

M10	M9	Dynamic ODT ($R_{TT(WR)}$)
0	0	$R_{TT(WR)}$ disabled
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

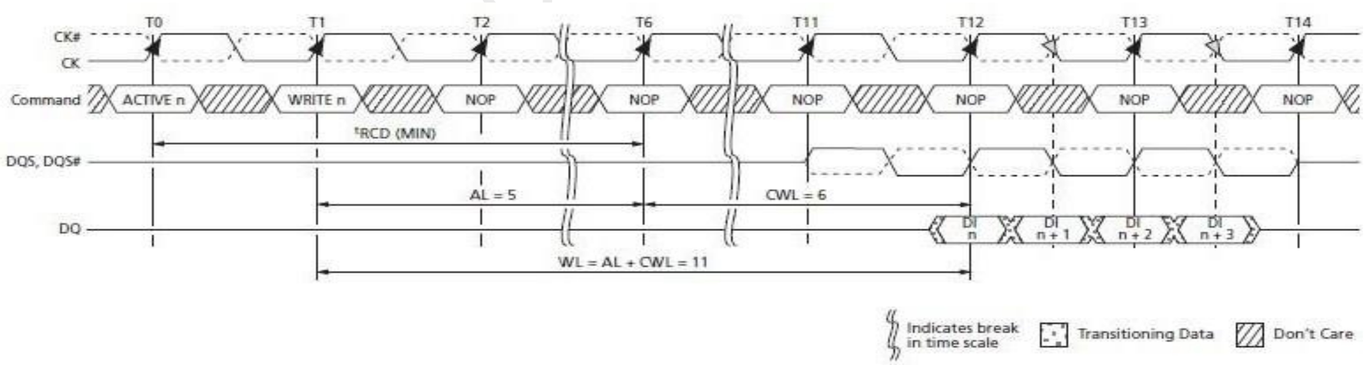
M6	Auto Self Refresh
0	Disabled: Manual
1	Enabled: Automatic

Note: 1. MR2[18, 15:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

CAS WRITE Latency(CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in.CWL must be correctly set to the corresponding operating clock frequency. The overall WRITE latency(WL) is equal to CWL+AL.

CAS WRITE Latency



AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function. When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh unless the user enables the SRT feature listed below when the T_C is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1x to 2x when the case temperature exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if ASR is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage.

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the selfrefresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate).In the disabled mode, SRT requires the user toensure the DRAM neverexceeds a T_C of 85°C while in self refresh mode unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh cur rent specifications do not apply.

SRT vs. ASR

If the normal case temperature limit of 85°C is not exceeded, then neither SRT nor ASR is required, and both can be disabled through out operation. However,if the extended temperature option of 95°C is needed, the user is required to provide a2x refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2x rate.

SRT forces the DRAM to switch the internal self refresh rate from 1x to 2x. Self refresh is performed at the 2x refreshrate regardless of the casetemperature.

ASR automatically switches the DRAM's internal self refresh rate from 1x to 2x. However,while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1x to 2x over the supported temperature range. One other disadvantage with ASR is the DRAM cannot always switch from a1x to a 2x refresh rate at an exact case temperature of 85°C. Although the DRAM will support data integrity when it switches from a 1x to a 2x refresh rate, it may switch at a lower temperature than 85°C.

Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

DYNAMIC ODT

The dynamic ODT($R_{TT(WR)}$) feature is defined by MR2[10,9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination on-the-fly.

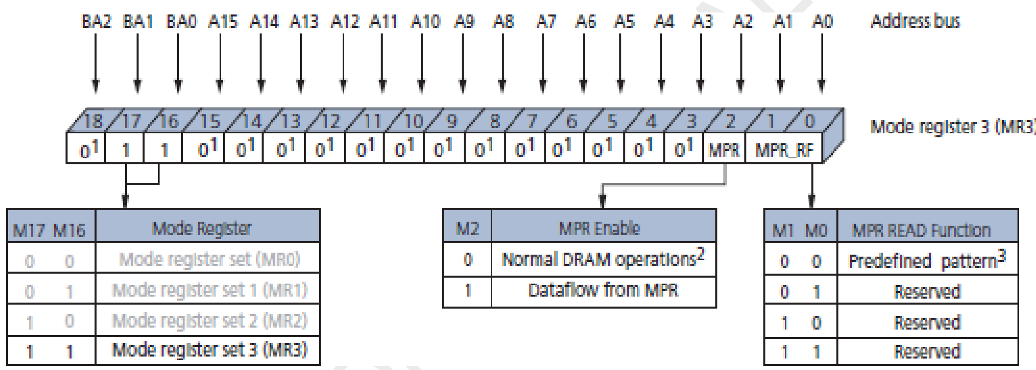
With dynamicODT($R_{TT(WR)}$) enabled, the DRAM switches from normal ODT ($R_{TT,nom}$) to dynamic ODT ($R_{TT(WR)}$) when beginning a WRITE burst and subsequently switches back to ODT($R_{TT,nom}$) at the completion of the WRITE burst. If $R_{TT,nom}$ is disabled, the $R_{TT,nom}$value will be High-Z. Special timing parameters must be adhered to when dynamic ODT ($R_{TT(WR)}$) is enabled: ODTLcnw, ODTLcnw4, ODTLcnw8, ODTH4, ODTH8, and ^{t}ADC.

Dynamic ODT is only applicable during WRITE cycles. If ODT ($R_{TT,nom}$) is disabled, dynamic ODT($R_{TT(WR)}$) is still permitted. $R_{TT,nom}$ and $R_{TT(WR)}$ can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state ofODT($R_{TT,nom}$). For detail on dynamic ODT operation, refer to Dynamic ODT.

Mode Register 3 (MR3)

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

Mode Register 3 (MR3) Definition



Notes: 1. MR3[18 and 15:3] are reserved for future use and must all be programmed to 0.
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will beignored.
3. Intended to be used for READ synchronization.

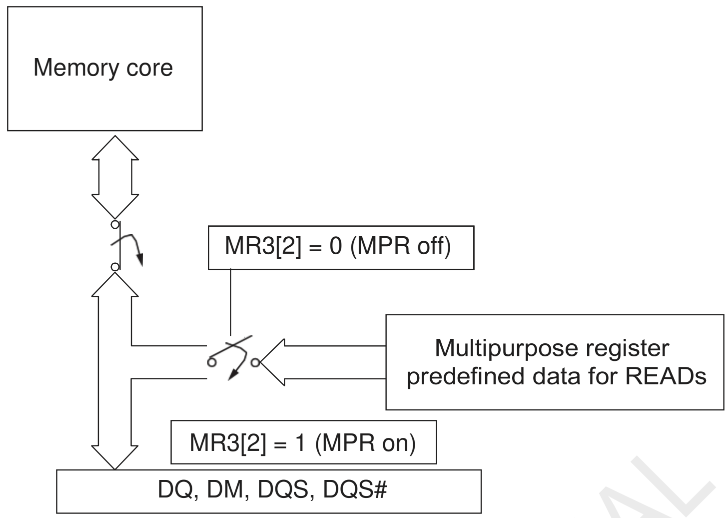
MULTIPURPOSE REGISTER (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register.

When the MPR is enabled, only RD or RDA commands are allowed until a subsequent

MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Multipurpose Register (MPR) Block Diagram



Notes: 1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	
MPR	MPR READ Function	Function
0	"Don't Care"	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array All subsequent WRITEs go to the DRAM memory array
1	A[1:0]	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

MPR Functional Description

The MPR JEDEC definition enables either a prime DQ (DQ0 on a x4 and a x8;on a x16, DQ0 = lower byte and DQ8 = upper byte) to out put the MPR data with the remaining DQs driven LOW,or for all DQ st out put the MPR data . The MPR read out supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] mustbe setto00asthe burst order is fixed pernibble
- A2 selects the burst order:
  - BL8, A2 is set to 0, and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7
- For burst chop 4 cases , the burst or deriss witched on the nibble base along with the following:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bi t0 (the firstbit) isassigned to LSB,and burst order bit7(thelastbit) is assigned to MSB
- A[9:3] area“Don’tCare”
- A10isa“Don’t Care”
- A11isa“Don’t Care”
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13isa“Don’t Care”
- BA[2:0] are a “Don’t Care”

MPR Register Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The pre defined pattern is always a repeating 0–1 bit pattern.

Examples of the different types of predefined READ pattern bursts are shown in the following .

MPR Readouts and Burst Order Bit Mapping

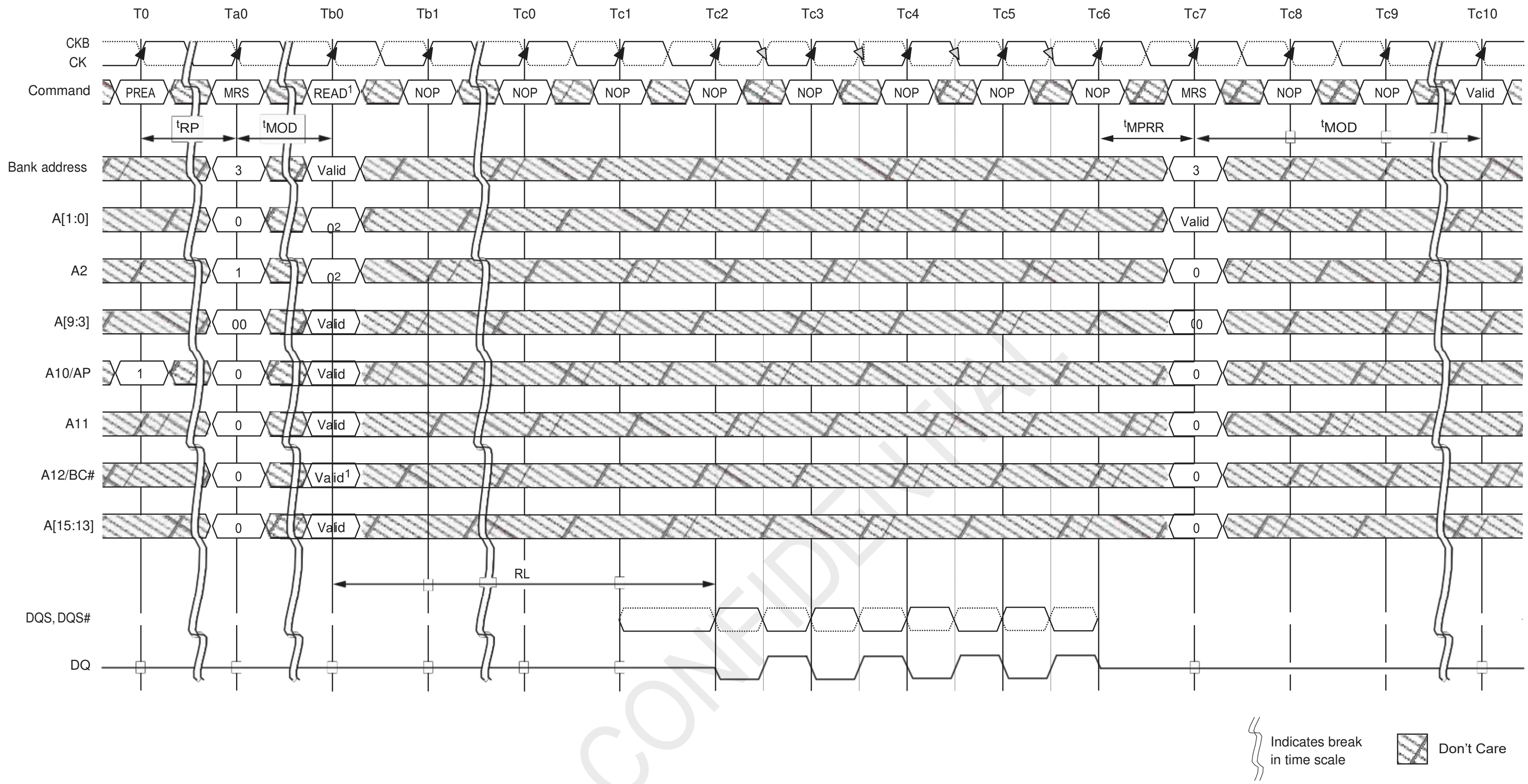
MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	00	READ predefined pattern for system calibration	BL8	000	Burst order: 0, 1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0, 1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A
1	10	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A

MPR Readouts and Burst Order Bit Mapping (Continued)

MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	11	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A

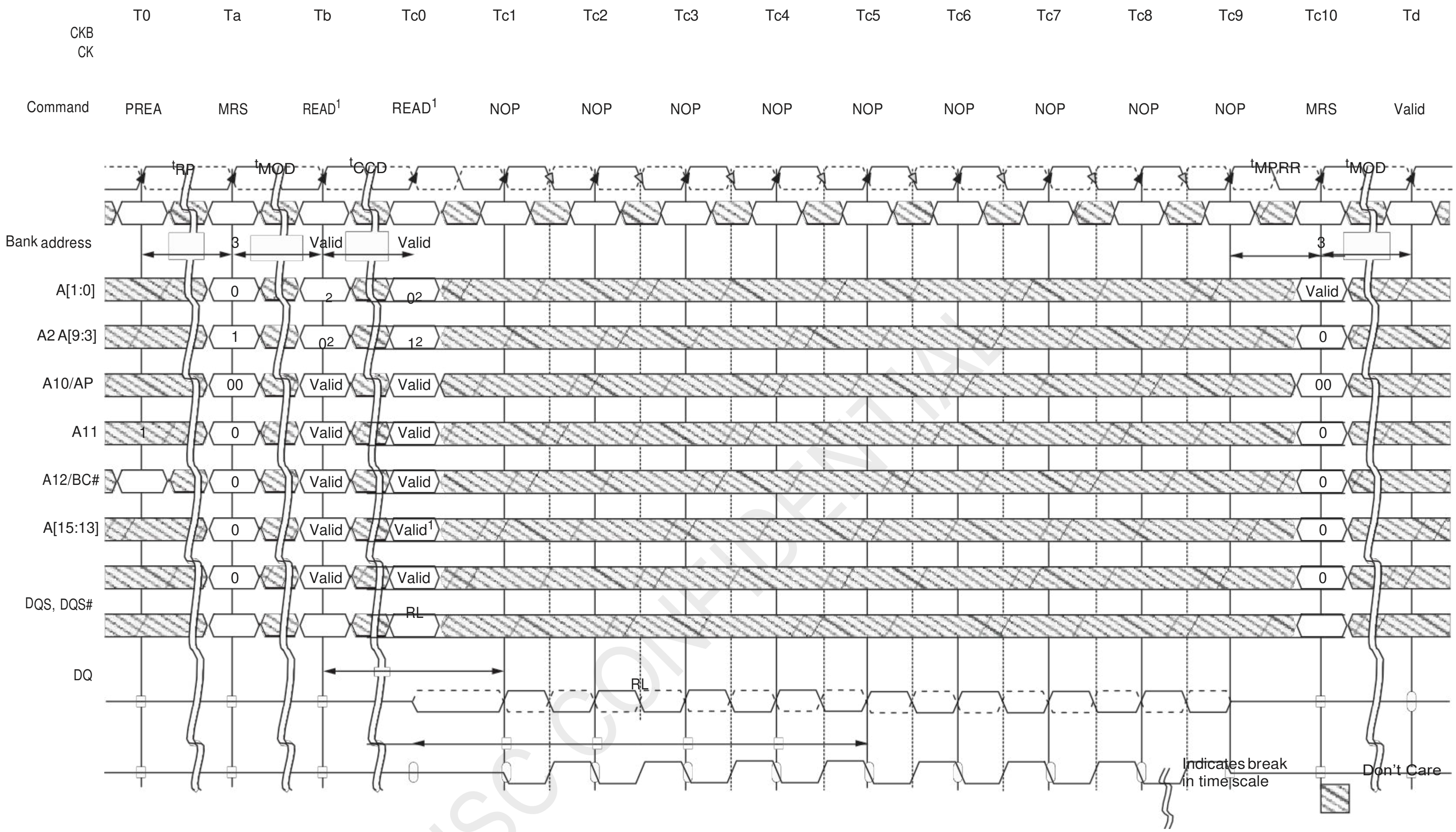
Note: 1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selec- ted MPR agent.

MPR System Read Calibration with BL8: Fixed Burst Order Single Readout



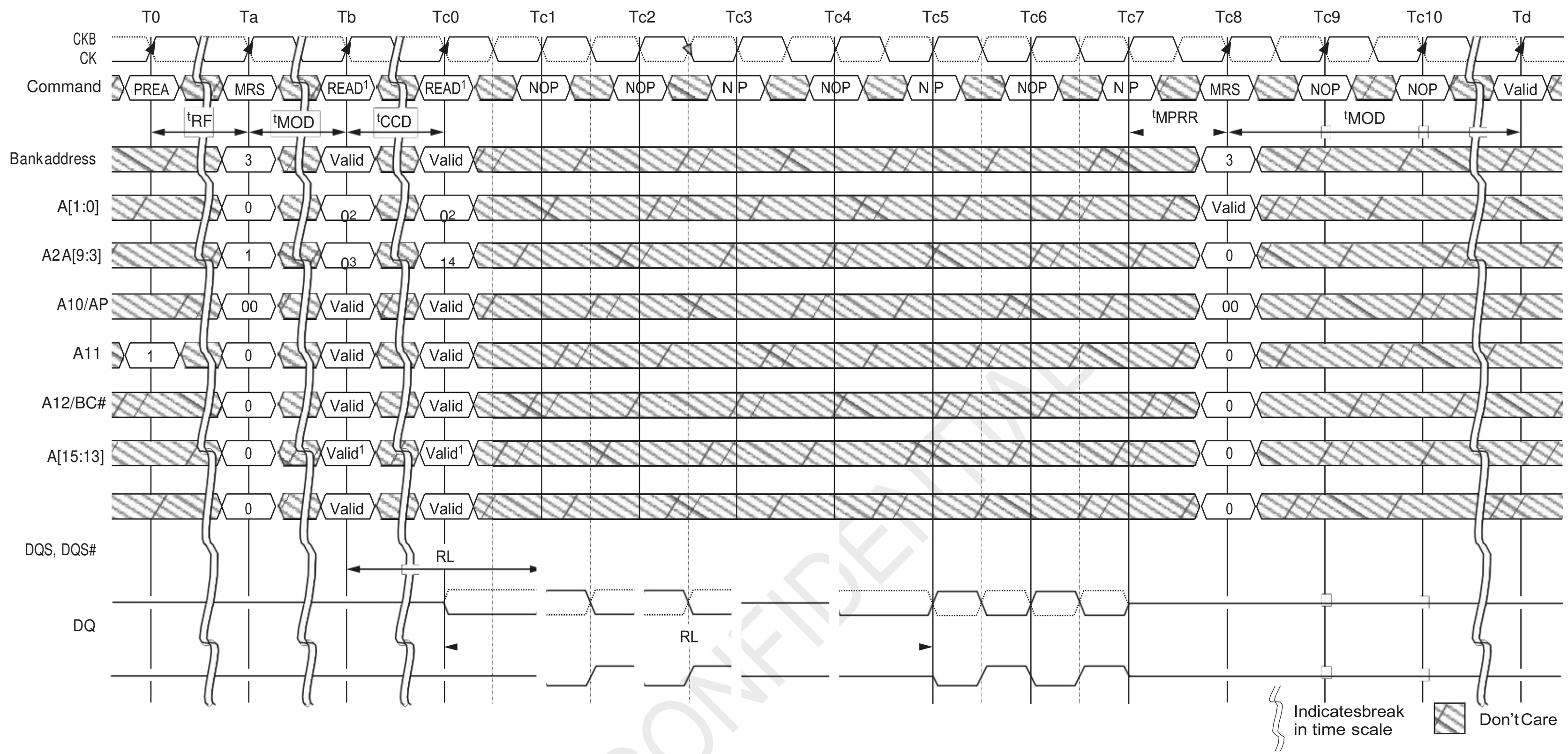
Notes: 1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 onA[2:0].

MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout



Notes: 1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 onA[2:0].

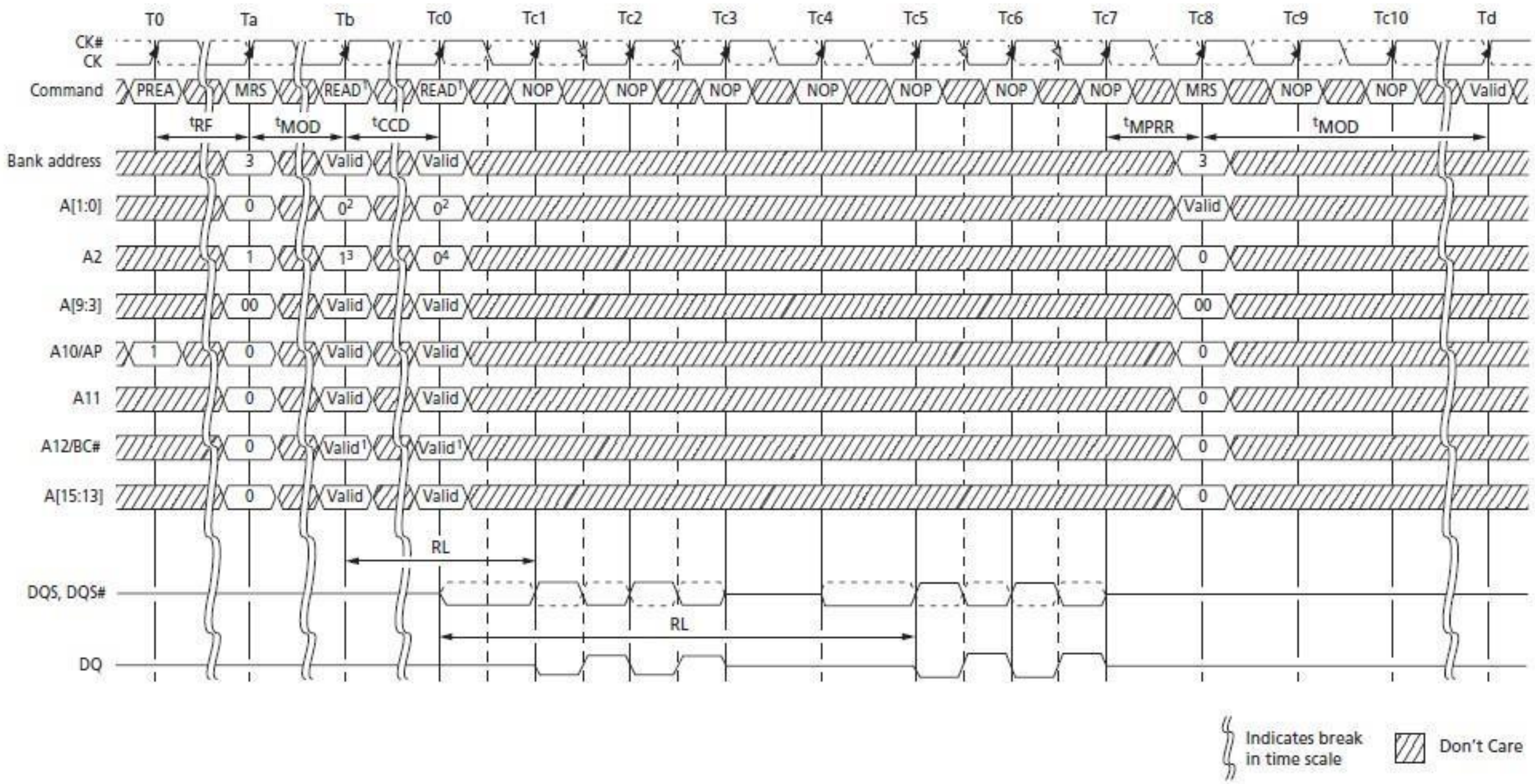
MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble



Notes: 1. READ with BC4 either by MRS or OTF.

2. Memory controller must drive 0 on A[1:0].
3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.
4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble



Notes: 1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

MPR Read Predefined Pattern

The pre determined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the read out pre determined read calibration pattern. The example is to perform multiple reads from the multipurpose register to do system level read timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the read calibration:

1. Precharge all banks
2. After ^{t}RP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all sub- sequentreadsandloadsthe pre defined pattern into the MPR. As soon as ^{t}MRD and ^{t}MOD are satisfied, the MPR is available
3. Data WRITE operations are not allowed until the MPR returns to the normal DRAM state
4. Issue a read with burst order information (all other address pins are "Don't Care"):
   - A[1:0] = 00 (data burst order is fixed starting at nibble)
   - A2=0(forBL8,burstorderisfixedas0,1,2,3,4,5,6,7)
   - A12 = 1 (use BL8)
5. After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (0,1,0,1,0,1,0,1)
6. The memory controller repeats the calibration reads until read data capture at memory controller is optimized
7. After the last MPR READ burst and after ^{t}MPRR has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] ="Don't Care" to thenormal DRAMstate. All subse- quent read and write accesses will be regular reads and writes from/to the DRAM array
8. When ^{t}MRD and ^{t}MOD are satisfied from the last MRS, the regular DRAM com- mands (such as activate a memory bank for regular read or write access) are per- mitted

MODE REGISTER SET (MRS) Command

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (orre-issued) when all banks are idle and in the precharged state (^{t}RP is satisfied and no data bursts are in progress). The controller must wait the specified time ^{t}MRD before initiating a subsequen to peration such as an ACTIVATE command . There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by ^{t}MOD. Both ^{t}MRD and ^{t}MOD parameters are shown. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION Operation

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the DRAM's ZQ ball to V_{SSQ}.

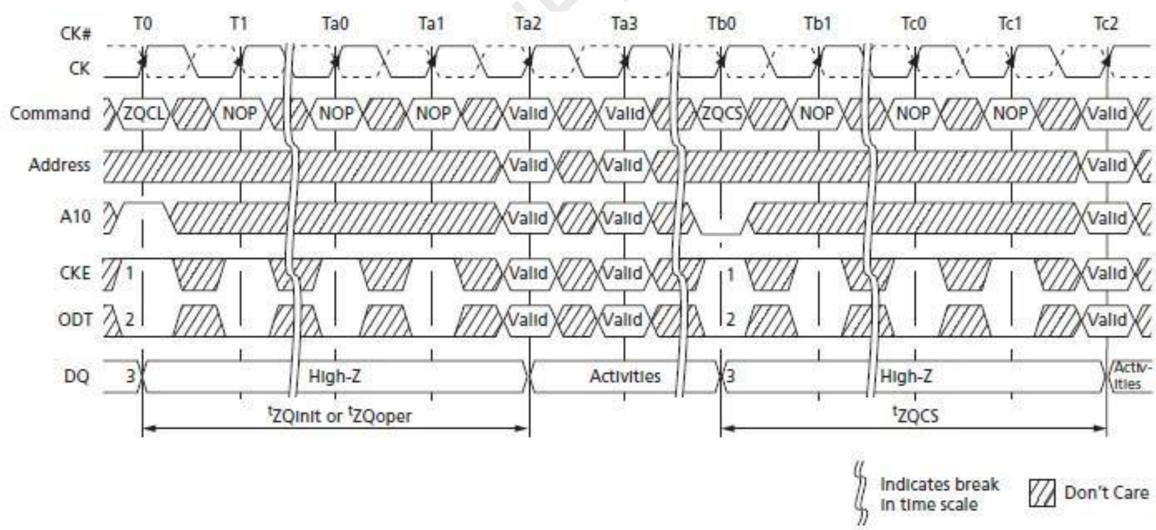
DDR3 SDRAM require a longer time to calibrate R_{ON} and ODT at power-up initialization and self refresh exit, and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQCL and ZQCS. An example of ZQ calibration timing is shown below.

All banks must be precharged and ^{t}RP must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than issuing another ZQCL or ZQCS command) can be performed on the DRAM channel by the controller for the duration of ^{t}ZQinit or ^{t}ZQoper. The quiet time on the DRAM channel helps accurately calibrate R_{ON} and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

In dual-rank systems that share the ZQ resistor between devices, the controller must not enable overlap of ^{t}ZQinit, ^{t}ZQoper, or ^{t}ZQCS between ranks.

ZQ CALIBRATION Timing (ZQCL and ZQCS)

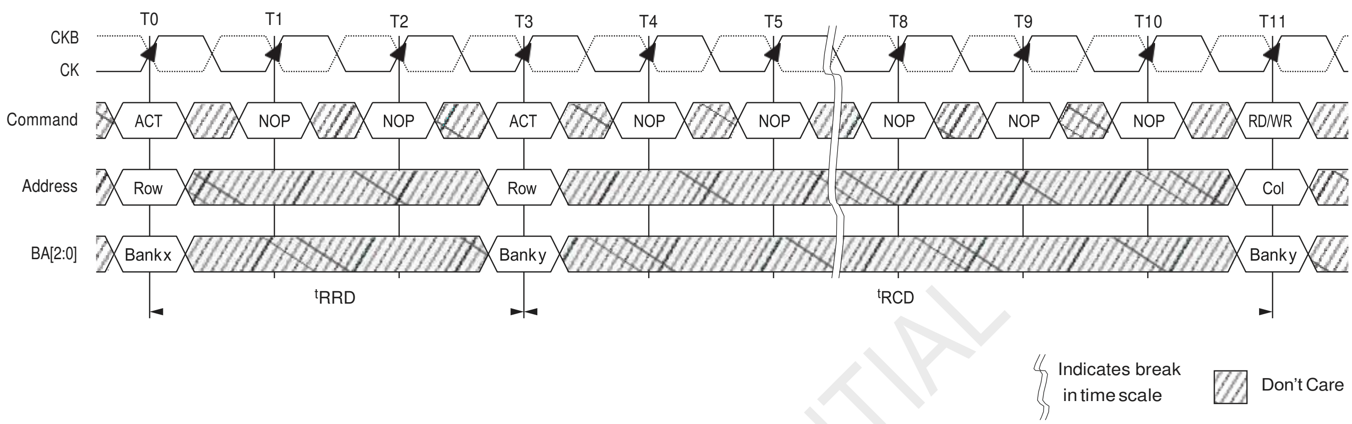


Notes:
1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

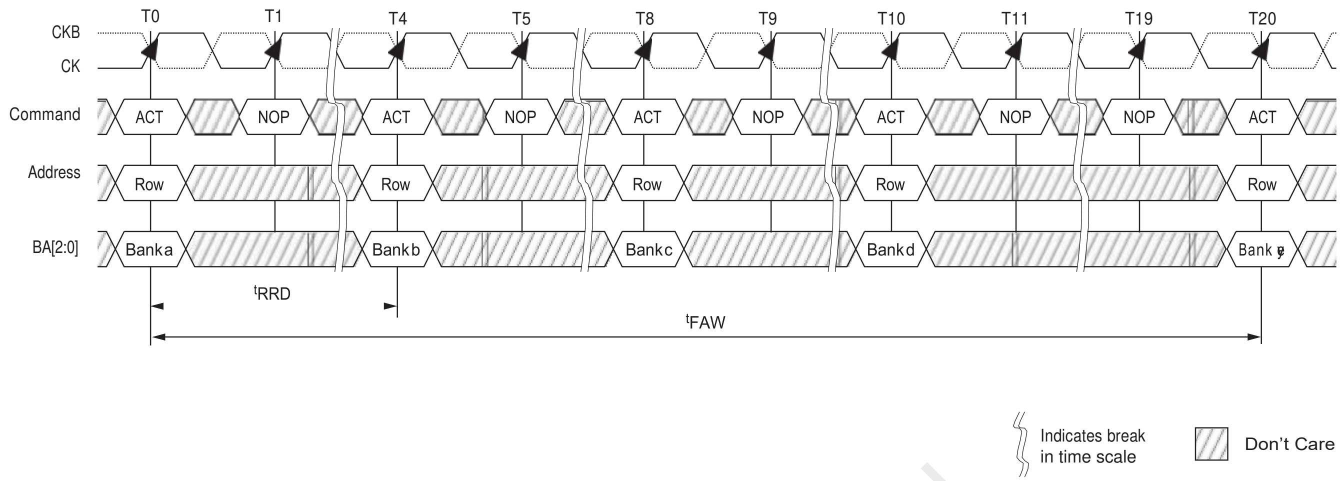
ACTIVATE Operation

Before any READ or WRITE commands canbe issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

Example: Meeting tRRD (MIN) and tRCD (MIN)



Example: tFAW

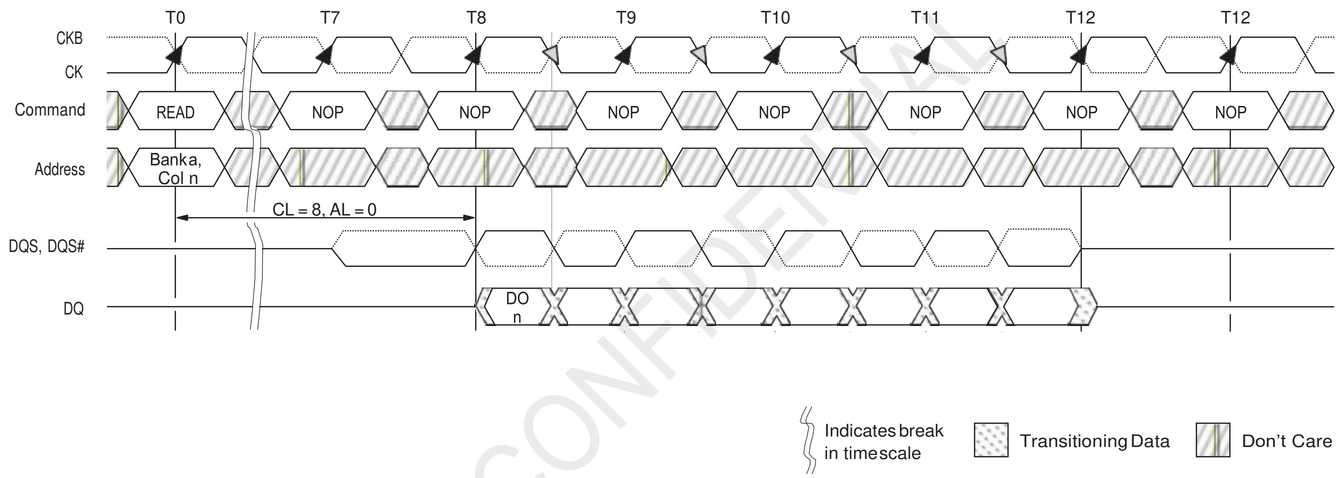


READ Operation

READ bursts are initiated with a READ command. The starting column and bankad-dresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled,the row being accessedis automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

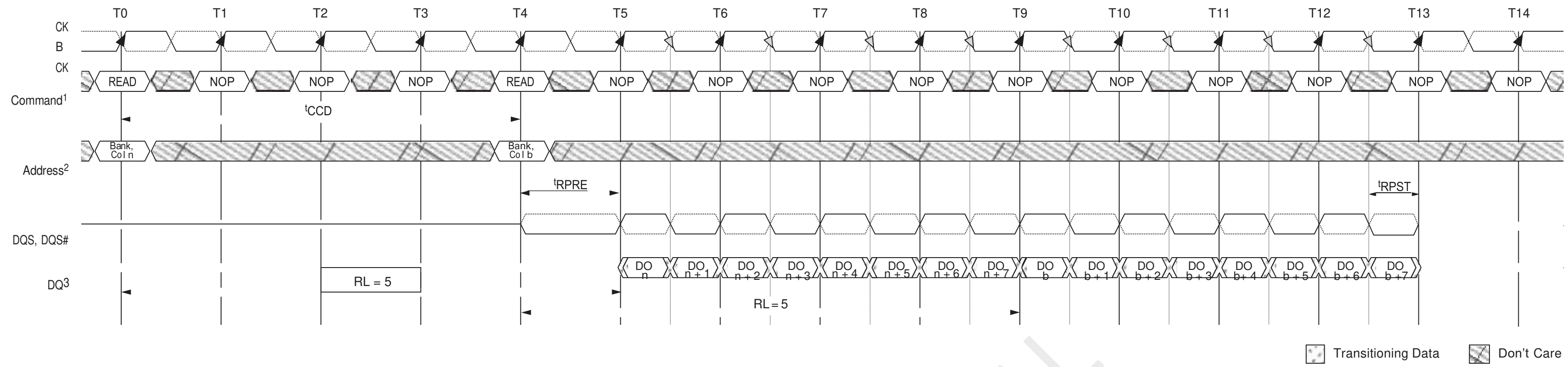
During READ bursts,the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of posted CAS additive latency(AL) andCAS latency(CL) (RL=AL+ CL). The value of AL and CL is programma-ble in the mode register via the MRS command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CKB). Shows an example of Rl based on a CL setting of 8 and an AL setting of 0.

READ Latency



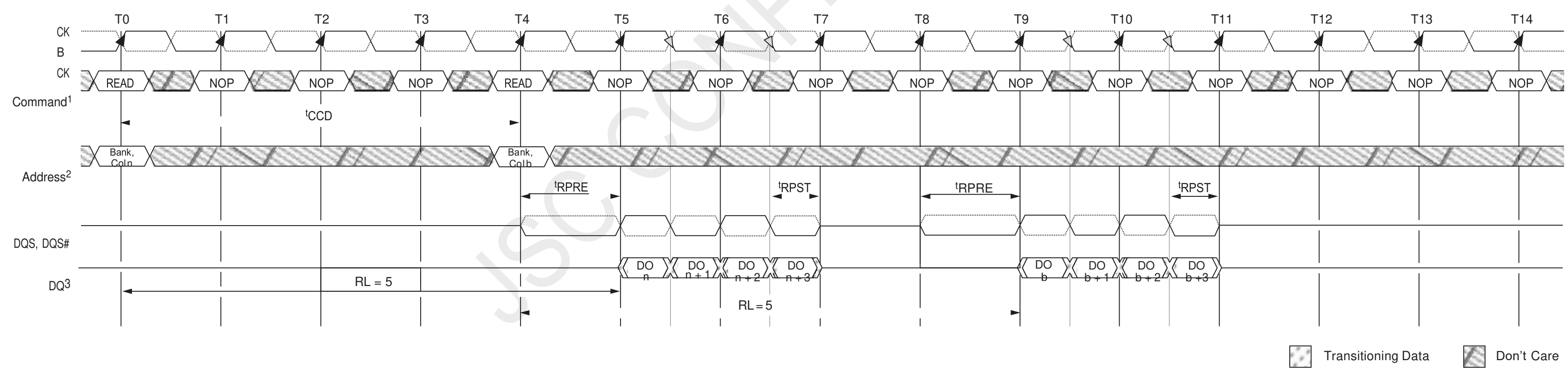
Notes: 1. DO *n* = data-out from column *n*.
2. Subsequent elements of data-out appear in the programmed order following DO *n*.

Consecutive READ Bursts (BL8)



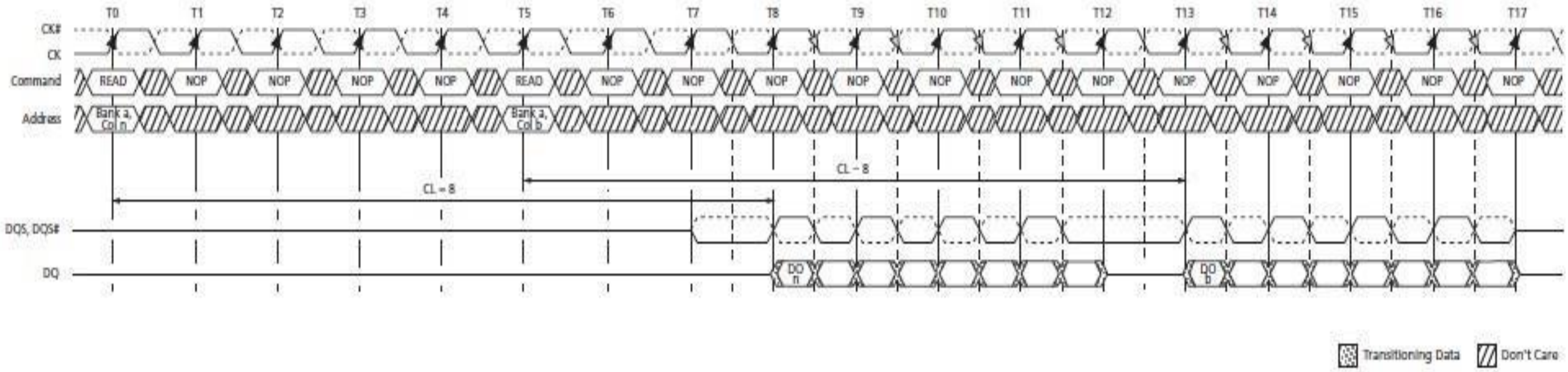
Notes: 1 . NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BL8, RL = 5 (CL = 5, AL= 0).

Consecutive READ Bursts (BC4)



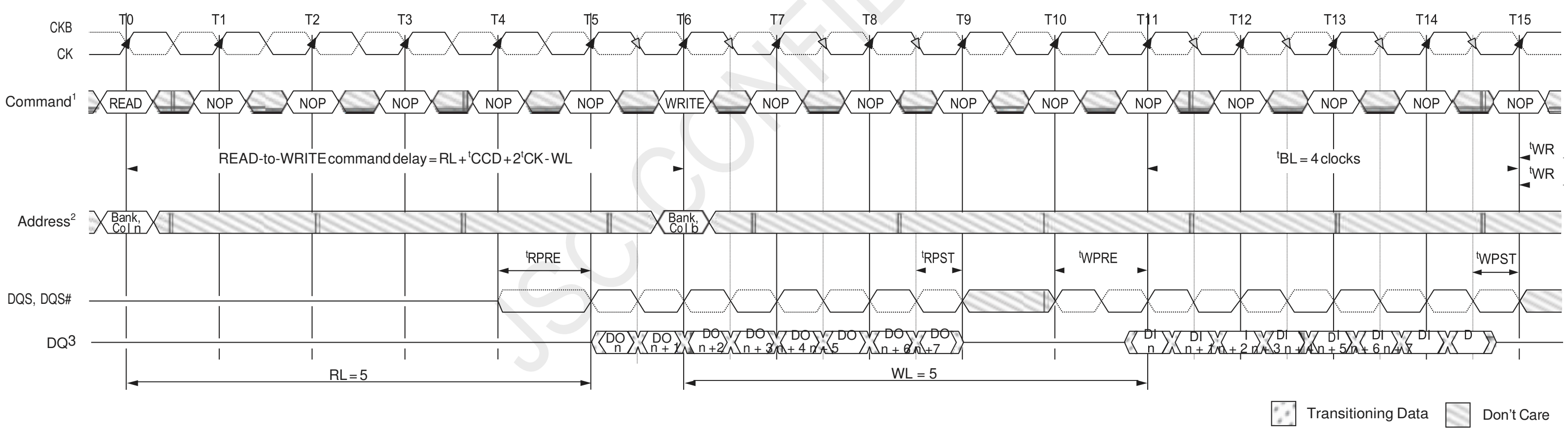
Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 setting is activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BC4, RL = 5 (CL = 5, AL = 0).

Nonconsecutive READ Bursts



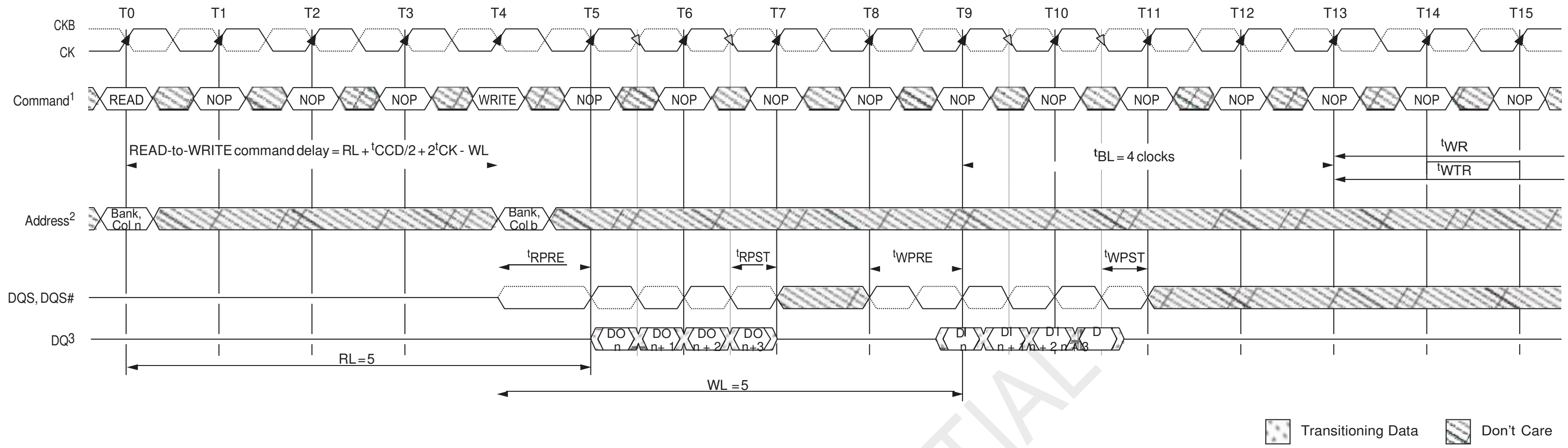
Notes: 1. AL = 0, RL = 8.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
4. Seven subsequent elements of data-out appear in the programmed order following DO *b*.

READ (BL8) to WRITE (BL8)



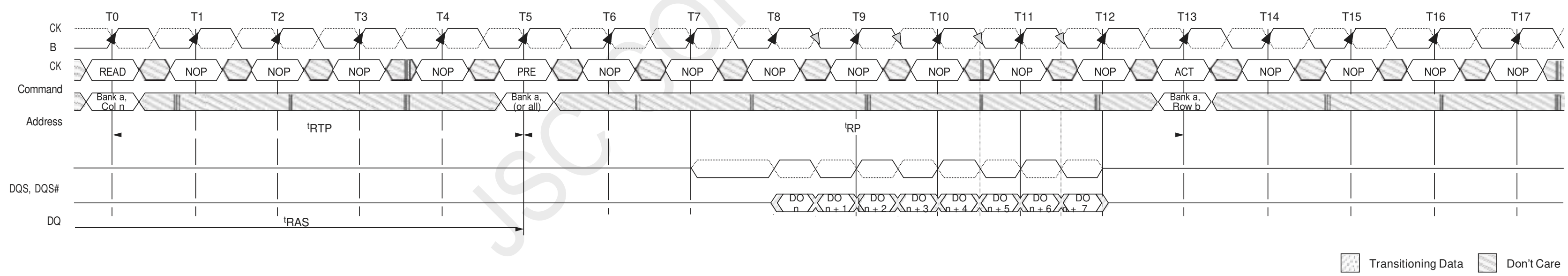
Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
3. DO *n* = data-out from column, DI *b* = data-in for column *b*.
4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

READ (BC4) to WRITE (BC4)OTF

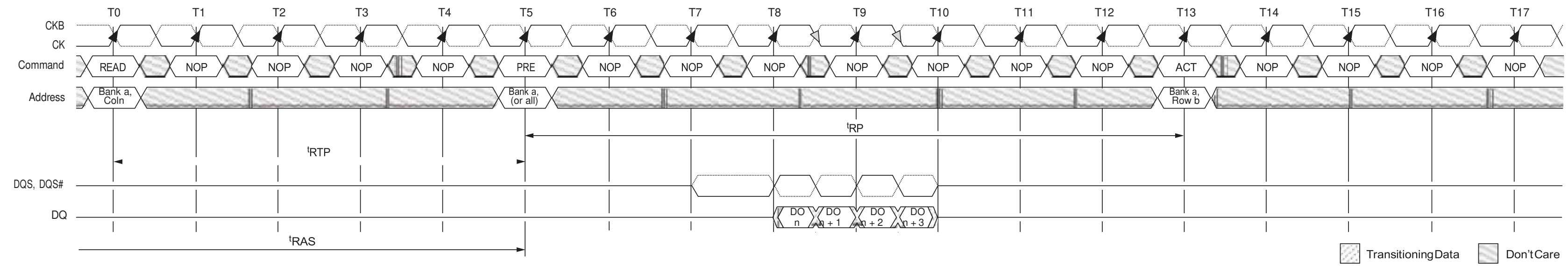


Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
3. DO *n* = data-out from column *n*; DI *n* = data-in from column *b*.
4. BC4, RL = 5 (AL - 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

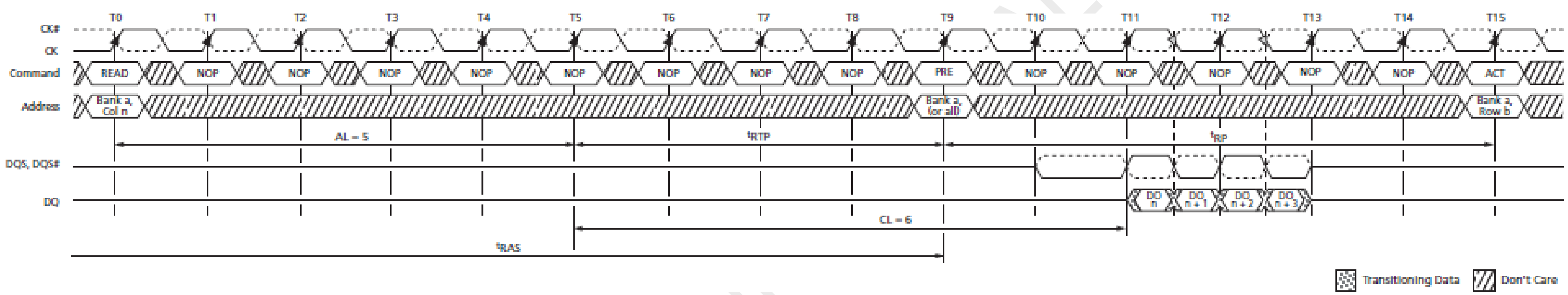
READ to PRECHARGE (BL8)



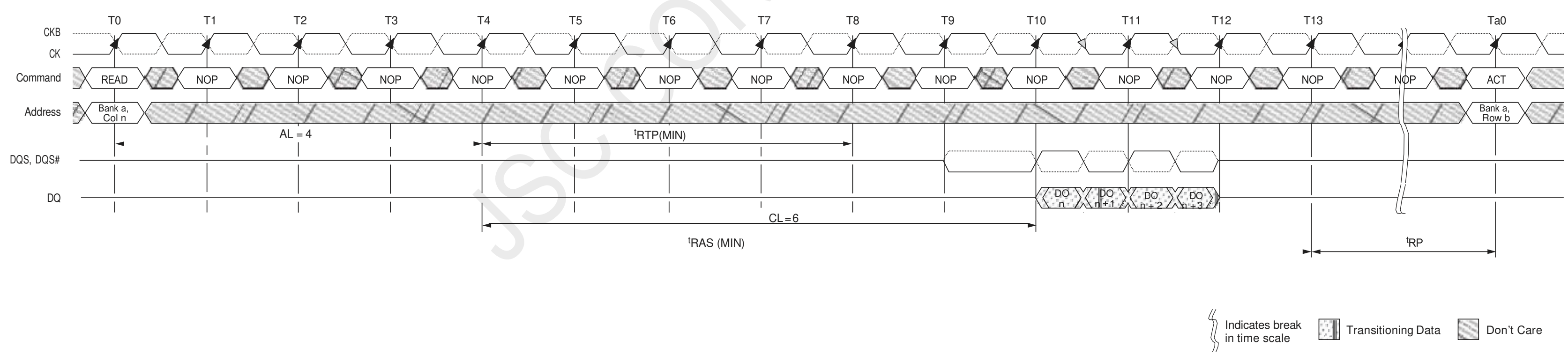
READ to PRECHARGE (BC4)



READ to PRECHARGE (AL = 5, CL = 6)



READ with Auto Precharge (AL = 4, CL = 6)



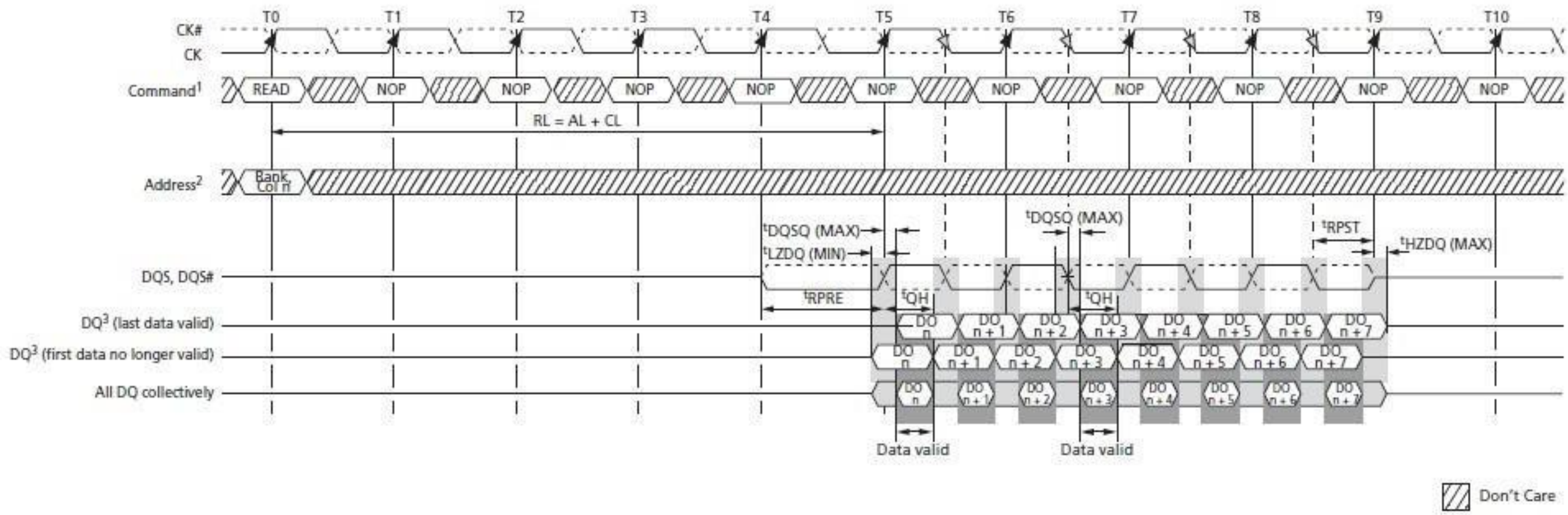
DQS to DQ output timing isshownin.The DQ transitions between valid data outputs must be within ^{t}DQSQ of the crossing point of DQS, DQS#. DQS must also maintaina minimum HIGH and LOW time of ^{t}QSH and ^{t}QSL. Prior to the READ preamble, the DQ balls will either be floating or terminated, depending on the status of the ODT signal.

Shows the strobe-to-clock timing during a READ. The crossing point DQS, DQS# must transition within ± ^{t}DQSCK of the clock crossing point. The data out has notiming relationship to CK, only to DQS, as shown.

Also show sthe READ preamble and postamble.Typically,both DQS and DQS# are High-Zto save power (V_{DDQ}).Priorto data output from the DRAM, DQS is driven LOW and DQS# is HIGH for ^{t}RPRE. This is known as the READ preamble.

The READpostamble, ^{t}RPST, is one half clock from the last DQS, DQS# transition. Dur ing the READ postamble, DQS is driven LOWand DQS# is HIGH. When complete,the DQ is disabled or continues terminating, depending on the state of the ODT signal. demonstrates how to measure ^{t}RPST.

Data Output Timing - tDQSQ and Data Valid Window

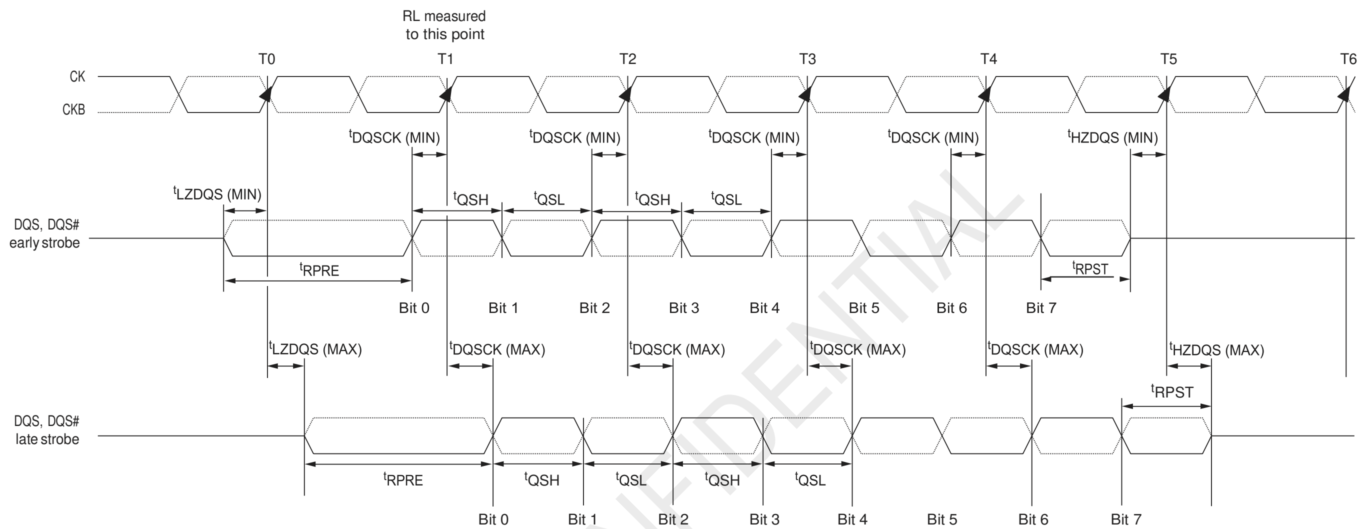


Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

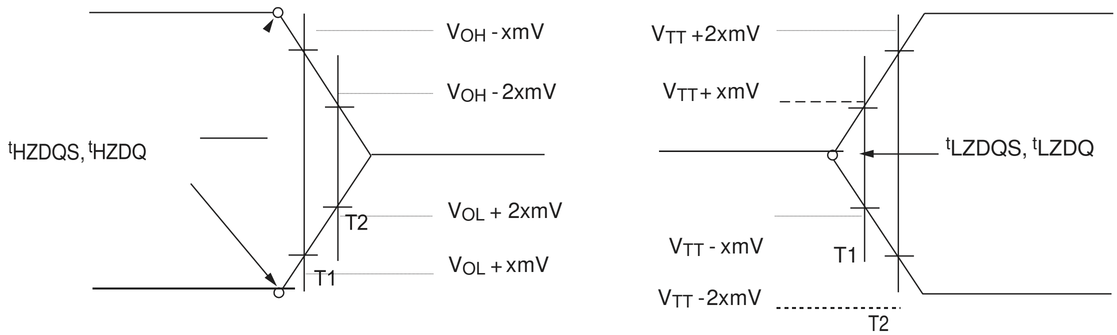
2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.
3. DO *n* = data-out from column *n*.
4. BL8, RL = 5 (AL = 0, CL = 5).
5. Output timings are referenced to $V_{DDQ}/2$ and DLL on and locked.
6. tDQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to CK.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can be early or late within a burst.

^{t}HZ and ^{t}LZ transitions occur in the same access time as valid data transitions. These parameter sare referenced to a specific voltage level that specifies when the device output is no longer driving ^{t}HZDQS and ^{t}HZDQ, or begins driving ^{t}LZDQS, ^{t}LZDQ. shows a method of calculating the point when the device is no longer driving ^{t}HZDQS and ^{t}HZDQ, or begins driving ^{t}LZDQS, ^{t}LZDQ, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters ^{t}LZDQS, ^{t}LZDQ, ^{t}HZDQS, and ^{t}HZDQ are defined as single-ended.

Data Strobe Timing – READs



Method for Calculating ^{t}LZ and ^{t}HZ



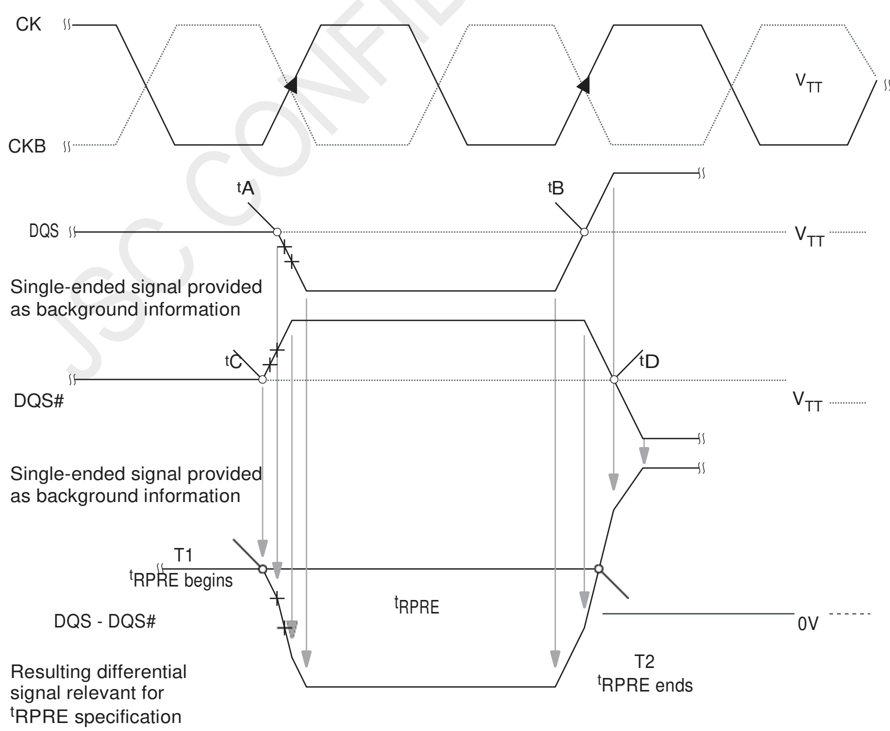
^{t}HZDQS, ^{t}HZDQ end point = 2 × T1 - T2 ^{t}LZDQS, ^{t}LZDQ begin point = 2 × T1 - T2

Notes: 1. Within a burst, the rising strobe edge is not necessarily fixed at ^{t}DQSCK (MIN) or ^{t}DQSCK (MAX). Instead, the rising strobe edge can vary between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX).

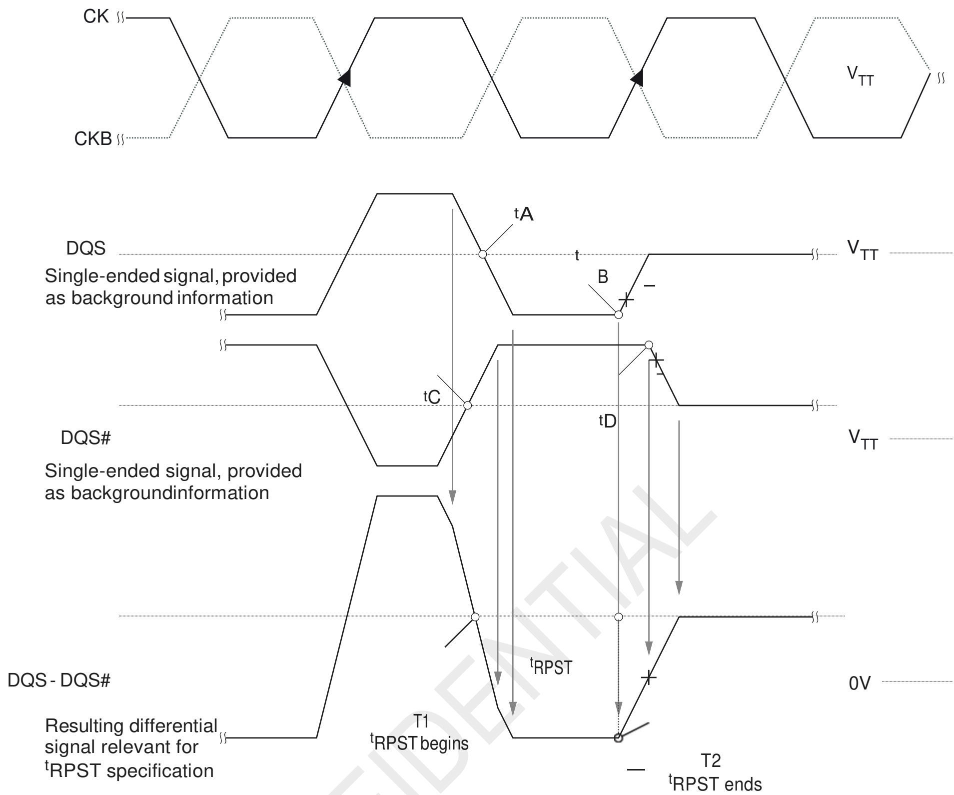
2. The DQS HIGH pulse width is defined by ^{t}QSH, and the DQS LOW pulse width is defined by ^{t}QSL. Likewise, ^{t}LZDQS (MIN) and ^{t}HZDQS (MIN) are not tied to ^{t}DQSCK (MIN) (early strobe case), and ^{t}LZDQS (MAX) and ^{t}HZDQS (MAX) are not tied to ^{t}DQSCK (MAX) (late strobe case); however, they tend to track one another.

3. The minimum pulse width of the READ preamble is defined by ^{t}RPRE (MIN). The minimum pulse width of the READ postamble is defined by ^{t}RPST (MIN).

^{t}RPRE Timing



^{t}RPST Timing



WRITE Operation

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for tha taccess. If auto precharge is selected, the row being accessed is pre-charged at the end of the WRITE burst. If auto precharge is no tselected, the row will remain open for sub sequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used through, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQS following the WRITE latency(WL) clocks later and subsequent data elements will be registered on successive edges of DQS. WRITE latency (WL) is defined as the sum of posted CAS additive latency(AL) and CAS WRITE latency (CWL) : WL = AL+ CWL. The values of AL and CWL are programmed in the MR0 and MR2 registers, respectively. Prior to the first valid DQS edge, a full cycle is needed (including a dummy cross over of DQS, DQS#) and specified as the WRITE preamble shown. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WLclocks $\pm{}^{t}$DQSS. through show the nominal case where ^{t}DQSS = 0ns; however, includes ^{t}DQSS (MIN) and ^{t}DQSS (MAX) cases.

Data may be masked fromcompleting a WRITE using datamask. The data mask occurs on the DM ball aligned to the WRITE data. If DM is LOW, the WRITE completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

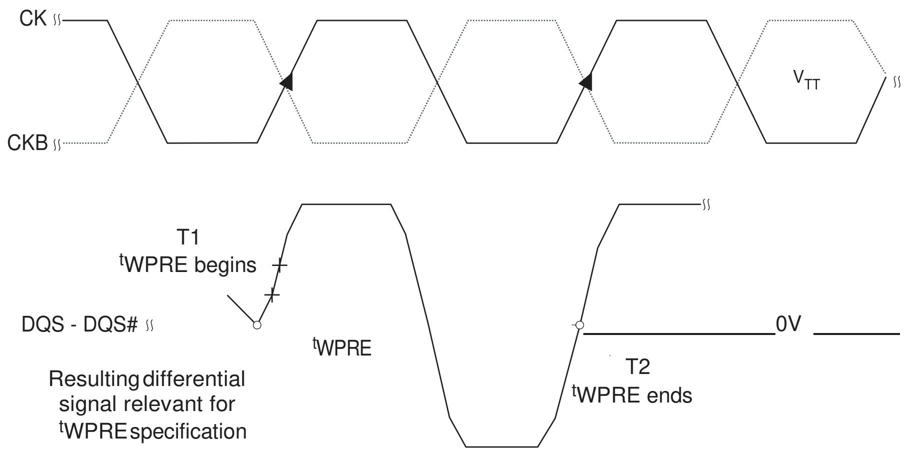
Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be ^{t}CCD clocks following the previous WRITE command. The first data element from the new burstis applied after the last element of acompleted burst.) show concatenated bursts. An example of non consecutive WRITEs is shown.

Data for any WRITE burst may be followed by a subsequent READ command after ^{t}WTR has been met .

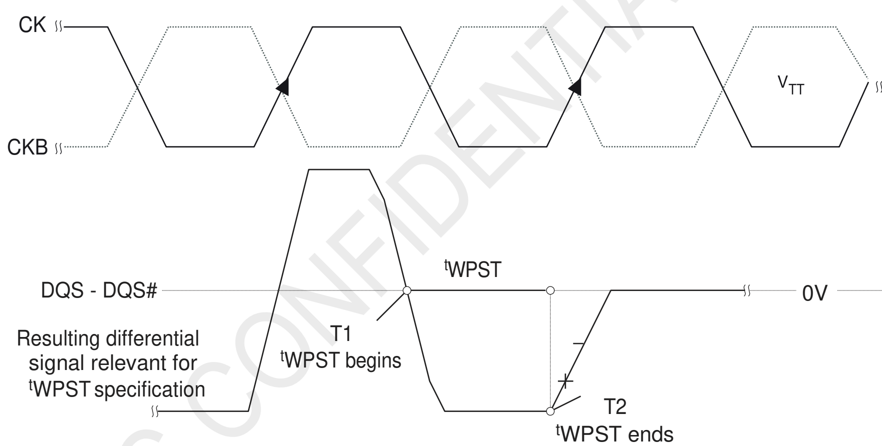
Data for any WRITE burst may be followed by a subsequent PRECHARGE command, providing ^{t}WRhasbeen met,as show.

Both ^{t}WTR and ^{t}WR starting time may vary, depending on the mode register settings (fixed BC4, BL8 versus OTF).

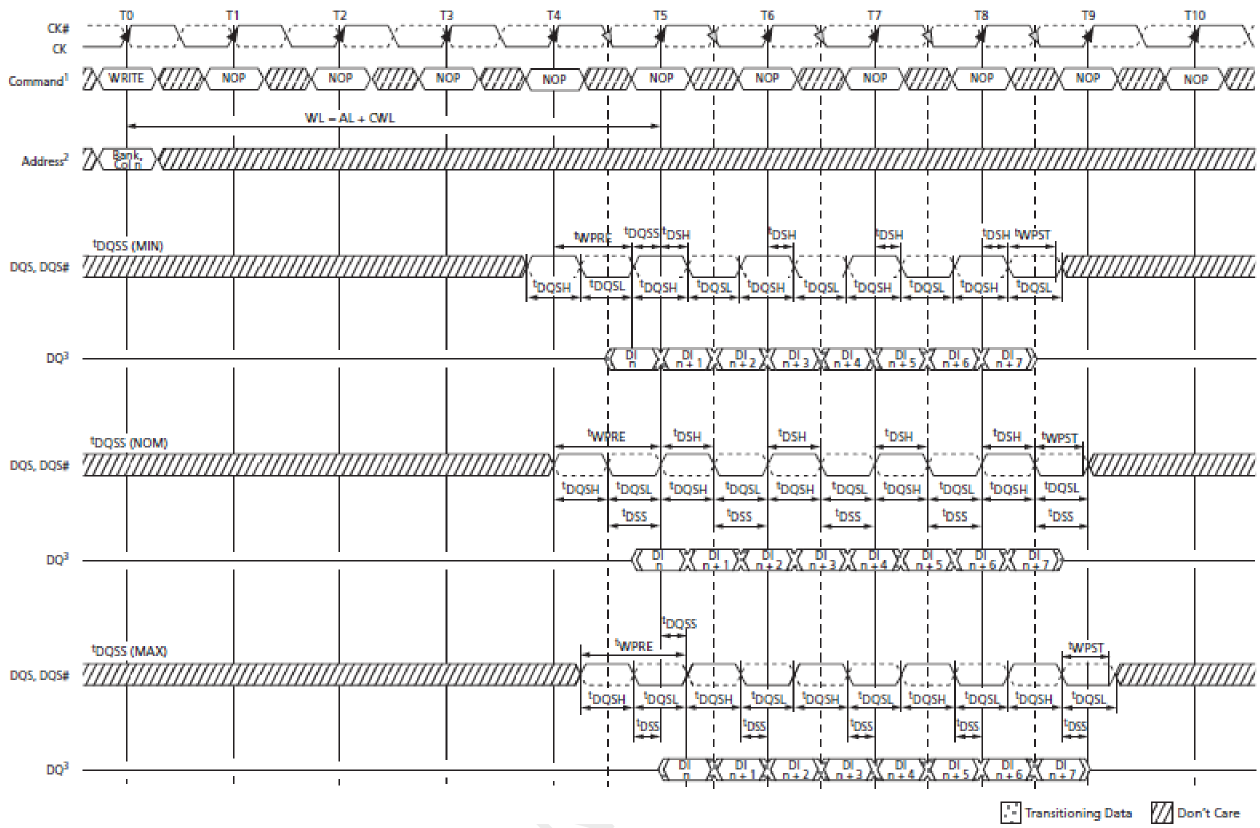
tWPRE Timing



tWPST Timing



WRITE Burst



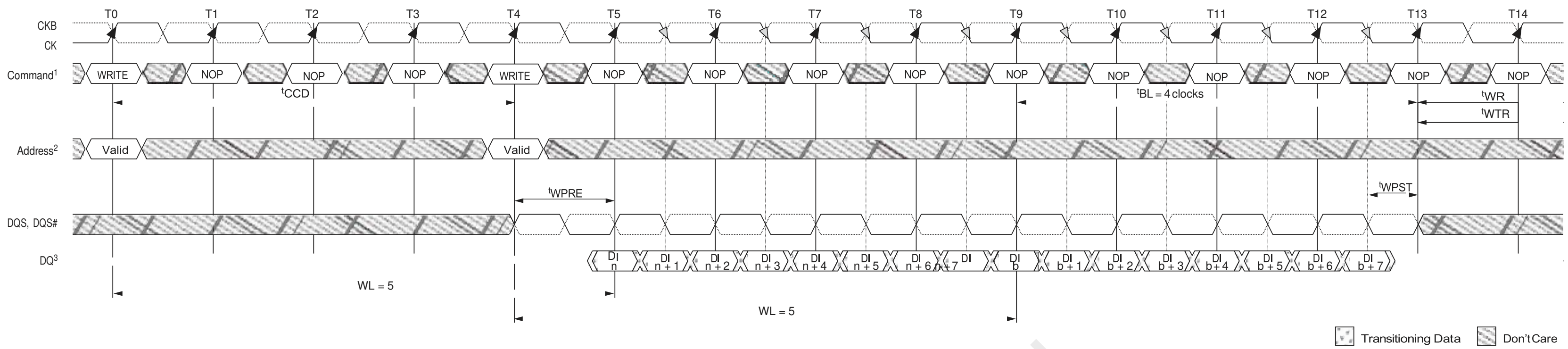
Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at thesetimes.

2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
3. DI *n* = data-in for column *n*. 4.

BL8, WL = 5 (AL = 0, CWL = 5).

5. ^{t}DQSS must be met at each rising clock edge.
6. ^{t}WPST is usually depicted as ending at the crossing of DQS, DQS#; however, ^{t}WPST actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

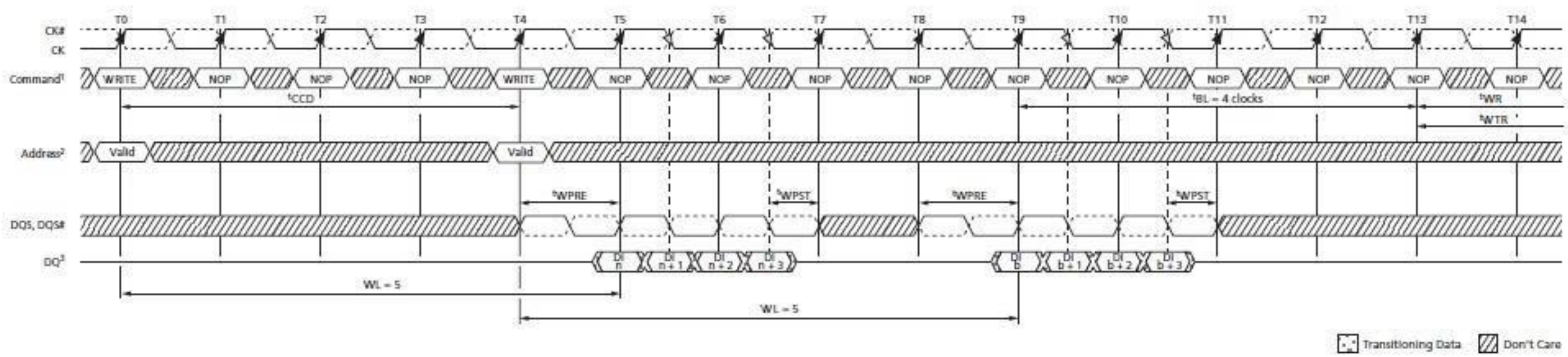
Consecutive WRITE (BL8) to WRITE (BL8)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. BL8, WL = 5 (AL = 0, CWL = 5).

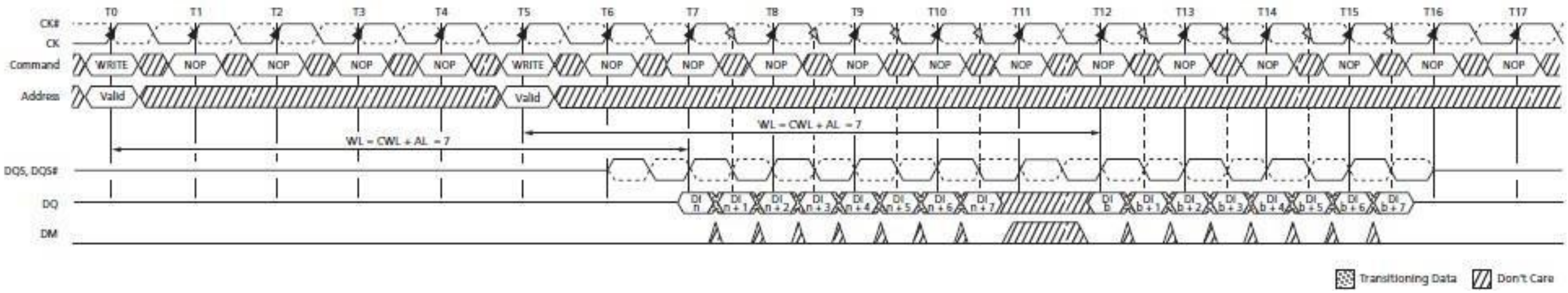
Consecutive WRITE (BC4) to WRITE (BC4) via OTF



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

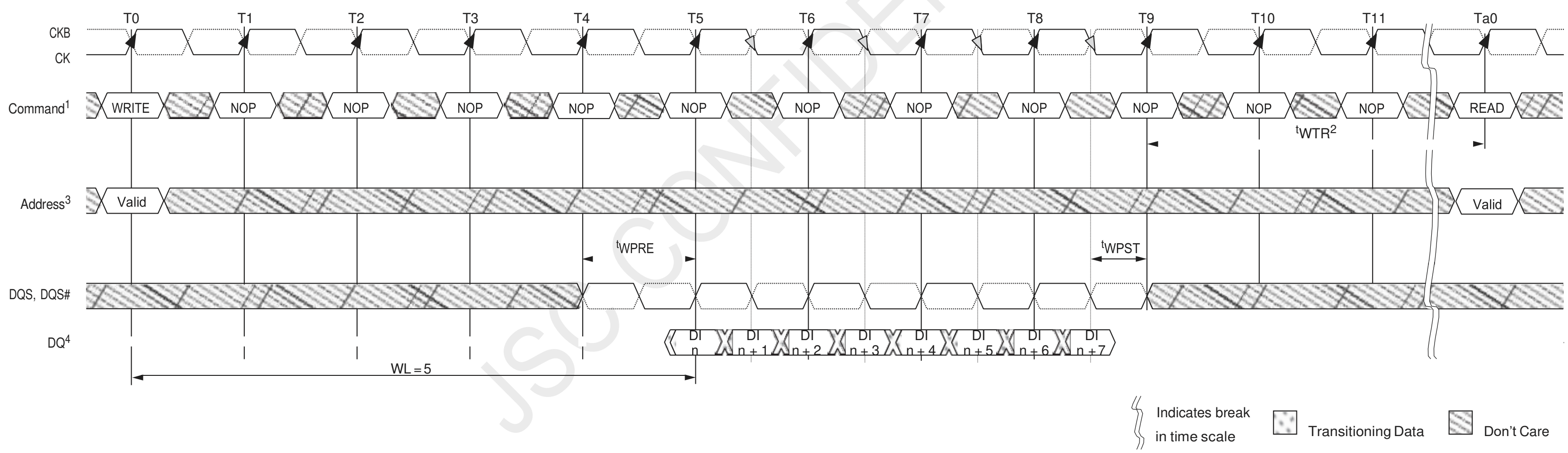
2. BC4, WL = 5 (AL = 0, CWL = 5).
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 andT4.
5. If set via MRS (fixed) tWR and tWTR would start T11 (2 cycles earlier).

Nonconsecutive WRITE to WRITE



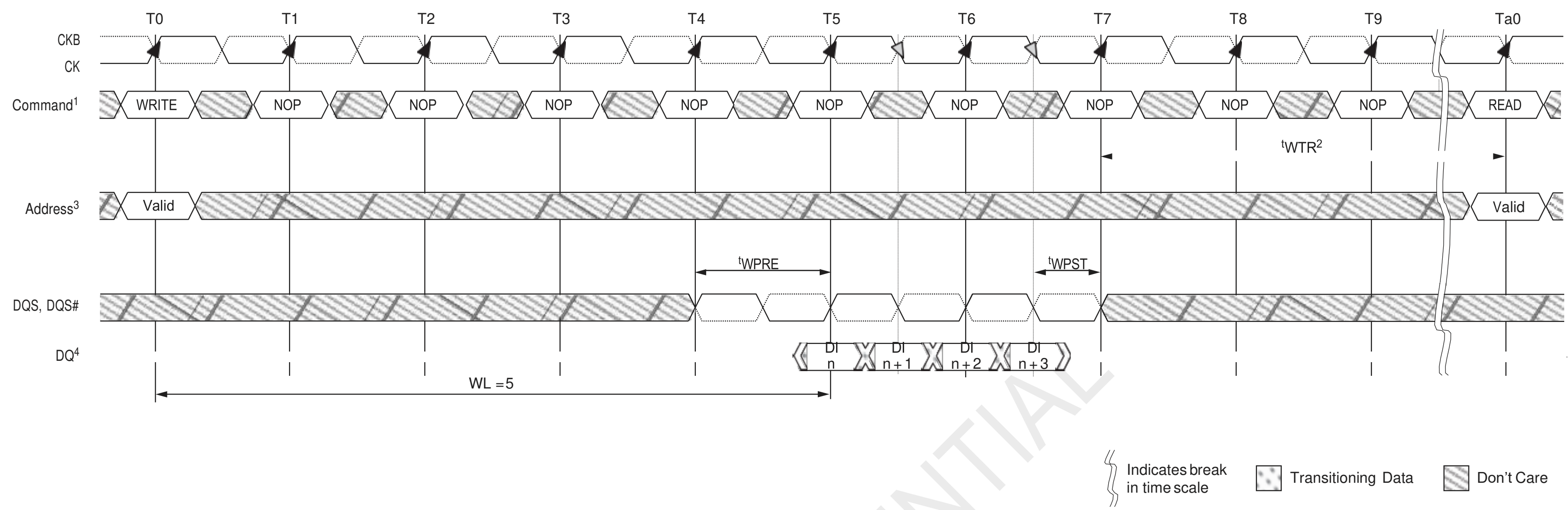
Notes: 1. DI *n* (or *b*) = data-in for column *n* (or column *b*).
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Each WRITE command may be to any bank.
4. Shown for WL = 7 (CWL = 7, AL = 0).

WRITE (BL8) to READ (BL8)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. ^{t}WTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
4. DI *n* = data-in for column *n*.
5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

WRITE to READ (BC4 Mode Register Setting)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

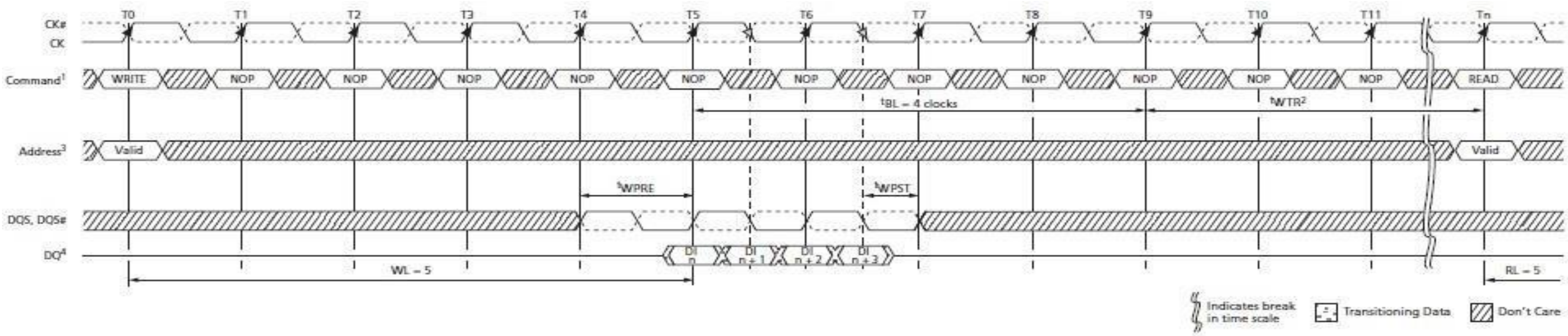
2. tWTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.

4. DI *n* = data-in for column *n*.

5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

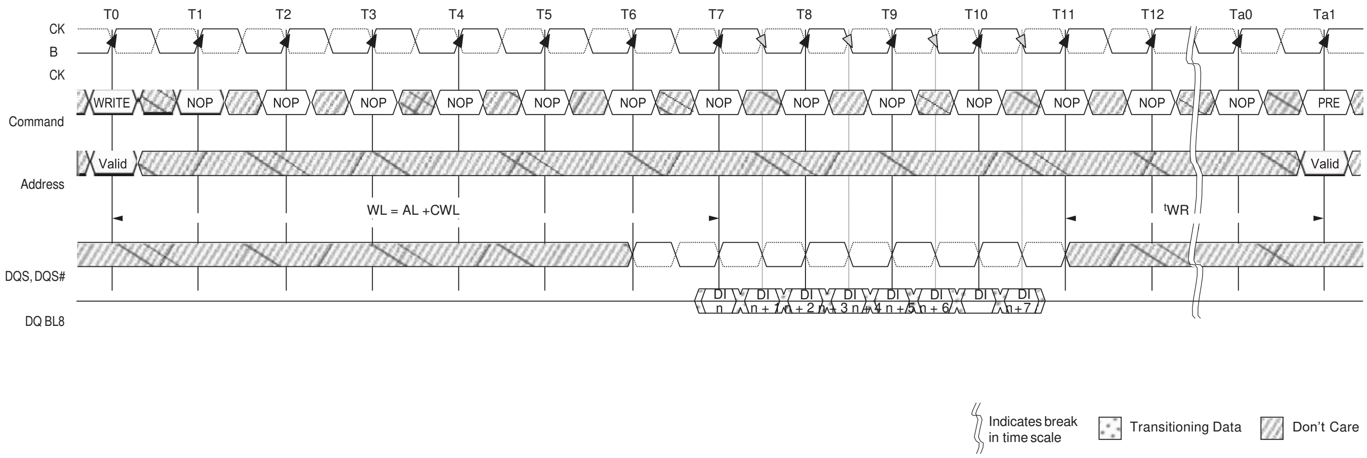
WRITE (BC4 OTF) to READ (BC4 OTF)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

2. ^{t}WTR controls the WRITE-to-READ delay to the same device and starts after ^{t}BL.
3. The BC4 OTF setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and the READ command at T*n*.
4. DI *n* = data-in for column *n*.
5. BC4, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

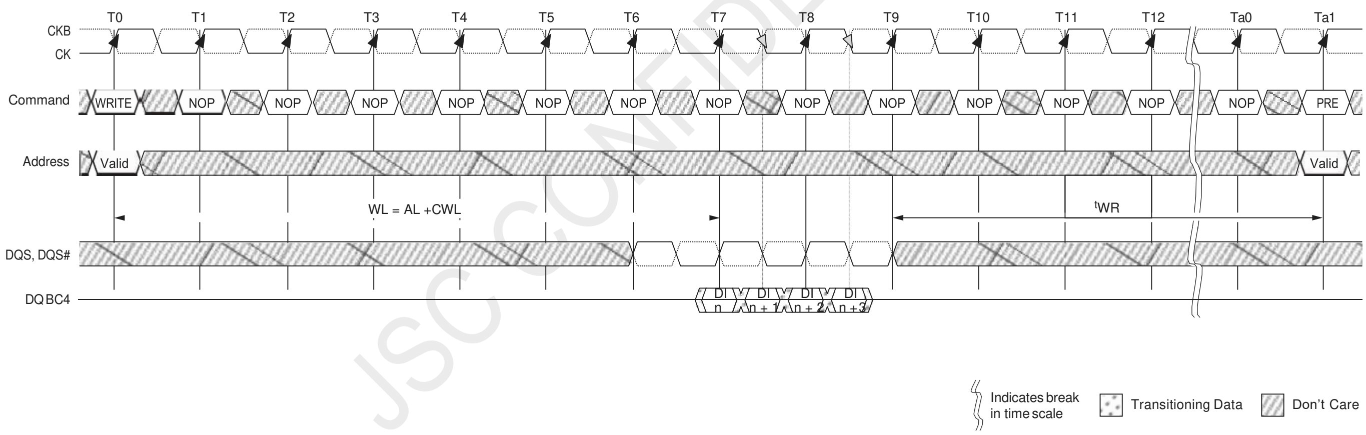
WRITE (BL8) to PRECHARGE



Notes: 1. DI *n* = data-in from column *n*.

2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Shown for WL = 7 (AL = 0, CWL = 7).

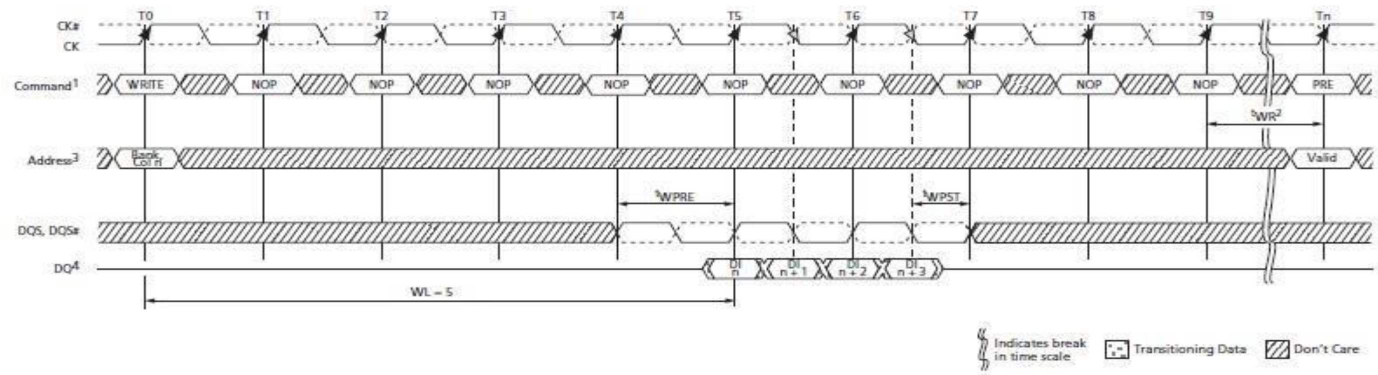
WRITE (BC4 Mode Register Setting) to PRECHARGE



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at thesetimes.

2. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data is shown at T7. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the samebank.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL= 5, RL = 5.

WRITE (BC4 OTF) to PRECHARGE



Notes: 1. NOP commands are shown for ease of illustration; other commands may bevalid at thesetimes.

2. The write recovery time (^{t}WR) is referenced from the rising clock edge at T9. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITEcommand at T0.
4. DI *n*= data-in for column *n*.
5. BC4 (OTF), WL = 5, RL = 5.

DQ Input Timing

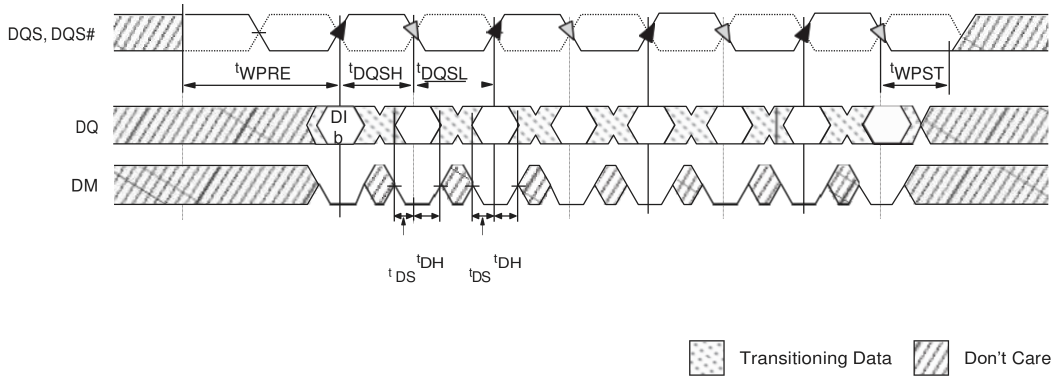
Shows the strobe-to-clock timing during a WRITE burst. DQS, DQS# must transition within 0.25^{t}CK of the clock transitions, as limited by ^{t}DQSS. All data and data mask setup and hold timings are measured relative to the DQS, DQS# crossing, not the clock crossing.

The WRITE preamble and postamble are also shown. One clock prior to data input to the DRAM,DQS must be HIGH and DQS# must be LOW.Then for a half clock, DQS is driven LOW(DQS# isdriven HIGH) during the WRITE preamble, ^{t}WPRE. Likewise, DQS must be kept LOW by the controller after the last data is written to the DRAM during the WRITE postamble, ^{t}WPST.

Data setup and hold times are also shown. All setup and hold times are measured from the crossing points of DQS and DQS#. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by ^{t}DQSH and ^{t}DQSL.

Data Input Timing



PRECHARGE Operation

Input A10 determines whether one bank or all banks are to be precharged and, in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as “Don’t Care.” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

SELF REFRESH Operation

The SELF REFRESH operation is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset uponexiting SELF REFRESH.

All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levelsuponentry/exit and during self refresh mode operation. V_{REFDQ} may float or not drive $V_{DDQ}/2$ while in self refresh mode under certain conditions:

- $V_{SS} < V_{REFDQ} < V_{DD}$ is maintained.
- V_{REFDQ} is valid and stable prior to CKE going back HIGH.
- The first WRITE operation may not occur earlier than 512 clocks after V_{REFDQ} is valid.
- All other self refresh mode exit timing requirements are met.

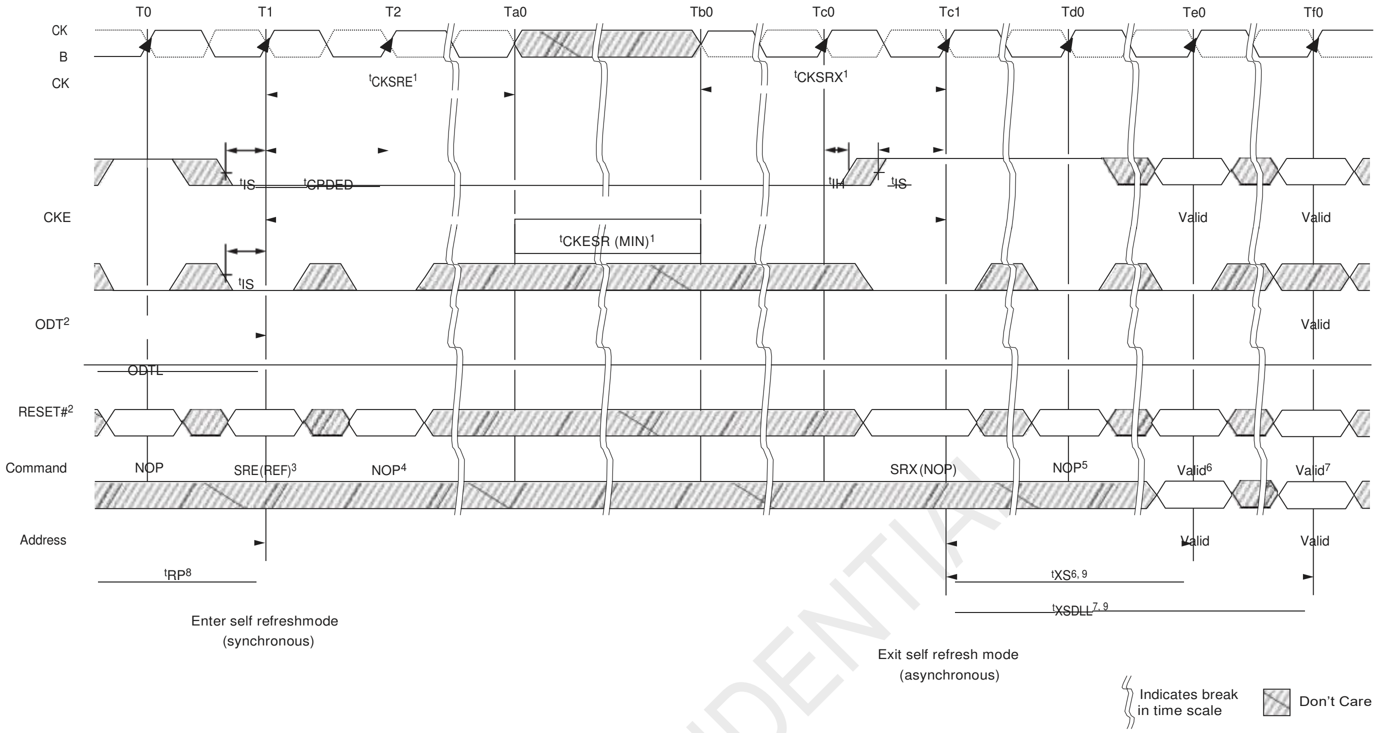
The DRAMmust be idle with all banks in the precharge state(^tRP is satisfied and no bursts are in progress) before a self refresh entry command can be issued. ODT must also be turned off before selfrefresh entry by registering the ODT ball LOW prior to the self refresh entry command (see On-Die Termination (ODT) (for timing requirements). If $R_{TT,nom}$ and $R_{TT(WR)}$ are disabled in the mode registers, ODT can be a“Don’t Care.” After these lf refresh entry command is registered, CKE must be held LOW to keep the DRAM in self refresh mode.

After the DRAM has entered self refresh mode, all external control signals, except CKE and RESET#, are “Don’t Care.” The DRAM initiates a minimum of one REFRESH command internally within the ^tCKE period when it enters self refresh mode.

The requirements for entering and exiting self refresh mode depend on the state of the clock during self refresh mode. First and foremost,the clock must be stable (meeting ^tCK specifications) when self refresh mode is entered. If the clock remains stable and the frequency is not altered while in self refreshmode,then the DRAM is allowed to exit self refresh mode after ^tCKESR is satisfied (CKE is allowed to transition HIGH ^tCKESR later than when CKE was registered LOW). Since the clock remains stable in self refresh mode(no frequencyc hange), ^tCKSRE and ^tCKSRX are not required. However, if the clock is altered during self refresh mode (if it is turned-off or its frequency changes), then ^tCKSRE and ^tCKSRX must be satisfied. When entering self refresh mode, ^tCKSRE must be satisfied prior to altering the clock's frequency. Prior to exiting self refresh mode, ^tCKSRX must be satisfied prior to registering CKE HIGH.

When CKE is HIGHduring self refresh exit, NOP or DES must be issued for ^tXS time. ^tXS is required for the completion of any internal refresh already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. ^tXS is also the earliest time self refresh reentry may occur. Before a command requiring a locked DLL can be applied, a ZQCL command must be issued, ^tZQOPER timing must be met, and ^tXSDLL must be satisfied. ODT must be off during ^tXSDLL.

Self Refresh Entry/Exit Timing



Notes: 1. The clock must be valid and stable, meeting ^{t}CK specifications at least ^{t}CKSRE after entering self refresh mode, and at least ^{t}CKSRX prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then ^{t}CKSRE and ^{t}CKSRX do not apply; however, ^{t}CKESR must be satisfied prior to exiting at SRX.

2. ODT must be disabled and R_{TT} off prior to entering self refresh at state T1. If both $R_{TT,nom}$ and $R_{TT(WR)}$ are disabled in the mode registers, ODT can be a "Don't Care."
3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
4. A NOP or DES command is required at T2 after the SRE command is issued prior tothe inputs becoming "Don't Care."
5. NOP or DES commands are required prior to exiting self refresh mode until stateTe0.
6. ^{t}XS is required before any commands not requiring a locked DLL.
7. ^{t}XSDLL is required before any commands requiring a locked DLL.
8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, ^{t}RP must be met, and no data bursts can be in progress.
9. Self refresh exit is asynchronous; however, ^{t}XS and ^{t}XSDLL timings start at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR at Tc1. ^{t}CKSRX timing is also measured so that ^{t}ISXR is satisfied at Tc1.

Extended Temperature Usage

JSC's DDR3 SDRAM support the optional extended case temperature (T_C) range of -40°C to 95°C. Thus, the SRT and ASR options must be used at a minimum.
The extended temperaturerange DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refresh requirement is accomplished by reducing the refresh period from 64ms to 32ms. However,self refresh mode requires either ASR or SRT to support the extended temperature.Thus,either ASR or SRT must be enabled whenT_C is above 85°C or self refresh can not be used until T_C is at or below 85°C. summarizes the two extended temperature options and summarizes how the two extended temperature options relate to one another.

Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6] = 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7] = 0: Normal operating temperature range (-10°C to 85°C) *MR2[7] = 1: Extended operating temperature range (-10°C to 95°C) If ASR is enabled (MR2[7] = 1), SRT must be set to 0, even if the extended temperature range is supported *MR2[7] = 0: SRT is disabled
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values) * MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH operation * MR2[6] = 0: ASR is disabled; must use manual self refresh temperature (SRT)

Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (-10°C to 85°C)
0	1	Self refresh mode is supported in normal and extended temperature ranges; When SRT is enabled, it increases self refresh power consumption	Normal and extended (-10°C to 95°C)
1	0	Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be temperature-dependent	Normal and extended (-10°C to 95°C)
1	1	Illegal	

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while an MRS, MPR, ZQCAL, READ,or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down I_{DD} specifications are not applicable until such operations have completed. Depending on the previous DRAM state and the command is sued prior to CKE going LOW, certain timing constraints must be satisfied. Timing diagrams detailing the different power-down mode entry and exits are shown.

Command to Power-Down Entry Parameters

DRAM Status	Last Command Prior to CKE LOW[1]	Parameter (Min)	Parameter Value
Idle or active	ACTIVATE	^{t}ACTPDEN	1^{t}CK
Idle or active	PRECHARGE	^{t}PRPDEN	1^{t}CK
Active	READ or READAP	^{t}RDPDEN	RL + 4^{t}CK + 1^{t}CK
Active	WRITE: BL8OTF, BL8MRS, BC4OTF	^{t}WRPDEN	WL + 4^{t}CK + ^{t}WR/^{t}CK
Active	WRITE: BC4MRS		WL + 2^{t}CK + ^{t}WR/^{t}CK
Active	WRITEAP: BL8OTF, BL8MRS, BC4OTF	^{t}WRAPDEN	WL + 4^{t}CK + WR + 1^{t}CK
Active	WRITEAP: BC4MRS		WL + 2^{t}CK + WR + 1^{t}CK
Idle	REFRESH	^{t}REFPDEN	1^{t}CK
Power-down	REFRESH	^{t}XPDLL	Greater of 10^{t}CK or 24ns
Idle	MODE REGISTER SET	^{t}MRSPDEN	^{t}MOD

Note: 1. If slow-exit mode precharge power-down is enabled and entered, ODT becomes asynchronous ^{t}ANPD prior to CKE going LOW and remains asynchronous until ^{t}ANPD + ^{t}XPDLL after CKE goes HIGH.

Entering power-down disables the input and output buffers, excluding CK, CKB, ODT, CKE, and RESET#. NOP or DES commands are required until ^{t}CPDED has been satisfied, at which time all specified input/output buffers are disabled. The DLL should be in alockedstate when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after allin progress commands are complete, the DRAM will be inactive power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-downmode must be programmed to exit with either as low exit mode or a fast exit mode.When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL also remains on when entering active power-down. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered. Refer to Asynchronous ODT Mode for detailed ODT usage requirements in slow

Exit mode precharge power-down. A summary of the two power-down modes is listed.

While in either power-down state,CKE is held LOW, RESET# is held HIGH, and as table clock signal must be maintained. ODT must be in a valid state but all other input signals are "Don't Care." If RESET # goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until ^{t}PD (MIN) has been satisfied. The maximum time allowed for power- down duration is^{t}PD(MAX) (9 ×^{t}REFI).

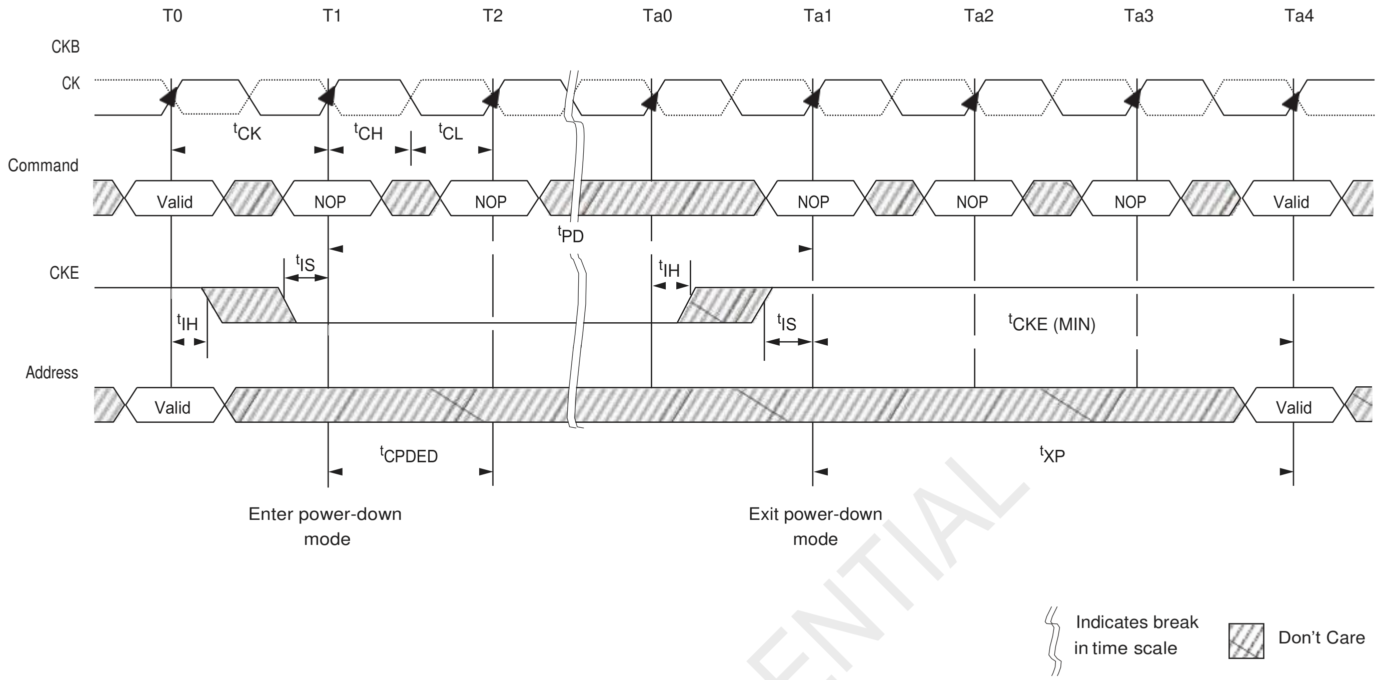
The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until ^{t}CKE has been satisfied. A valid, executable command may be applied after power-down exit latency, ^{t}XP, and ^{t}XPDLL have been satisfied. A summary of the power-down modes is listed be- low.

For specific CKE-intensive operations, such as repeating a power-down-exit-to-refresh-to-power-down-entry sequence,the number of clockc yclesb etween power-dow nexit and power-down entry may not be sufficient to keep the DLLproperlyupdated.Inaddi- tion to meeting^{t}PD whenthe REFRESH command is used between power-down exit and power-down entry, two other conditions must be met. First,^{t}XP must be satisfied before issuing the REFRESHcommand. Second, ^{t}XPDLL must be satisfied before the next power-down may be entered. An example is shown .

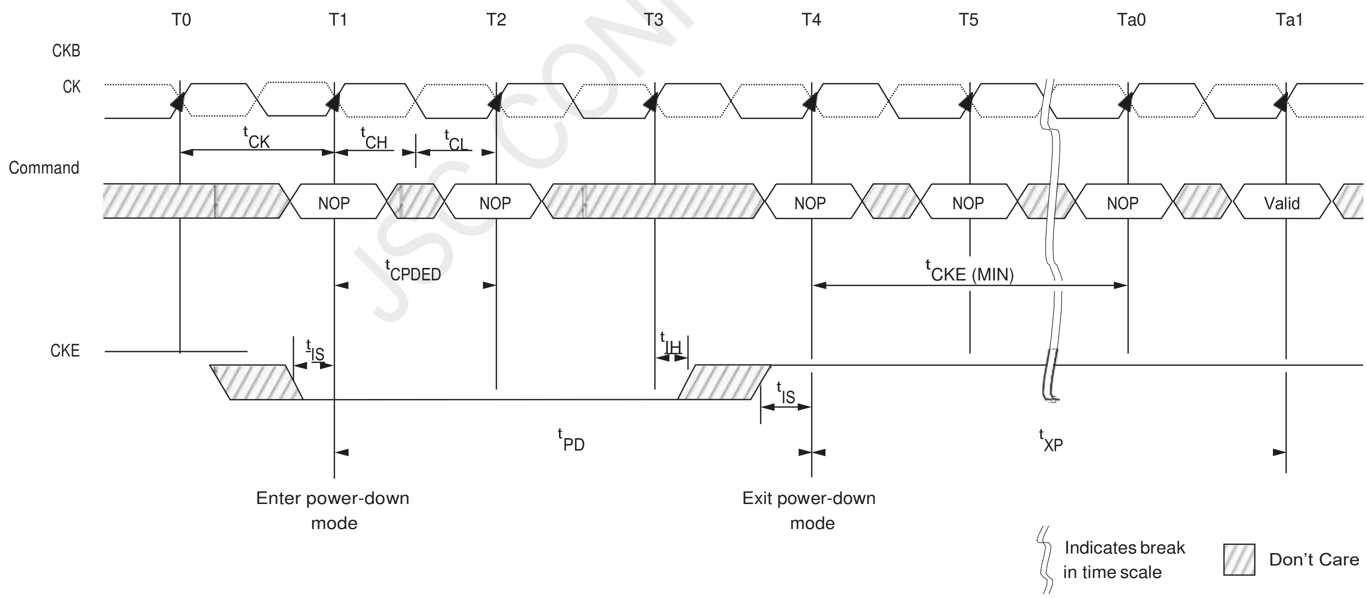
Power-Down Modes

DRAM State	MR0[12]	DLL State	Power-Down Exit	Relevant Parameters
Active (any bank open)	"Don't Care"	On	Fast	^{t}XP to any other valid command
Precharged (all banks precharged)	1	On	Fast	^{t}XP to any other valid command
	0	Off	Slow	^{t}XPDLL to commands that require the DLL to be locked (READ, RDAP, or ODT on); ^{t}XP to any other valid command

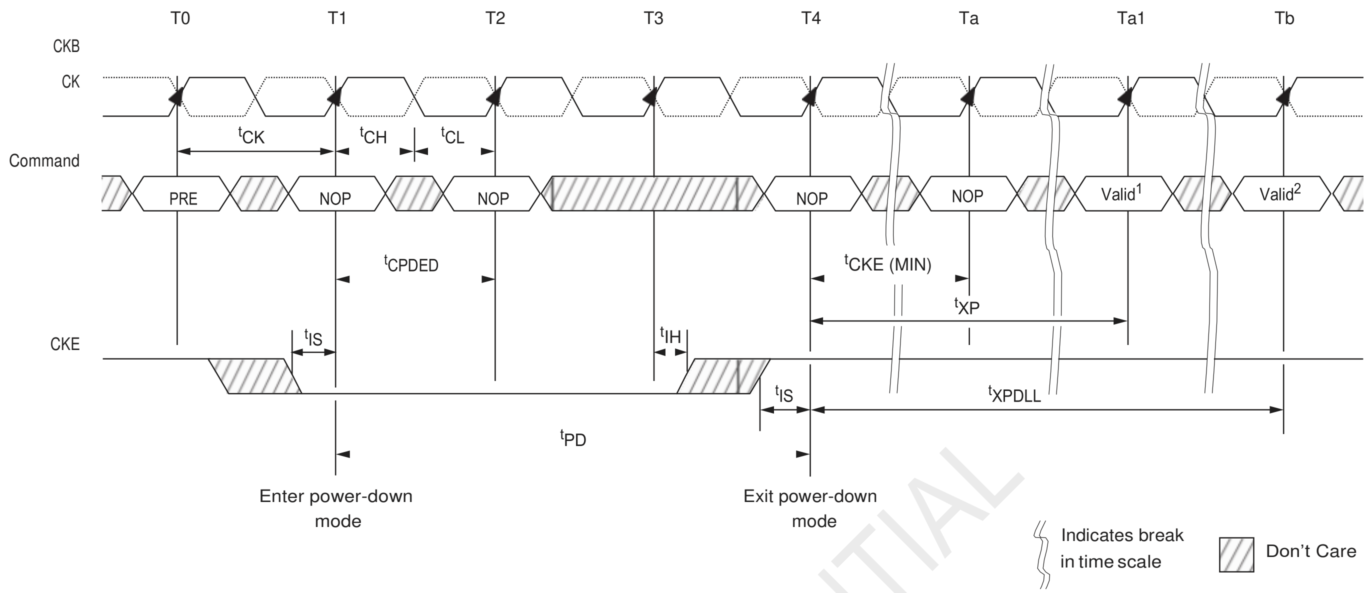
Active Power-Down Entry and Exit



Precharge Power-Down (Fast-Exit Mode) Entry and Exit

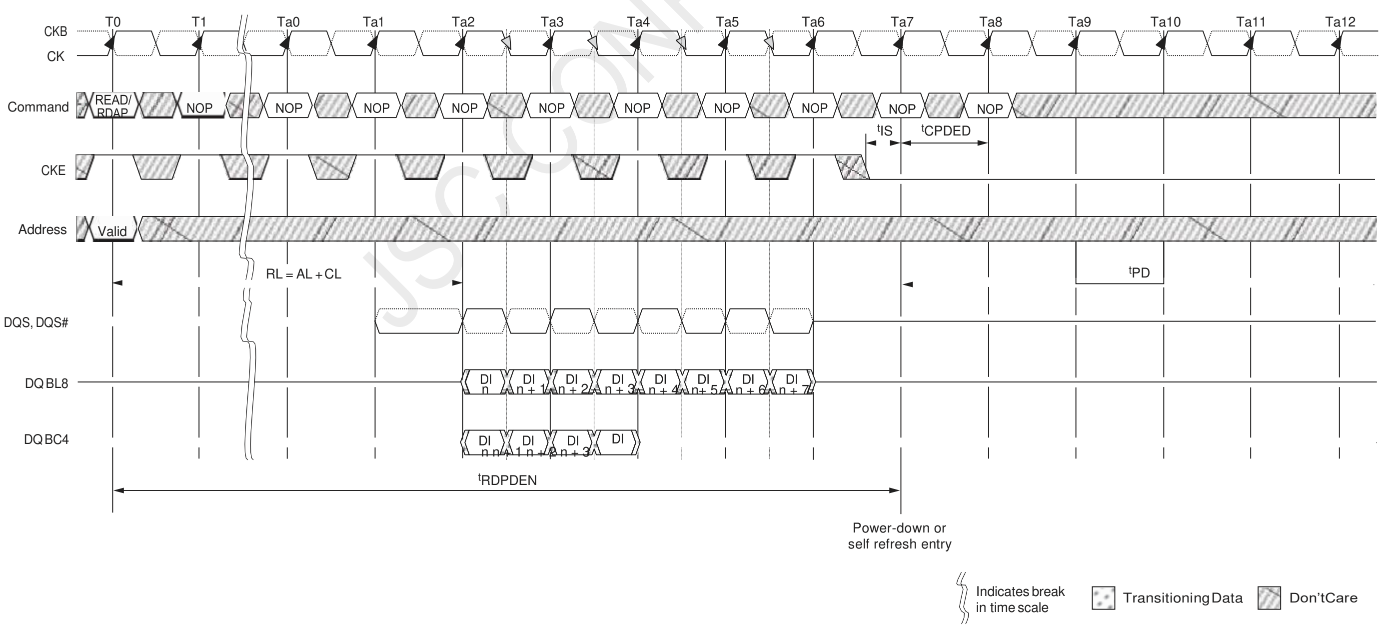


Precharge Power-Down (Slow-Exit Mode) Entry and Exit

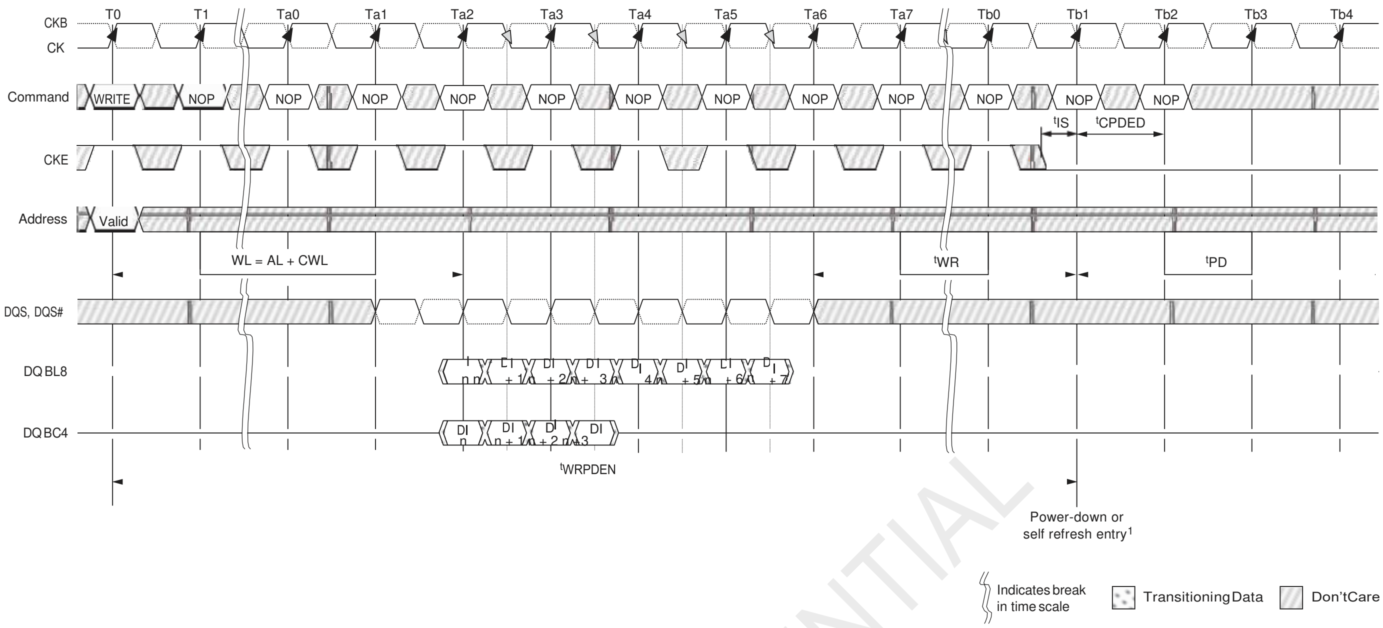


Notes: 1. Any valid command not requiring a locked DLL.
2. Any valid command requiring a locked DLL.

Power-Down Entry After READ or READ with Auto Precharge (RDAP)

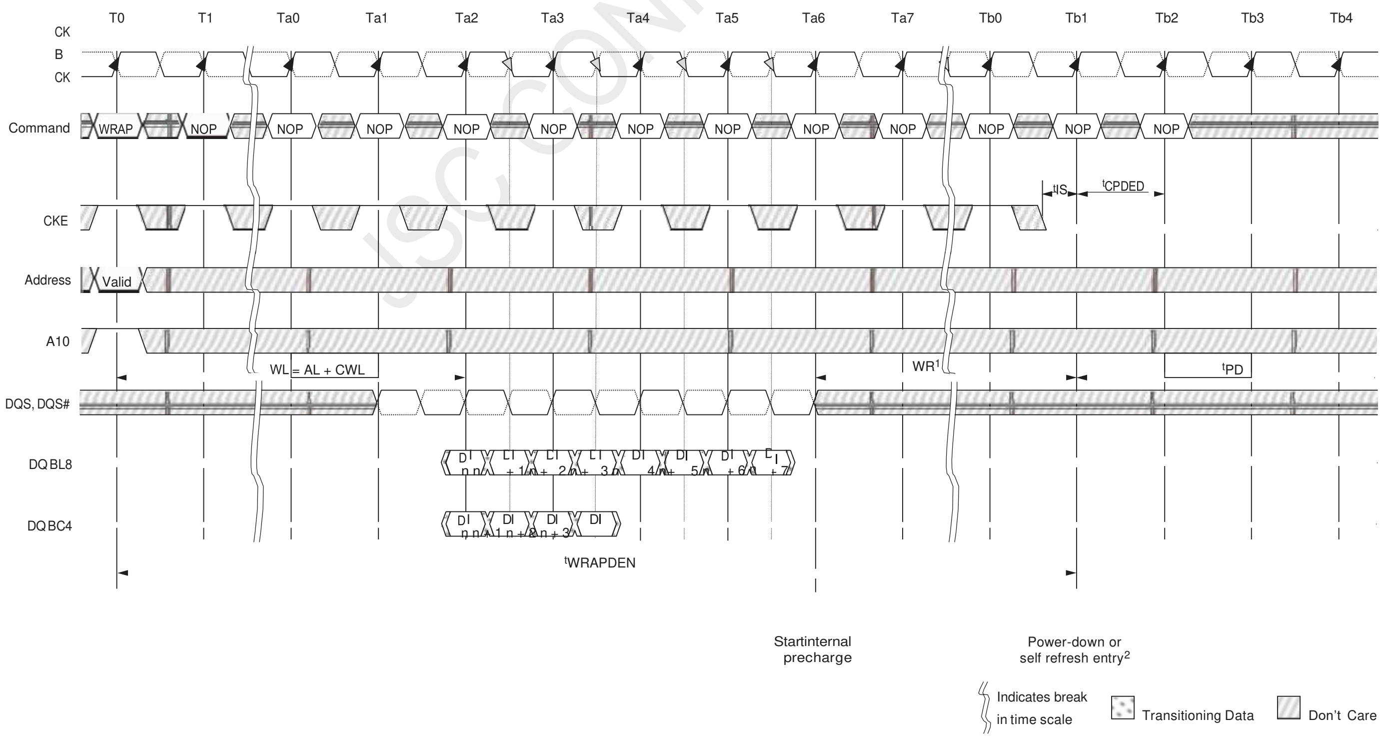


Power-Down Entry After WRITE



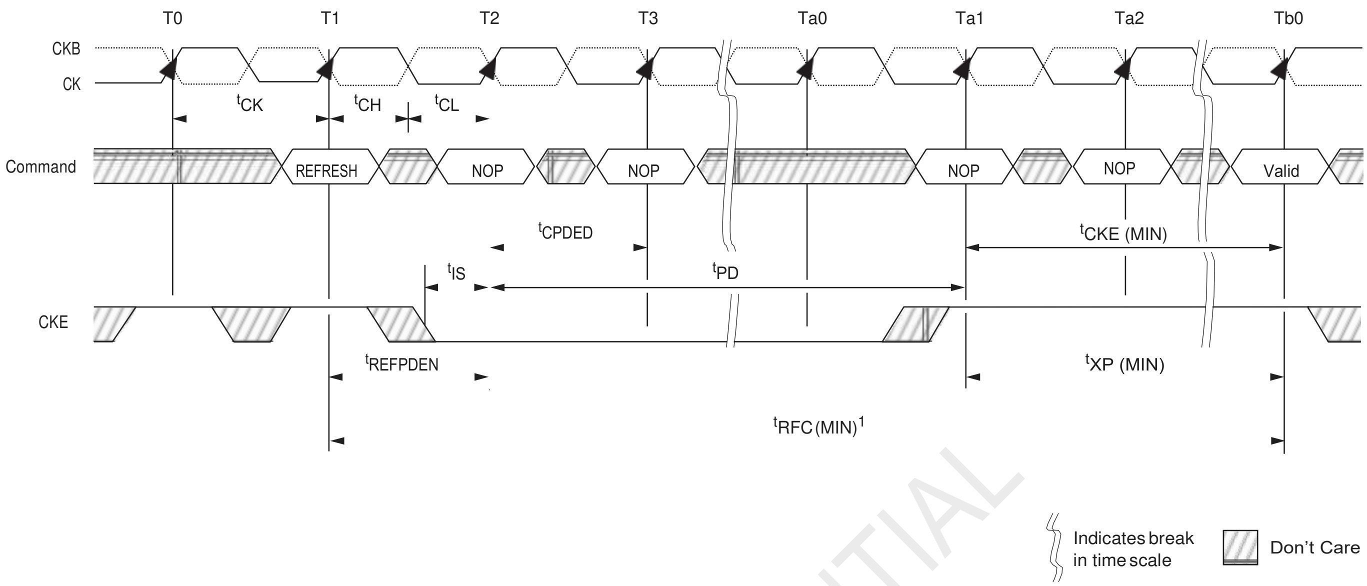
Note: 1. CKE can go LOW 2^{t}CK earlier if BC4MRS.

Power-Down Entry After WRITE with Auto Precharge (WRAP)



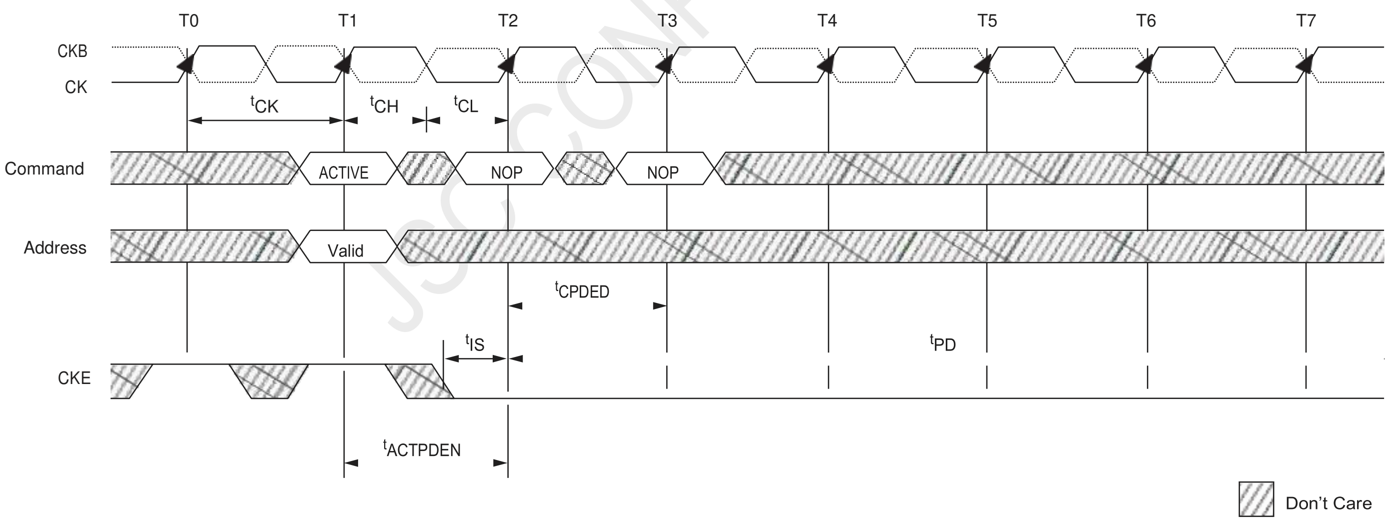
Notes: 1. ^{t}WR is programmed through MR0[11:9] and represents ^{t}WRmin (ns)/^{t}CK rounded up to the next integer ^{t}CK.
2. CKE can go LOW 2^{t}CK earlier if BC4MRS.

REFRESH to Power-Down Entry

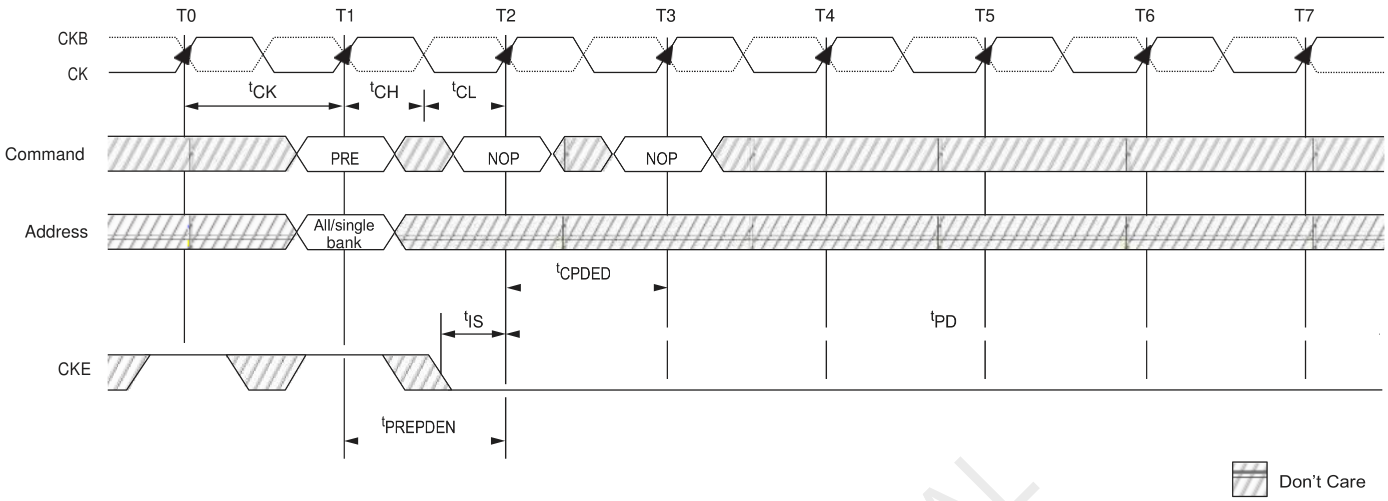


Note: 1. After CKE goes HIGH during tRFC, CKE must remain HIGH until tRFC is satisfied.

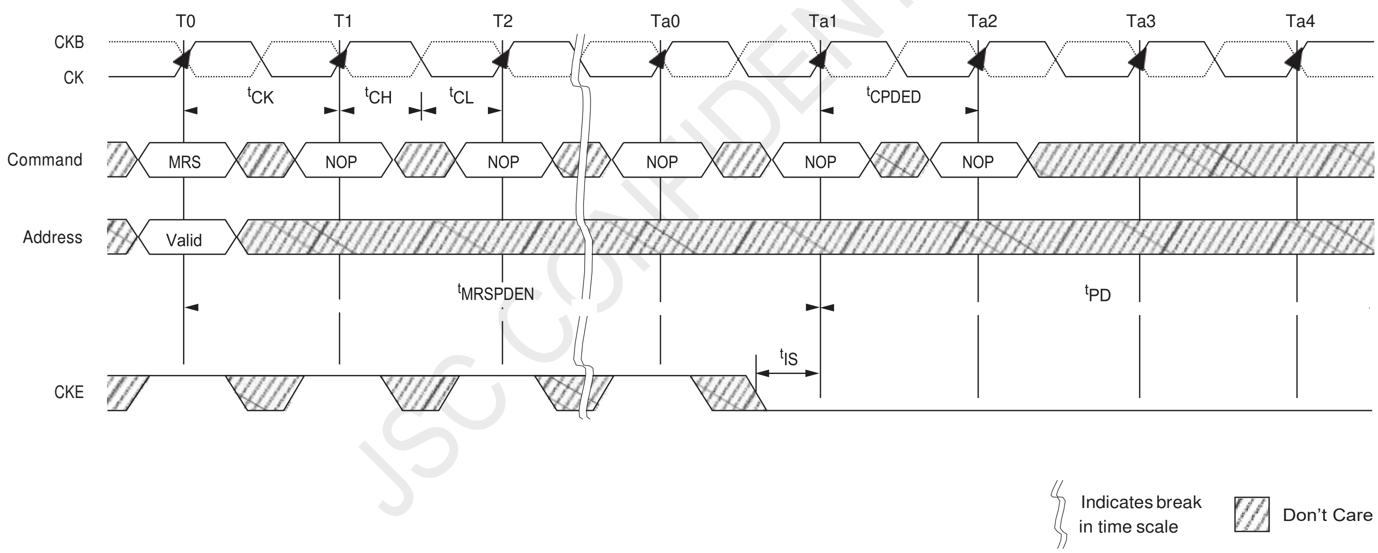
ACTIVATE to Power-Down Entry



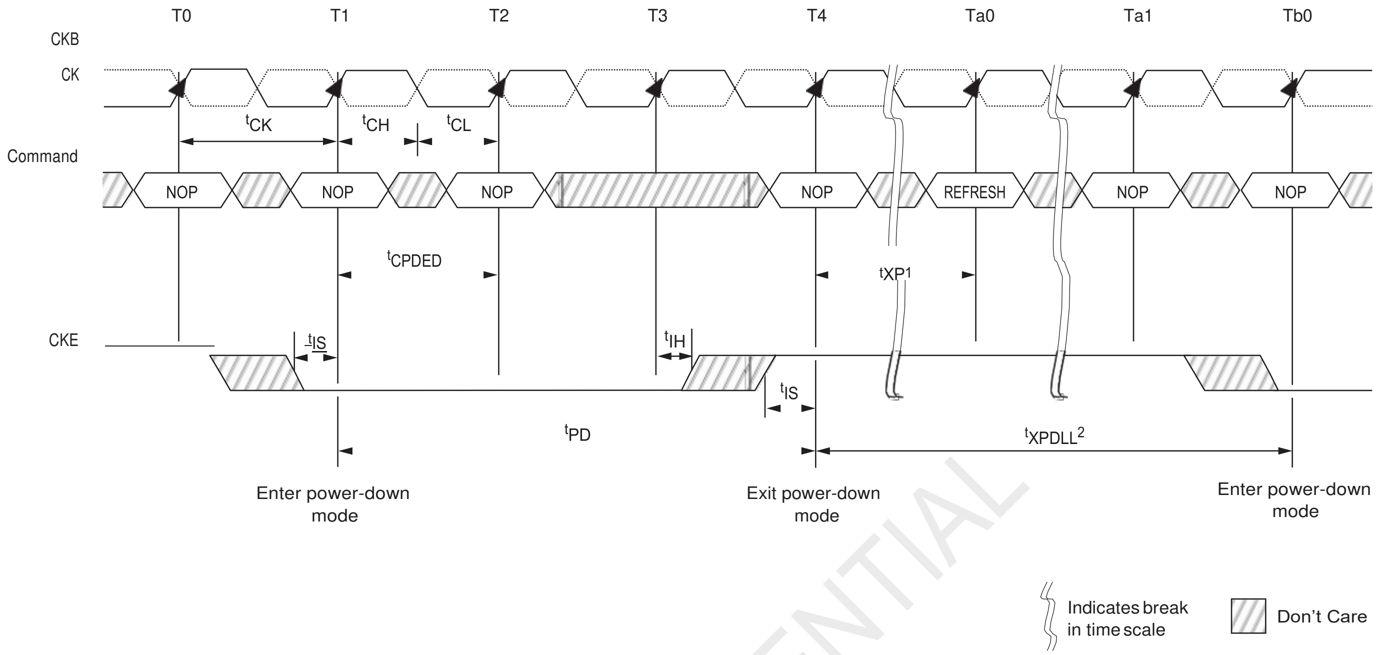
PRECHARGE to Power-Down Entry



MRS Command to Power-Down Entry



Power-Down Exit to Refresh to Power-Down Entry

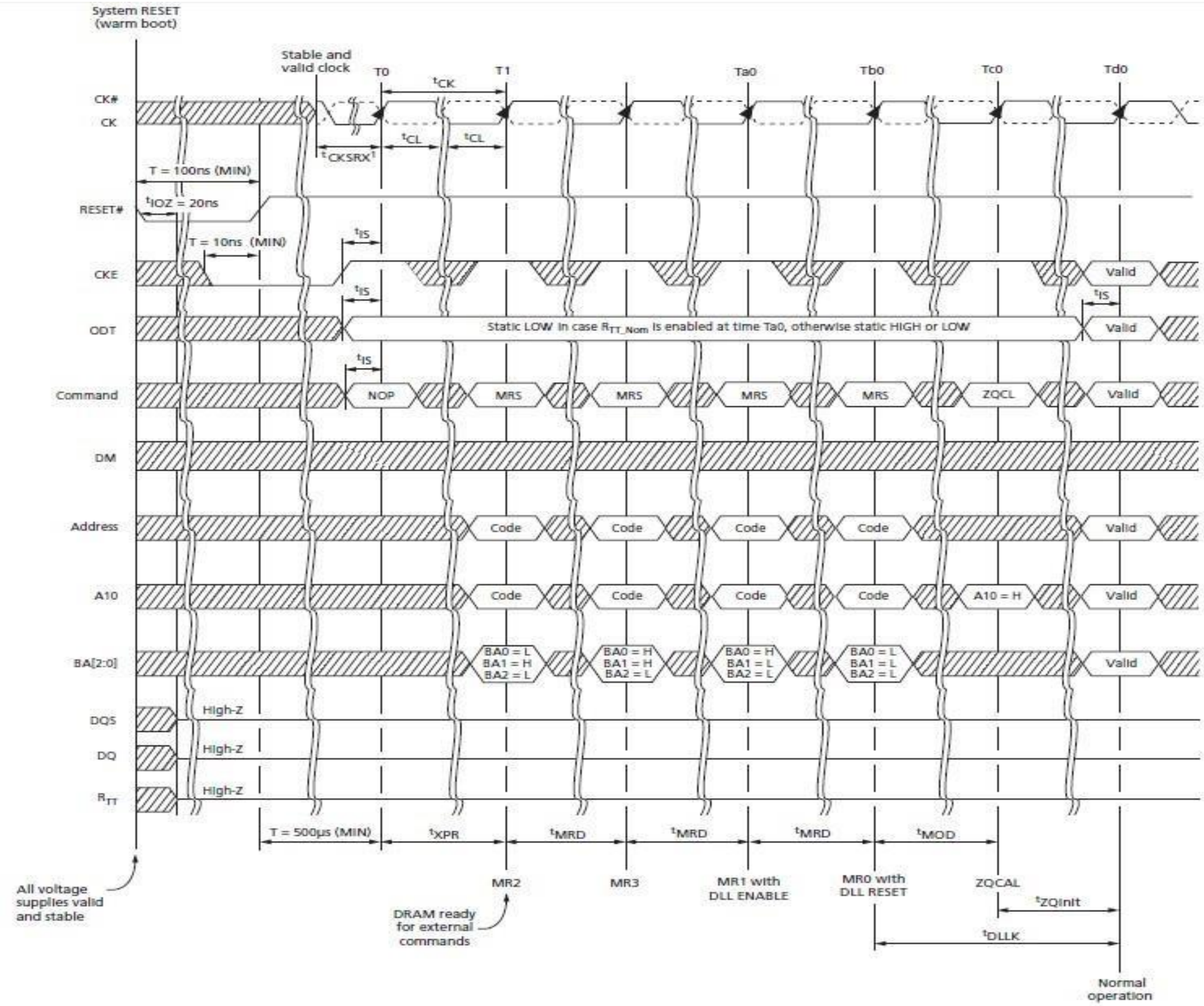


Notes: 1. tXP must be satisfied before issuing the command.
2. tXPDLL must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

RESET Operation

The RESET signal (RESET#) is an asynchronous reset signal that triggers anytime it drops LOW, and there are no restrictions about when it can go LOW. After RESET# goes LOW,it must remain LOW for 100ns. During this time,the outputs are disabled, ODT (R_{TT}) turns off (High-Z),and the DRAM reset sitself. CKE should be driven LOW prior t o RESET# being driven HIGH. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed. All counters, except refresh counters, on theDRAMare reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

RESET Sequence



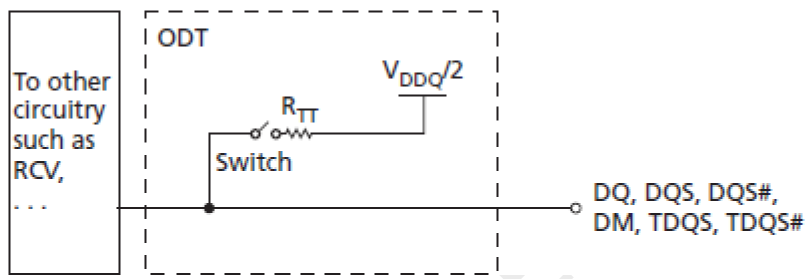
Note: 1. The minimum time required is the longer of 10ns or 5 clocks.

On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM for x4 and x8 configuration (and TDQS, TDQS# for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control

pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this documen.

On-Die Termination



Functional Representation of ODT

Thevalue of R_{TT} (ODT termination resistance value) is determined by the settings of several mode register bits. The ODT ball is ignored while in self refresh mode (must be turned off prior to self refresh entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous mode (when the DLL is off during precharge power-downorwhen the DLL is synchronizing).
Nominal ODT is the base termination and isusedinany allowable ODTstate.
Dynamic ODT is applied only during writes and provides OTF switching from no R_{TT} or $R_{TT,nom}$ to $R_{TT(WR)}$.

The actual effective termination, $R_{TT(EFF)}$, maybe different from R_{TT} targeted due to non linearity of the termination. For $R_{TT(EFF)}$ values and calculations.

Nominal ODT

ODT(NOM) is the base termination resistance for each applicable ball; it is enabled or disabled via MR1[9,6,2] (see Mode Register1(MR1) Definition),and it is turned on or off via the ODT ball.

Truth Table - ODT (Nominal)

Note 1 applies to the entire table

MR1[9, 6, 2]	ODT Pin	DRAM Termination State	DRAM State	Notes
000	0	$R_{TT,nom}$ disabled, ODT off	Any valid	2
000	1	$R_{TT,nom}$ disabled, ODT on	Any valid except self refresh, read	3
000–101	0	$R_{TT,nom}$ enabled, ODT off	Any valid	2
000–101	1	$R_{TT,nom}$ enabled, ODT on	Any valid except self refresh, read	3
110 and 111	X	$R_{TT,nom}$ reserved, ODT on or off	Illegal	

Notes: 1. Assumes dynamic ODT is disabled (see Dynamic ODT when enabled).
2. ODT is enabled and active during most writes for proper termination, but it is not illegal for it to be off during writes.
3. ODT must be disabled during reads. The $R_{TT,nom}$ value is restricted during writes. Dynamic ODT is applicable if enabled.

Nominal ODT resistance $R_{TT,nom}$ is defined by MR1[9,6,2],as shown in Mode Register1 (MR1) Definition. The $R_{TT,nom}$termination value applies to the output pins previously mentioned. DDR3SDRAM supports multiple $R_{TT,nom}$ values based on RZQ/*n* where *n* can be 2,4,6,8, or 12 and RZQ is 240Ω. $R_{TT,nom}$ termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode.

Write accesses use $R_{TT,nom}$ if dynamic ODT ($R_{TT(WR)}$) is disabled. If $R_{TT,nom}$ is used during writes, only RZQ/2, RZQ/4, and RZQ/6 are allowed. ODT timings are summarized as well as listed in the Electrical Characteristics and AC Operating Conditions table.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in Synchronous ODTMode.

ODT Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3L Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)} \pm {}^{t}AON$	CWL + AL - 2	^{t}CK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)} \pm {}^{t}AOF$	CWL + AL - 2	^{t}CK
$^{t}AONPD$	ODT asynchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$	2–8.5	ns
$^{t}AOFPD$	ODT asynchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$	2–8.5	ns
ODTH4	ODT minimum HIGH time after ODT assertion or write (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	$4^{t}CK$	^{t}CK
ODTH8	ODT minimum HIGH time after write (BL8)	Write registration with ODT HIGH	ODT registered LOW	$6^{t}CK$	^{t}CK
^{t}AON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Electrical Characteristics and AC Operating Conditions table	ps
^{t}AOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	$0.5^{t}CK \pm 0.2^{t}CK$	^{t}CK

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3SDRAM can be changed without issuing an MRS command, essentially changing the ODT termination on the fly. With dynamic ODTR$_{TT(WR)}$) enabled, the DRAM switches from nominal ODTR$_{TT,nom}$) to dynamic ODT R$_{TT(WR)}$) when beginning a WRITE burst and subsequently switches back to nominal ODTR$_{TT,nom}$) at the completion of the WRITE burst. This requirement is supported by the dynamic ODT feature, as described below.

Dynamic ODT Special Use Case

When DDR3 devices are architect as a single rank memory array, dynamic ODT offers a special use case : the ODT ball can be wired high (via a current limiting resistor preferred) by having R$_{TT,nom}$ disabled via MR1 and R$_{TT(WR)}$ enabled via MR2. This will allow the ODT signal not to have to be routed yet the DRAM can provide ODT coverage during write accesses.

When enabling this special use case, some standard ODT spec conditions may be violated : ODT is sometimes suppose to be held low. Such ODT spec violation (ODT not LOW) is allowed under this special use case. Most not ably, if Write Leveling is used, this would appear to be a problem since R$_{TT(WR)}$ cannot be used (should be disabled) and R$_{TT(NOM)}$ should be used.

For Write leveling during this special use case, with the DLL locked, then R$_{TT(NOM)}$ may be enabled when entering Write Leveling mode and disabled when exiting Write Leveling mode. More so,R$_{TT(NOM)}$ must be enabled when enabling Write Leveling, via same MR1 load, and disabled when disablingWrite Leveling, via same MR1 load if R$_{TT(NOM)}$ is to be used.

ODT will turn-on within a delay of ODTLon+ ^{t}AON+ ^{t}MOD+ 1CK (enablingvia MR1) or turn-off within a delay of ODTL off+ ^{t}AOF+ ^{t}MOD +1CK. Asseenin the table below, between the Load Mode of MR1 and the previously specified delay, the value of ODT is uncertain. this means the DQODT termination could turn-on and then turn-off again during the period of stated uncertainty.

Write Leveling with Dynamic ODT Special Case

Begin R$_{TT,nom}$ Uncertainty	End R$_{TT,nom}$ Uncertainty	I/Os	R$_{TT,nom}$ Final State
MR1 load mode command: Enable Write Leveling and R$_{TT(NOM)}$	ODTLon + ^{t}AON + ^{t}MOD + 1CK	DQS, DQS#	Drive R$_{TT,nom}$ value
		DQs	No R$_{TT,nom}$
MR1 load mode command: Disable Write Leveling and R$_{TT(NOM)}$	ODTLoff + ^{t}AOFF + ^{t}MOD + 1CK	DQS, DQS#	No R$_{TT,nom}$
		DQs	No R$_{TT,nom}$

Functional Description

The dynamic ODT mode is enabled if either MR2[9] or MR2[10] is set to 1. Dynamic ODT is not supported during DLL disable mode so R$_{TT(WR)}$ must be disabled. The dynamic ODT function is described below:

- TwoR$_{TT}$ values are available—R$_{TT,nom}$ and R$_{TT(WR)}$.
  - The value for R$_{TT,nom}$ is preselected via MR1[9, 6, 2].
  - The value for R$_{TT(WR)}$ is preselected via MR2[10, 9].

- During DRAM operation without READ or WRITE commands, the termination is controlled.
  - Nominal termination strength $R_{TT,nom}$ is used.
  - Termination on/off timing is controlled via the ODT ball and latencies ODTL on and ODTL off.
- When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered, and if dynamic ODT is enabled, the ODT termination is controlled.
  - A latency of ODTL after the WRITE command: termination strength $R_{TT,nom}$ switches to $R_{TT(WR)}$
  - A latency of ODTLcwn 8 (for BL 8, fixed or OTF) or ODTL cwn 4 (for BC4, fixed or OTF)
    after the WRITE command: termination strength $R_{TT(WR)}$ switches back to $R_{TT,nom}$.
  - On/off termination timing is controlled via the ODT ball and determined by ODT- Lon, ODTL off, ODTH4, and ODTH8.
  - During the ^tADC transition window, the value of R_{TT} is undefined.

ODT is constrained during writes and when dynamic ODT is enabled (see the table below, Dynamic ODT Specific Parameters). ODT timings listed in the ODT Parameters table in On-Die Termination(ODT) also apply to dynamic ODT mode.

Dynamic ODT Specific Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3L Speed Bins	Unit
ODTLcnw	Change from $R_{TT,nom}$ to $R_{TT(WR)}$	Write registration	R_{TT} switched from $R_{TT,nom}$ to $R_{TT(WR)}$	WL - 2	^tCK
ODTLcwn4	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BC4)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	4^tCK + ODTL off	^tCK
ODTLcwn8	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BL8)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	6^tCK + ODTL off	^tCK
^tADC	R_{TT} change skew	ODTLcnw completed	R_{TT} transition complete	$0.5^tCK \pm 0.2^tCK$	^tCK

Mode Registers for $R_{TT,nom}$

MR1 ($R_{TT,nom}$)			$R_{TT,nom}$ (RZQ)	$R_{TT,nom}$ (Ohm)	$R_{TT,nom}$ Mode Restriction
M9	M6	M2			
0	0	0	Off	Off	n/a
0	0	1	RZQ/4	60	Self refresh
0	1	0	RZQ/2	120	
0	1	1	RZQ/6	40	
1	0	0	RZQ/12	20	Self refresh, write
1	0	1	RZQ/8	30	
1	1	0	Reserved	Reserved	n/a

Mode Registers for $R_{TT,nom}$ (Continued)

MR1 ($R_{TT,nom}$)			$R_{TT,nom}$ (RZQ)	$R_{TT,nom}$ (Ohm)	$R_{TT,nom}$ Mode Restriction
M9	M6	M2			
1	1	1	Reserved	Reserved	n/a

Note: 1. RZQ = 240Ω. If $R_{TT,nom}$ is used during WRITEs, only RZQ/2, RZQ/4, RZQ/6 are allowed.

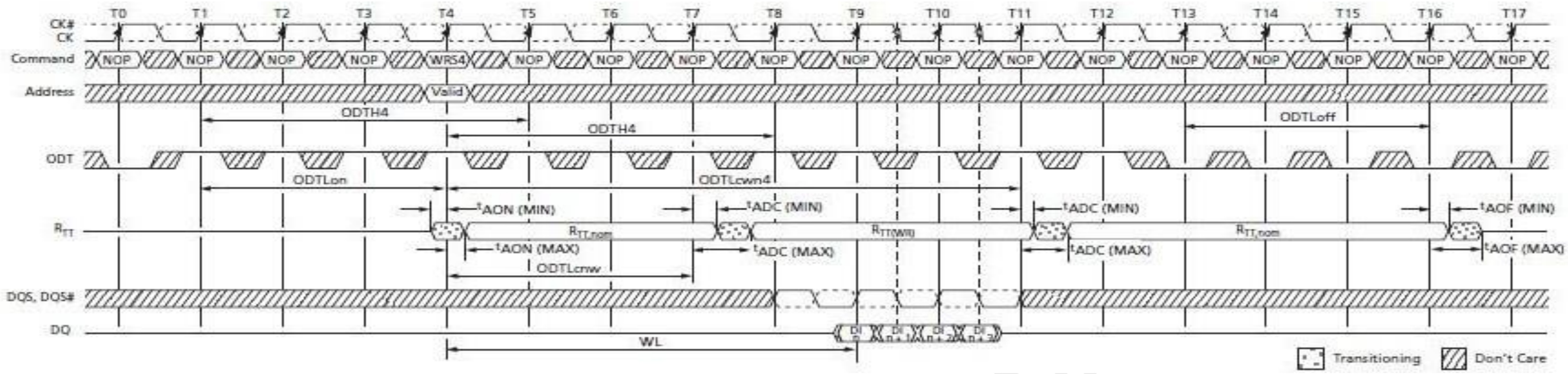
Mode Registers for $R_{TT(WR)}$

MR2 ($R_{TT(WR)}$)		$R_{TT(WR)}$ (RZQ)	$R_{TT(WR)}$ (Ohm)
M10	M9		
0	0	Dynamic ODT off: WRITE does not affect $R_{TT,nom}$	
0	1	RZQ/4	60
1	0	RZQ/2	120
1	1	Reserved	Reserved

Timing Diagrams for Dynamic ODT

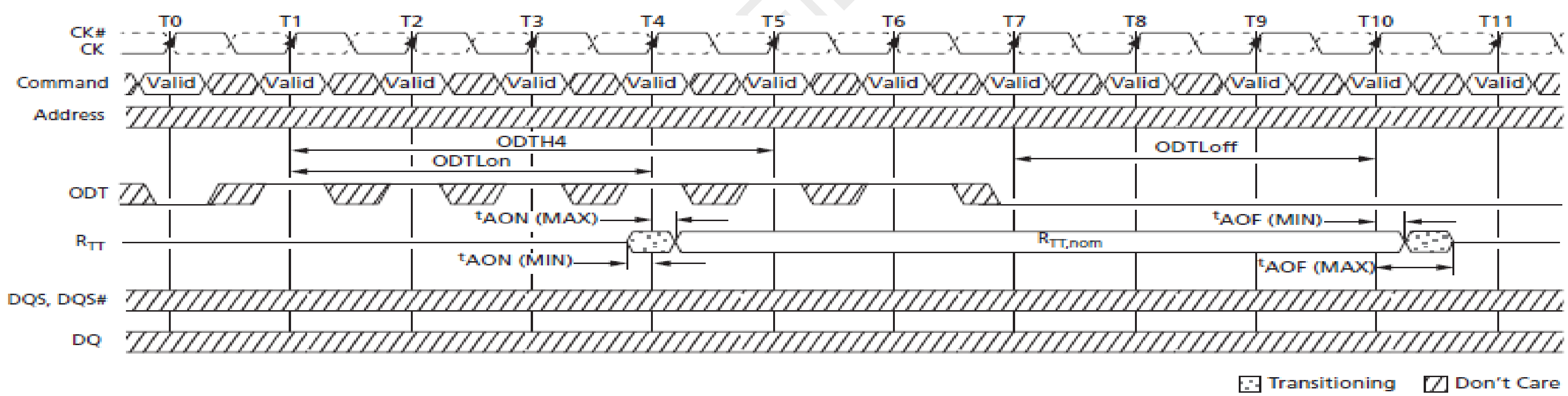
Title
Dynamic ODT: ODT Asserted Before and After the WRITE, BC4
Dynamic ODT: Without WRITE Command
Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8
Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4
Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

Dynamic ODT: ODT Asserted Before and After the WRITE, BC4



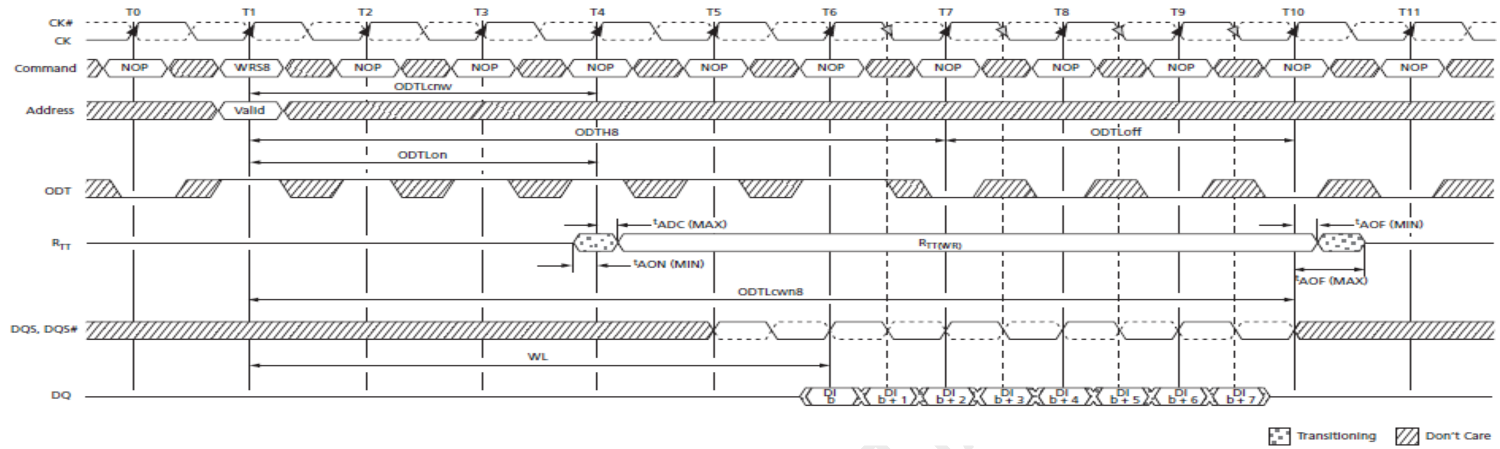
Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ and $R_{TT(WR)}$ are enabled.
2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

Dynamic ODT: Without WRITE Command



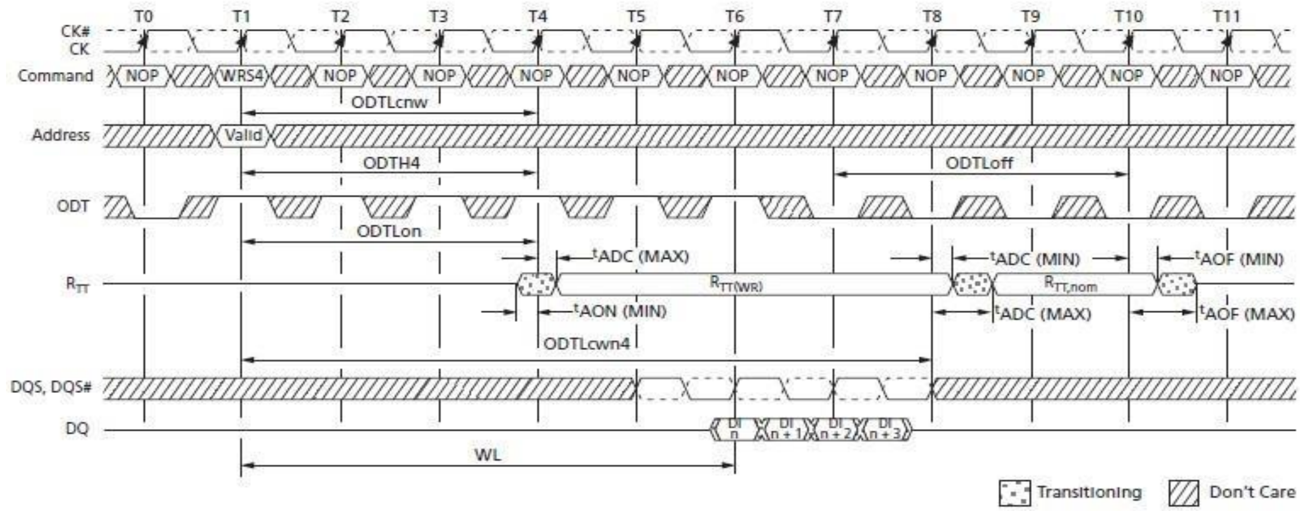
Notes: 1. AL = 0, CWL = 5. $R_{TT,nom}$ is enabled and $R_{TT(WR)}$ is either enabled or disabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW; in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8



Notes: 1. Via MRS or OTF; AL = 0, CWL = 5. If $R_{TT,nom}$ can be either enabled or disabled, ODT can be HIGH. $R_{TT(WR)}$ is enabled.
2. In this example, ODTH8 = 6 is satisfied exactly.

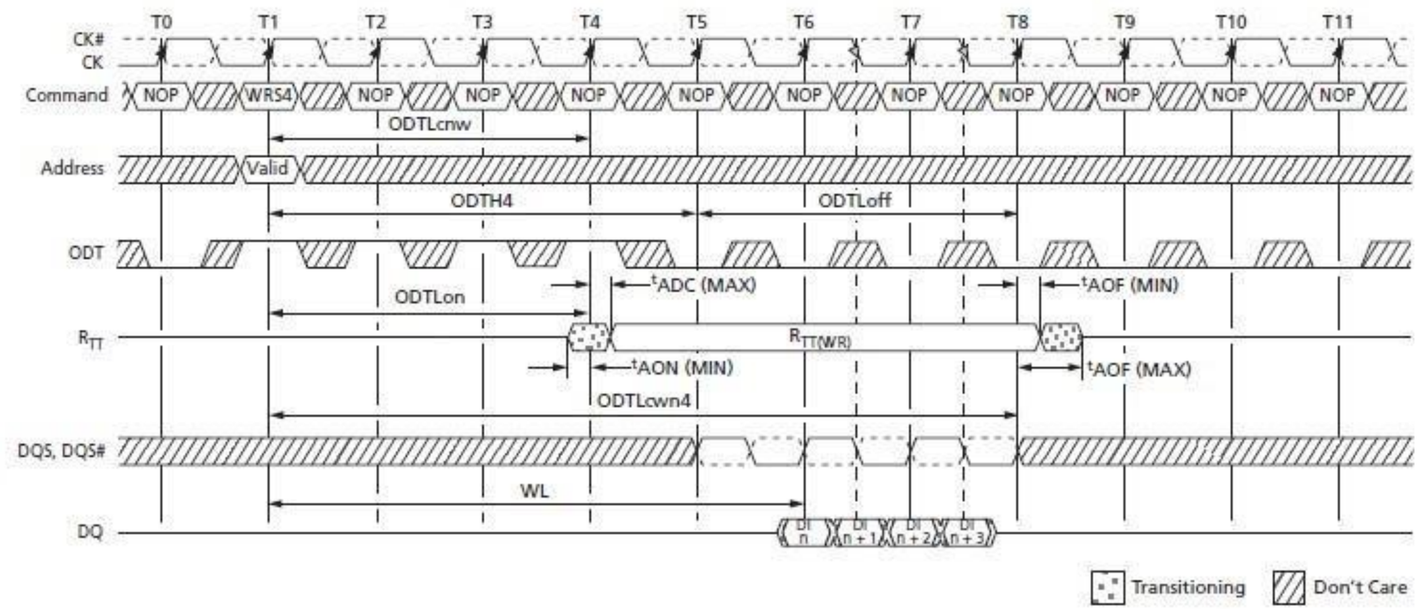
Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ and $R_{TT(WR)}$ are enabled.

2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ can be either enabled or disabled. If disabled, ODT can remain HIGH. $R_{TT(WR)}$ is enabled.

2. In this example ODTH4 = 4 is satisfied exactly.

Synchronous ODT Mode

Synchronous ODT mode is selected when ever the DLL is turned on and locked and when either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled. Based on the power-down definition, these modes are:

- Any bank active with CKE HIGH
- Refresh mode with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode (regardless of MR0[12])
- Precharge power-down mode if DLL is enabled by MR0[12] during precharge power- down

ODT Latency and Posted ODT

In synchronous ODT mode, R_{TT} turns on ODTL on clock cycles after ODT is sampled HIGH by arising clock edge and turns off ODTL off clock cycles after ODT is registered LOW by arising clock edge. The actual on/off times varies by ^{t}AON and ^{t}AOF around each clock edge. The ODT latency is tied to the WRITE latency (WL) byODTLon=WL- 2 and ODTLoff=WL- 2.

Since write latency is made up of CAS WRITE latency (CWL) and additive latency(AL), the AL programmed into the mode register (MR1[4,3]) also applies to the ODT signal. The device's internal ODT signal is delayed a number of clock cycles defined by the AL relative to the external ODT signal. Thus, ODTL on=CWL+AL-2 and ODTL off=CWL+ AL- 2.

Timing Parameters

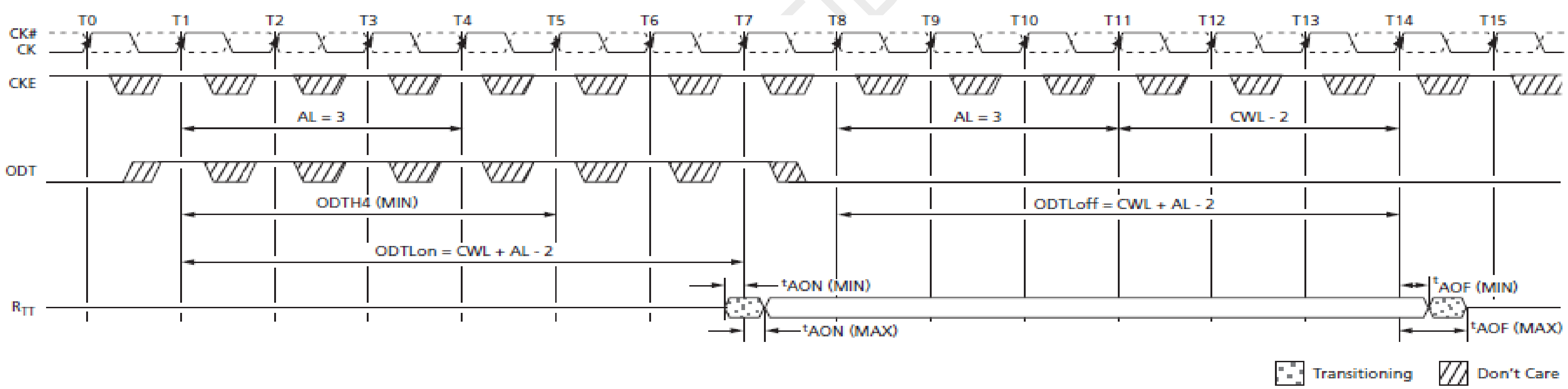
Synchronous ODT mode uses the following timing parameters: ODTLon, ODTL off, ODTH4,ODTH8,^{t}AON, and ^{t}AOF. The minimum R_{TT} turn-ontime(^{t}AON[MIN]) is the point at which the device leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turn-ontime (^{t}AON[MAX]) is the point at which ODT resistance is fully on. Both are measured relative to ODTL on. The minimum R_{TT} turn-off time(^{t}AOF[MIN]) is the point at which the device starts to turn off ODT resistance. The maximum R_{TT} turn off time(^{t}AOF[MAX]) is the point at which ODT has reached High-Z. Both are measured from ODTL off.

When ODT is asserted, it must remain HIGH until ODTH4 is satisfied. If aWRITE command is registered by the DRAM with ODT HIGH, then ODT must remain HIGH until ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command. ODTH4 and ODTH8 are measured from ODT registered HIGH to ODT registered LOW or from the registration of a WRITE command until ODT is registered LOW.

Synchronous ODT Parameters

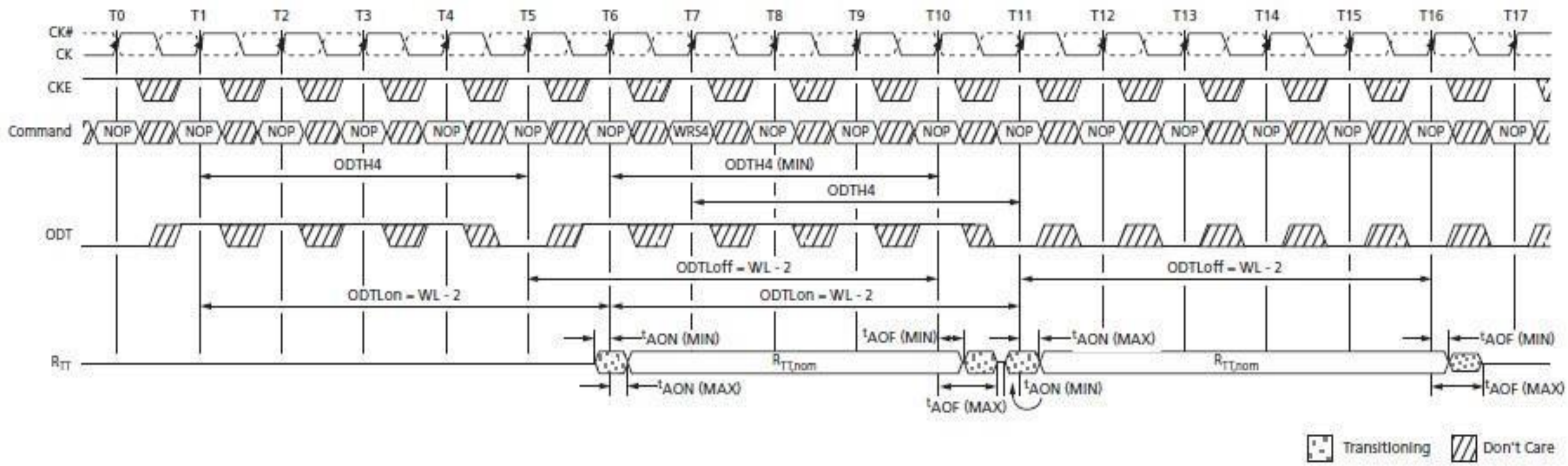
Symbol	Description	Begins at	Defined to	Definition for All DDR3L Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$ $\pm^t$AON	CWL + AL - 2	^{t}CK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$ $\pm^t$AOF	CWL +AL - 2	^{t}CK
ODTH4	ODT minimum HIGH time after ODT assertion or WRITE (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	4^{t}CK	^{t}CK
ODTH8	ODT minimum HIGH time after WRITE (BL8)	Write registration with ODT HIGH	ODT registered LOW	6^{t}CK	^{t}CK
^{t}AON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Electrical Characteristics and AC Operating Conditions table	ps
^{t}AOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	0.5^{t}CK ± 0.2^{t}CK	^{t}CK

Synchronous ODT



Note: 1. AL = 3; CWL = 5; ODTLon = WL = 6.0; ODTLoff = WL - 2 = 6. $R_{TT,nom}$ is enabled.

Synchronous ODT (BC4)



Notes: 1. WL = 7. $R_{TT,nom}$ is enabled. $R_{TT(WR)}$ is disabled.

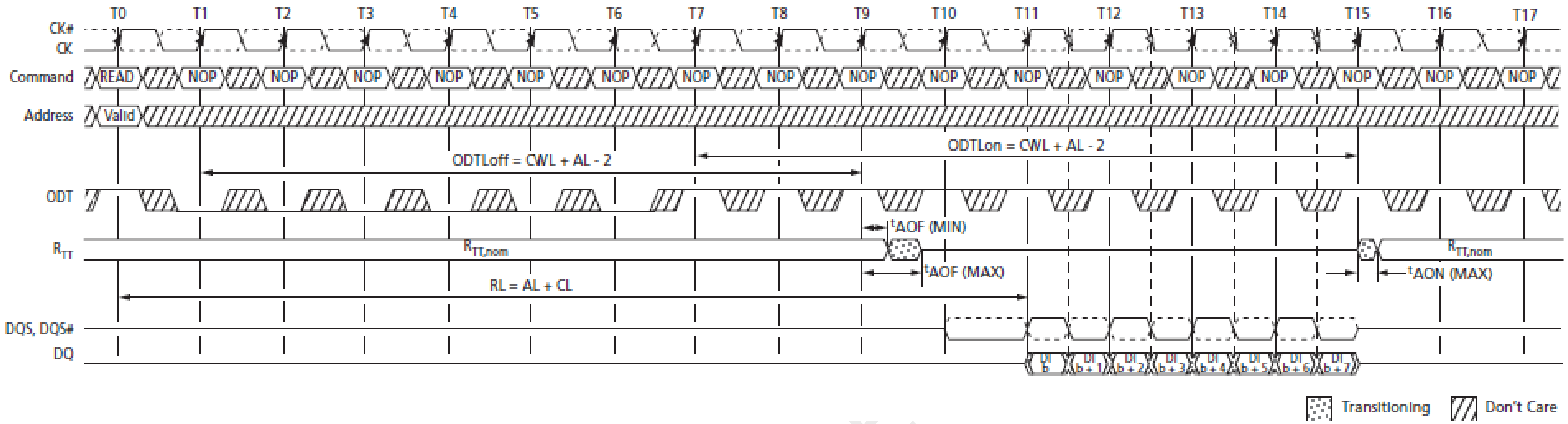
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).
3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).
4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.
5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

ODT Off During READs

Because the device cannot terminate and drive at the same time, R_{TT} must be disabled at least one-half clock cycle before the READ preamble by driving the ODTball LOW (if either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled). R_{TT} may not be enabled until the end of the postamble, as shown in the following example.

Note: ODT may be disabled earlier and enabled later than shown.

ODT During READs



note: 1. ODT must be disabled externally during READs by driving ODT LOW. For example, CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8. $R_{TT,nom}$ is enabled. $R_{TT(WR)}$ is a "Don't Care."

Asynchronous ODT Mode

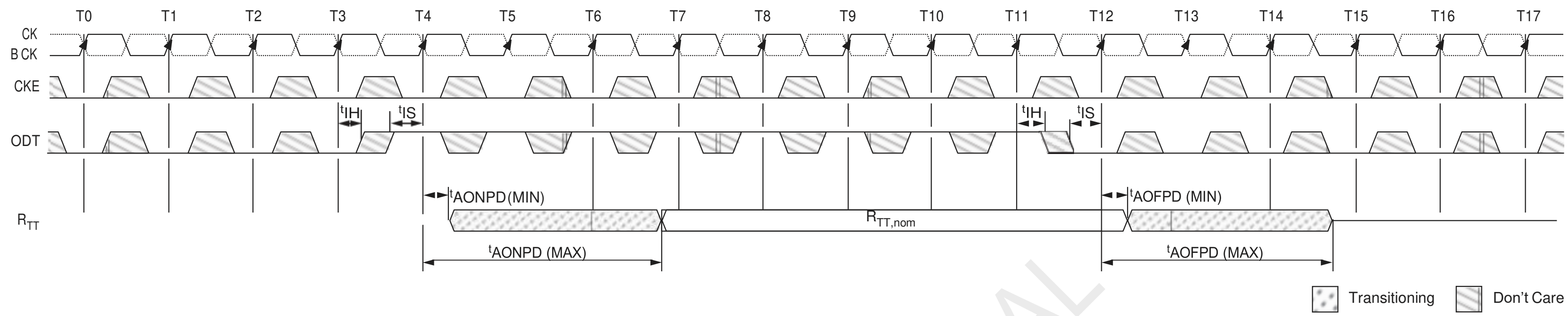
Asynchronous ODT mode is available when the DRAM runs in DLL on mode and when either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; however, the DLL is temporarily turned off in precharged power-down stand by (via MR0[12]). Additionally, ODT operates asynchronously when the DLL is synchronizing after being reset. See Power-DownMode for definition and guidance over power-down details.

In asynchronous ODT timing mode,the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls R_{TT} by analog time. The timing parameters ^{t}AONPD and ^{t}AOFPD replace ODTL on/^{t}AON and ODTLoff/^{t}AOF, respectively, when ODT operates asynchronously.

The minimum R_{TT} turn-ontime (^{t}AONPD [MIN]) is the point at which the device termination circuit leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turn- on time (^{t}AONPD [MAX]) is the point at which ODT resistance is fully on. ^{t}AONPD (MIN) and ^{t}AONPD(MAX) are measured from ODT being sampled HIGH.

The minimum R_{TT} turn-off time (^{t}AOFPD [MIN]) is the point at which the device termination circuit starts to turn off ODT resistance. Maximum R_{TT} turn-off time (^{t}AOFPD [MAX]) is the point at which ODT has reached High-Z. ^{t}AOFPD (MIN) and ^{t}AOFPD (MAX) are measured from ODT being sampled LOW.

Asynchronous ODT Timing with Fast ODT Transition



Note: 1. AL is ignored.

Asynchronous ODT Timing Parameters for All Speed Bins

Symbol	Description	Min	Max	Unit
^{t}AONPD	Asynchronous R_{TT} turn-on delay (power-down with DLL off)	2	8.5	ns
^{t}AOFPD	Asynchronous R_{TT} turn-off delay (power-down with DLL off)	2	8.5	ns

Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry)

There is a transition period around power-down entry(PDE) where the DRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in precharge power-down mode by the setting MR0[12] =0. Power-down entry begins ^{t}ANPD prior to CKE first being registered LOW, and ends when CKE is first registered LOW. ^{t}ANPD is equal to the greater of ODTLoff+ 1^{t}CK or ODTLon+1^{t}CK. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, power-down entry ends ^{t}RFC after the REFRESH command, rather than when CKE is first registered LOW . Power-down entry then becomes the greater of ^{t}ANPD and ^{t}RFC- REFRESH command to CKE registered LOW.

ODT assertion during power-down entry results in an R_{TT} change as early as the lesser of ^{t}AONPD(MIN) and ODTLon× ^{t}CK+ ^{t}AON(MIN), or as late as the greater of ^{t}AONPD (MAX) and ODTLon× ^{t}CK+ ^{t}AON(MAX). ODT de-assertion during power-down entry can result in an R_{TT} change as early as the lesser of ^{t}AOFPD (MIN) and ODTLoff× ^{t}CK+ ^{t}AOF(MIN),or as late as the greater of ^{t}AOFPD(MAX) and ODTLoff × ^{t}CK + ^{t}AOF(MAX).
summarizes these parameters.

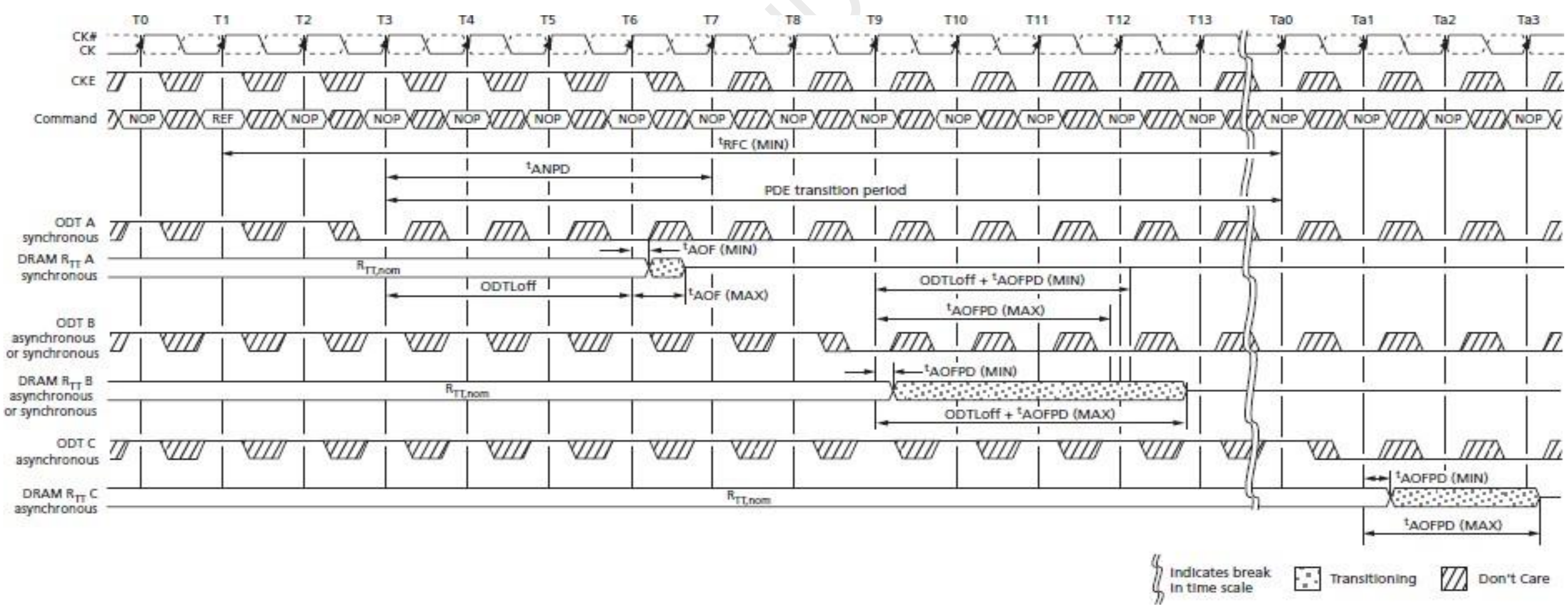
If AL has a large value, the uncertainty of the state of R_{TT} becomes quite large. This is because ODT Lon and ODTLoff are derived from the WL; and WL is equal to CWL+AL. shows three different cases:

- ODT_A: Synchronous behavior before ^{t}ANPD.
- ODT_B: ODTstate changes during the transitionperiodwith ^{t}AONPD(MIN) < ODTLon × ^{t}CK + ^{t}AON (MIN) and ^{t}AONPD (MAX) > ODTLon × ^{t}CK + ^{t}AON (MAX).
- ODT_C: ODT state changes after the transition period with asynchronous behavior.

ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period

Description	Min	Max
Power-down entry transition period (power-down entry)	Greater of: ^{t}ANPD or ^{t}RFC - refresh to CKE LOW	
Power-down exit transition period (power-down exit)	^{t}ANPD + ^{t}XPDLL	
ODT to R_{TT} turn-on delay (ODTLon = WL - 2)	Lesser of: ^{t}AONPD (MIN) (2ns) or ODTLon × ^{t}CK + ^{t}AON (MIN)	Greater of: ^{t}AONPD (MAX) (8.5ns) or ODTLon × ^{t}CK + ^{t}AON (MAX)
ODT to R_{TT} turn-off delay (ODTLoff = WL - 2)	Lesser of: ^{t}AOFPD (MIN) (2ns) or ODTLoff × ^{t}CK + ^{t}AOF (MIN)	Greater of: ^{t}AOFPD (MAX) (8.5ns) or ODTLoff × ^{t}CK + ^{t}AOF (MAX)
^{t}ANPD	WL - 1 (greater of ODTLoff + 1 or ODTLon + 1)	

Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry



Note: 1. AL = 0; CWL = 5; ODTL(off) = WL - 2 = 3.

Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit)

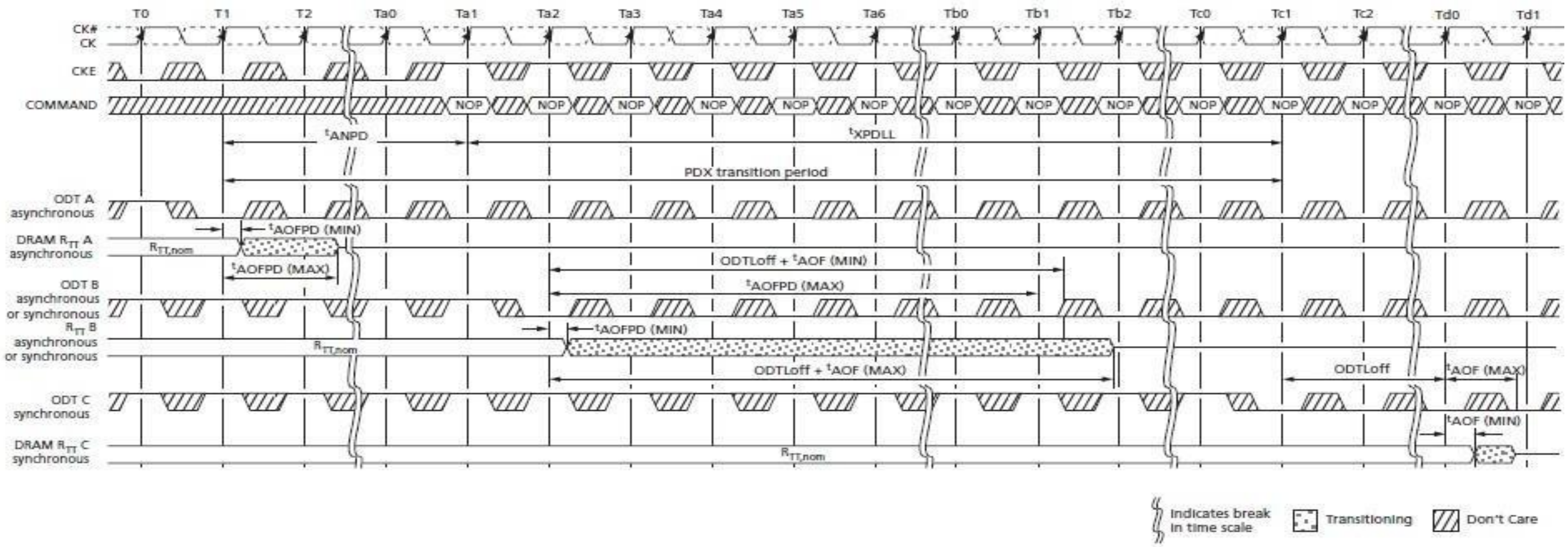
The DRAM's ODT can exhibite it her asynchronous or synchronous behavior during power- down exit(PDX). This transition period occurs if the DLL is selected to be off when in precharge power-down mode bysetting MR0[12] to 0. Power-down exit begins ^tANPD prior to CKE first being registered HIGH, and ends ^tXPDLL after CKE is first registered HIGH.^tANPD is equal to the greater of ODTLoff+ 1^tCKor ODTLon+ 1^tCK. The transition period is ^tANPD + ^tXPDLL.

ODT assertion during power-down exit results in an R_{TT} change as early as the lesser of ^tAONPD (MIN) and ODTLon × ^tCK + ^tAON(MIN), or as late as the greaterof ^tAONPD (MAX) and ODTLon×^tCK+ ^tAON(MAX).ODT de-assertion during power-down exit may result in an R_{TT} change as early as the lesser of ^tAOFPD(MIN) and ODTLoff×^tCK+ ^tAOF(MIN), or as late as the greater of ^tAOFPD(MAX) and ODTLoff×^tCK+^tAOF(MAX). summarizes these parameters.

If AL has a large value,the uncertainty of the R_{TT} state becomes quite large. This is because ODTL on and ODTL off are derived from WL, and WL is equal to CWL+AL. shows three different cases:

- ODT C: Asynchronous behavior before ^tANPD.
- ODTB : ODT state changes during the transition period, with^tAOFPD(MIN) <ODTL- off× ^tCK + ^tAOF(MIN), and ODTLoff× ^tCK + ^tAOF(MAX) > ^tAOFPD (MAX).
- ODT A: ODT state changes after the transition period with synchronous response.

Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit



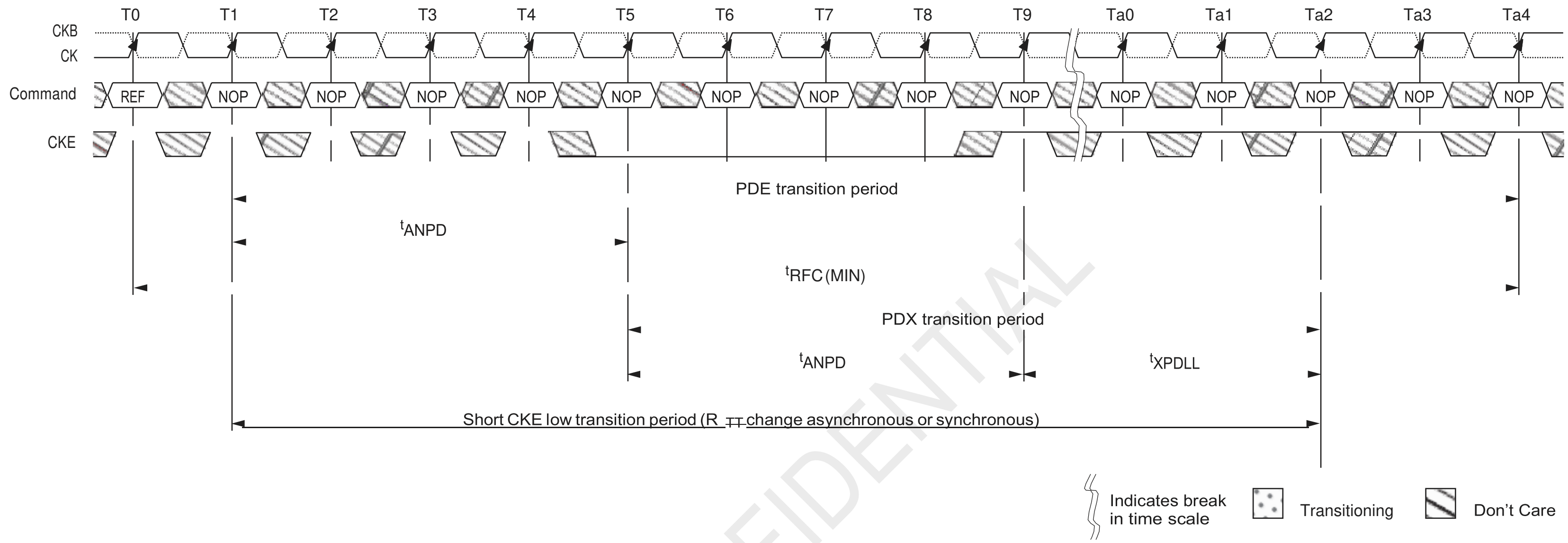
Note: 1. CL = 6; AL = CL - 1; CWL = 5; ODTLoff = WL - 2 = 8.

Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse)

If the time in the precharge power-down or idle states is very short (short CKE LOW pulse),the power-down entry and power-down exit transition periods overlap.When overlap occurs, the response of the DRAM's R_{TT} to a change in the ODT state can be synchronous or asynchronous from the start of the power-down entry transition period to the end of the power-down exit transition period, even if the entry period ends later than the exit period.

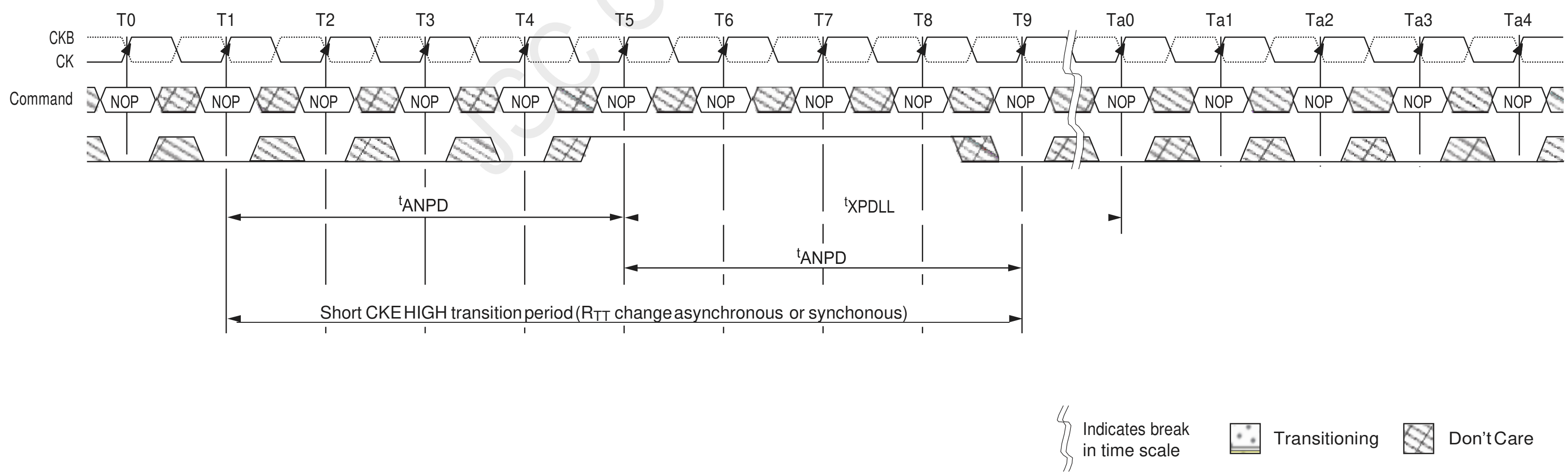
If the time in the idle state is very short (short CKE HIGH pulse), the power-down exit andpower-down entry transition periods overlap.When this overlap occurs, the response of the DRAM's R_{TT} to a change in the ODT state may be synchronous or asynchronous from the start of power-down exit transition period to the end of the power- down entry transition period.

Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping



Note: 1. AL = 0, WL = 5, ^{t}ANPD = 4.

Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping



Note: 1. AL = 0, WL = 5, ^{t}ANPD = 4.