MIC333/2333

23 µA, 300 kHz Zero-Drift Operational Amplifiers

Features

- High DC Precision:
  - Offset Voltage: V_{OS} = ±8 µV (maximum)
  - Offset Voltage Drift: V_{OS} Drift = ±0.03 µV/°C (maximum)
  - Open-Loop Gain: A_{OL} = 120 dB (minimum, V_{DD} = 5.5V)
  - Power Supply Rejection Ratio (PSRR): PSRR = 120 dB (minimum, V_{DD} = 5.5V)
  - Common-Mode Rejection Ratio (CMRR): CMRR = 120 dB (minimum, V_{DD} = 5.5V)
  - Input Noise Voltage: E_{ni} = 1 μV_{P-P} (typical, f = 0.1 Hz to 10 Hz)
- Low Power and Supply Voltages:
  - Quiescent Current per amplifier: I_Q = 23 µA/amplifier (typical)
  - Supply Voltage Range: +1.8V to +5.5V
- Rail-to-Rail Input/Output (I/O)
- Gain Bandwidth Product: GBWP = 300 kHz (typical)
- Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C
- Available Package Options:
  - Single Operational Amplifier: MIC333
  - Dual Operational Amplifier: MIC2333
- Packaging:
  - 5-Lead SC70 (MIC333 only)
  - 5-Lead SOT-23 (MIC333 only)
  - 8-Lead MSOP (MIC2333 only)
- Automotive Qualified (AEC Q100, Grade 1)

Typical Applications

- Sensor Conditioning
- Portable Electronics
- Medical Instrumentation
- Temperature Measurement
- DC Offset Correction
- Automotive Electronics

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Analog Demonstration and Evaluation Boards
- Application Notes

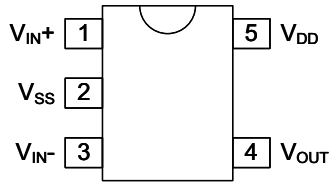
General Description

The MIC333/2333 family of operational amplifiers offers input offset voltage correction at the cost of very low offset and offset drift. These amplifiers are low power devices with a typical gain bandwidth product (GBWP) of 300 kHz. Additionally, they are unity gain stable, without $1/f$ noise and have good power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). MIC333/2333 devices operate with a single supply voltage as low as +1.8V, while drawing 23 µA/amplifier (typical) of quiescent current.

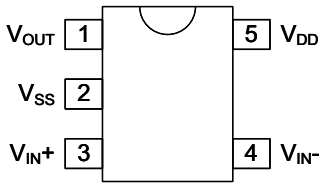
Designed using an advanced CMOS process, these zero-drift operational amplifiers are offered in single (MIC333) and dual (MIC2333) packages.

Pin Configuration

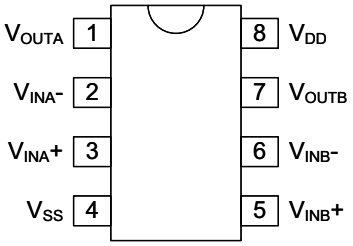
MIC333
5-Lead SC70



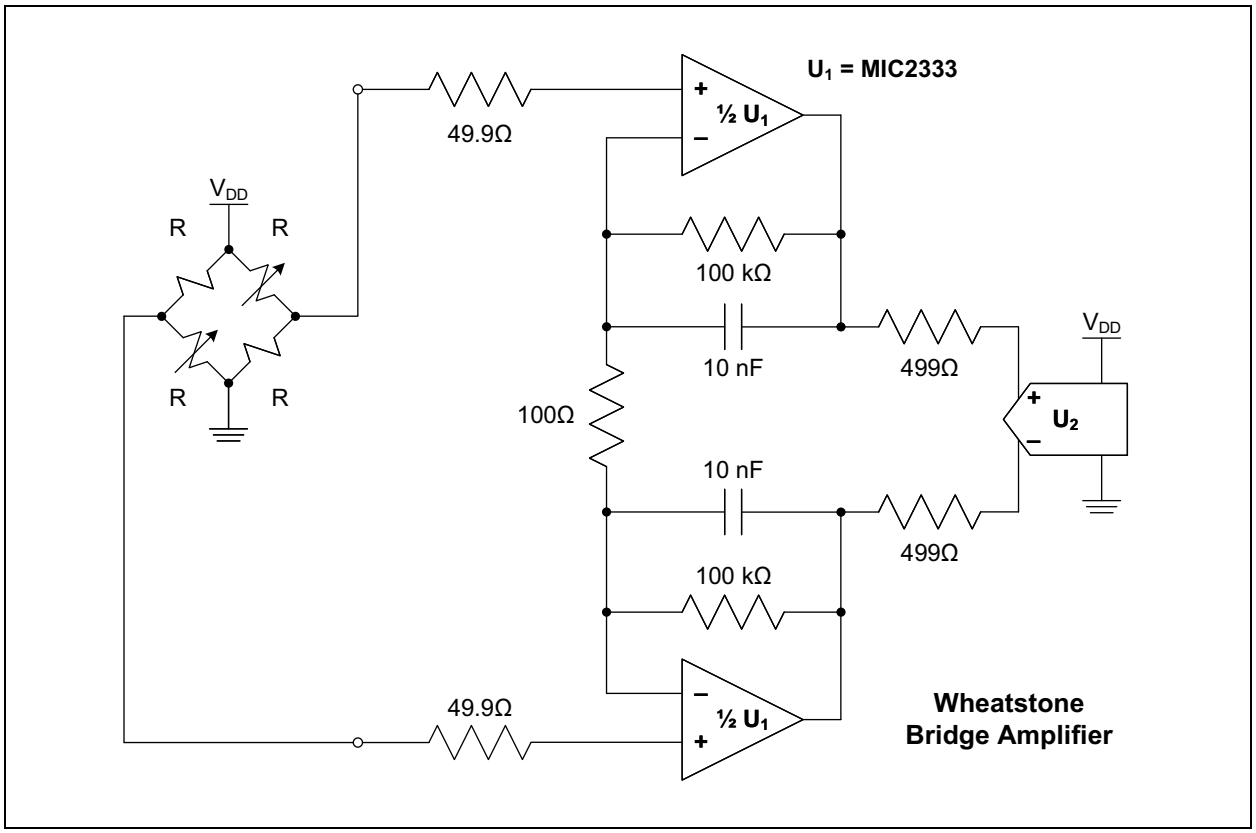
MIC333
5-Lead SOT-23



MIC2333
8-Lead MSOP



Typical Application Circuit



Key Performance Plots

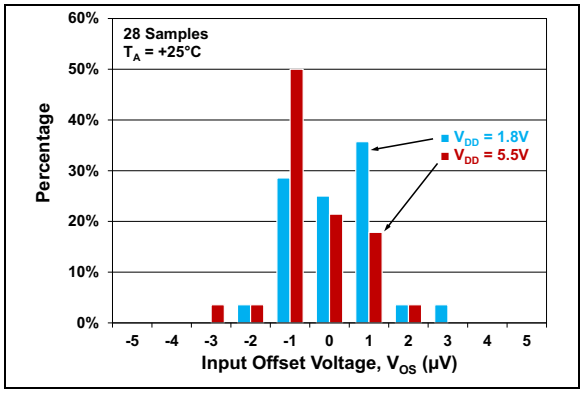


FIGURE 1: *Input Offset Voltage.*

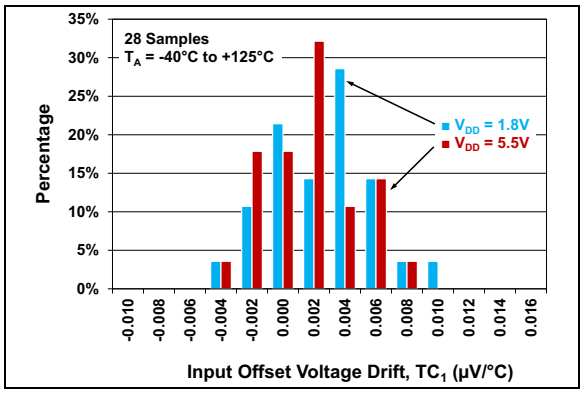


FIGURE 2: *Input Offset Voltage Drift.*

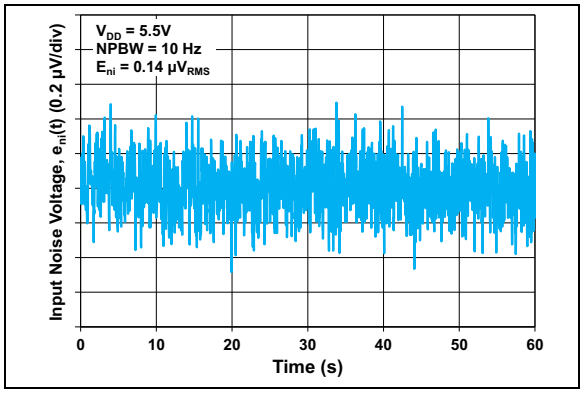


FIGURE 3: *Input Noise vs. Time, 10 Hz Filter and V_{DD} = 5.5V.*

1.0 ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings(†)

$V_{DD} – V_{SS}$ 6.5V
Current at Input Pins . . . . . ±2 mA
Analog Inputs (V_{IN}+ and V_{IN}-)(*) . . . . . V_{SS} – 1V to V_{DD} + 1V
All Other Inputs and Outputs . . . . . V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage . . . . . $|V_{DD} – V_{SS}|$
Output Short Circuit Current . . . . . Continuous
Current at Output and Supply Pins . . . . . ±30 mA
Storage Temperature (T_{STG}) . . . . . -65°C to +150°C
Maximum Junction Temperature (T_J) . . . . . +150°C
Electrostatic Discharge (ESD) Protection on All Pins (HBM, CDM, MM) . . . . . ≥ 2 kV, 1.5 kV, 400V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

* For more details, see **Section 4.2.1, "Rail-to-Rail Inputs"**.

1.2 Electrical Characteristics

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Standard Operating Conditions: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF (refer to Figure 1-4 and Figure 1-5).

Parameter	Symbol	Min.	Typical	Max.	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	12	23	34	µA	I_O = 0A
POR Trip Voltage	V_{POR}	0.9	—	1.6	V	
Input Offset						
Input Offset Voltage	V_{OS}	-8	—	+8	µV	T_A = +25°C
Input Offset Voltage Linear Temperature Coefficient	TC_1	-0.03	—	+0.03	µV/°C	T_A = -40°C to +125°C (**Note 1**)
Input Offset Voltage Quadratic Temperature Coefficient	TC_2	—	±0.05	—	nV/°C^2	T_A = -40°C to +125°C
Input Offset Aging	ΔV_{OS}	—	0.14	—	μV_{RMS}	After 408 hours at T_A = +150°C
Power Supply Rejection	PSRR	120	135	—	dB	
Input Bias Current and Impedance (Note 2)						
Input Bias Current	I_B	—	+5	—	pA	T_A = +5°C
Input Bias Current across Temperature	I_B	—	+20	—	pA	T_A = +85°C
	I_B	0	+2.9	+5	nA	T_A = +125°C
Input Offset Current	I_{OS}	—	±130	—	pA	T_A = +5°C
Input Offset Current across Temperature	I_{OS}	—	±140	—	pA	T_A = +85°C
	I_{OS}	-1	±0.4	+1	nA	T_A = +125°C

Note 1: For design guidance only. Not production tested.
2: For more details, see **Section 4.3.5, "Input Bias Currents"**.
3: Figure 2-16 shows how V_{CML} and V_{CMH} change across temperature.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Standard Operating Conditions: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF (refer to Figure 1-4 and Figure 1-5).						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Input Bias Current and Impedance (continued)						
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range Low	V_{CML}	—	—	V_{SS} – 0.15	V	**Note 3**
Common Mode Input Voltage Range High	V_{CMH}	V_{DD} + 0.2	—	—	V	**Note 3**
Common Mode Rejection	CMRR	110	125	—	dB	V_{DD} = 1.8V, V_{CM} = -0.15V to +2V (**Note 3**)
		120	135	—	dB	V_{DD} = 5.5V, V_{CM} = -0.15V to +5.7V (**Note 3**)
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	103	125	—	dB	V_{DD} = 1.8V, V_{OUT} = +0.3V to +1.6V
		120	135	—	dB	V_{DD} = 5.5V, V_{OUT} = +0.3V to +5.3V
Output						
Minimum Output Voltage Swing	V_{OL}	V_{SS}	V_{SS} + 14	V_{SS} + 45	mV	R_L = 10 kΩ, G = +2, 0.5V Input Overdrive
		—	V_{SS} + 1.4	—	mV	R_L = 100 kΩ, G = +2, 0.5V Input Overdrive
Maximum Output Voltage Swing	V_{OH}	V_{DD} – 45	V_{DD} – 14	V_{DD}	mV	R_L = 10 kΩ, G = +2, 0.5V Input Overdrive
		—	V_{DD} – 1.4	—	mV	R_L = 100 kΩ, G = +2, 0.5V Input Overdrive
Output Short Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±21	—	mA	V_{DD} = 5.5V

Note 1: For design guidance only. Not production tested.

2: For more details, see **Section 4.3.5, "Input Bias Currents"**.

3: Figure 2-16 shows how V_{CML} and V_{CMH} change across temperature.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Standard Operating Conditions: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF (refer to Figure 1-4 and Figure 1-5).

Parameter	Symbol	Min.	Typical	Max.	Units	Conditions
Amplifier AC Response						
Gain Bandwidth Product	GBWP	—	300	—	kHz	
Slew Rate	SR	—	0.13	—	V/µs	
Phase Margin	PM	—	70	—	°	G = +1
Amplifier Noise Response						
Input Noise Voltage	E_{ni}	—	0.33	—	μV_{P-P}	f = 0.01 Hz to 1 Hz
		—	1	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	50	—	nV/√Hz	f < 2 kHz
Input Noise Current Density	i_{ni}	—	6.5	—	fA/√Hz	
Amplifier Distortion (Note 1)						
Inter-Modulation Distortion	IMD	—	52	—	μV_{PK}	V_{CM} tone = 50 mV_{PK} at 100 Hz, G_N = +1
Amplifier Step Response						
Start Up Time	t_{STR}	—	2	—	ms	G = +1, 0.1% V_{OUT} settling (**Note 2**)
Offset Correction Settling Time	t_{STL}	—	100	—	µs	G = +1, V_{IN} step of 2V, V_{OS} within 100 µV of its final value
Offset Overdrive Recovery Time	t_{ODR}	—	120	—	µs	G = -10, ±0.5V input overdrive to V_{DD}/2, V_{IN} 50% point to V_{OUT} 90% point (**Note 3**)

Note 1: These parameters were characterized using the circuit shown in Figure 1-6. In Figure 2-29 and Figure 2-30, there is an inter-modulation distortion (IMD) tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

2: High gains behave differently. For more details, see **Section 4.3.3, "Offset at Power-up"**.

3: t_{ODR} includes some uncertainty due to clock edge timing.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Standard Operating Conditions: Unless otherwise indicated,

Parameter	Symbol	Min.	Typical	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_{OP}	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_{STG}	-65	—	+150	°C	
Junction-to-Ambient Thermal Package Resistances						
Thermal Resistance: 5-Lead SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance: 5-Lead SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance: 8-Lead MSOP	θ_{JA}	—	211	—	°C/W	

Note 1: Operation must not cause T_J to exceed the specified Maximum Junction Temperature (+150°C).

1.3 Timing Diagrams

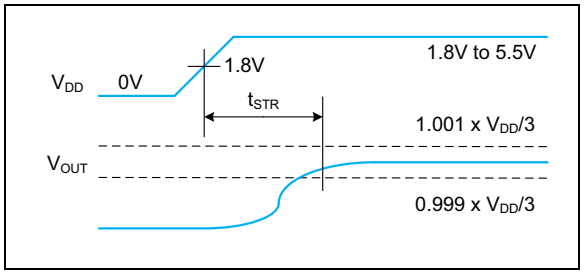


FIGURE 1-1: *Amplifier Start-up.*

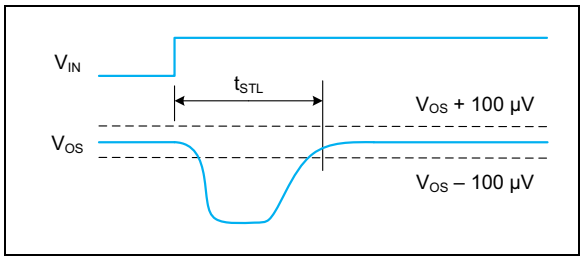


FIGURE 1-2: *Offset Correction Settling Time.*

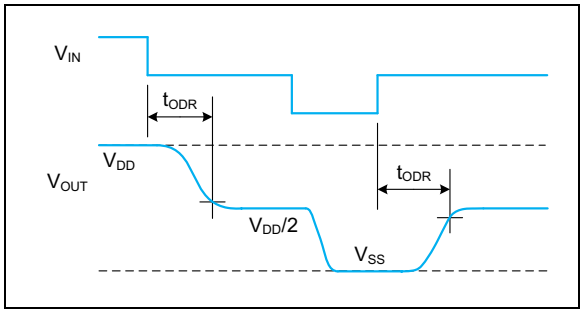


FIGURE 1-3: *Output Overdrive Recovery.*

1.4 Test Circuits

Figure 1-4 and Figure 1-5 show the circuits used for most DC and AC tests. Locate the bypass capacitors as detailed in **Section 4.3.10, "Supply Bypassing and Filtering"**. To minimize bias current effects, resistor R_N must be equal to the parallel equivalent of resistors R_F and R_G: $1/R_N = 1/R_F + 1/R_G$.

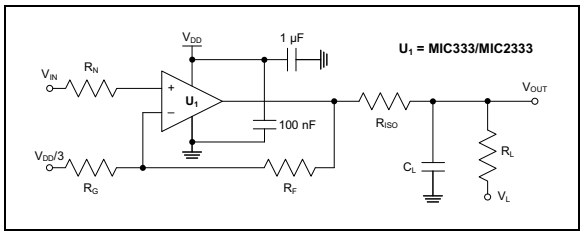


FIGURE 1-4: *AC and DC Test Circuit for Most Noninverting Gain Conditions.*

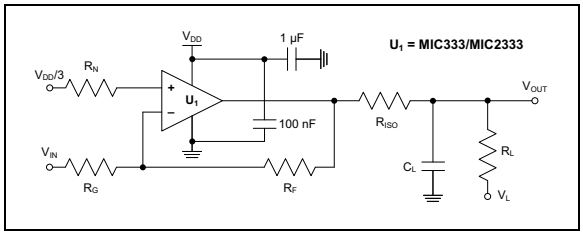


FIGURE 1-5: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

The circuit shown in Figure 1-6 tests the dynamic behavior of the input: inter-modulation distortion (IMD), start-up time (t_{STR}), offset correction settling time (t_{STL}) and output overdrive recovery time (t_{ODR}).

The potentiometer balances the resistor network: V_{OUT} must equal V_{REF} at DC. The common mode input voltage of the operational amplifier is $V_{CM} = V_{IN}/2$. The error at the input (V_{ERR}) appears at V_{OUT} with a noise gain of 10 V/V.

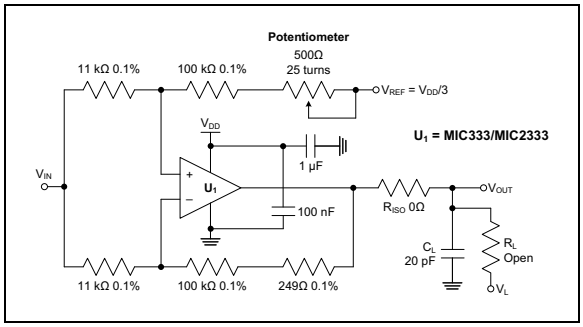


FIGURE 1-6: *Test Circuit for Dynamic Input Behavior.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

2.1 DC Input Precision

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

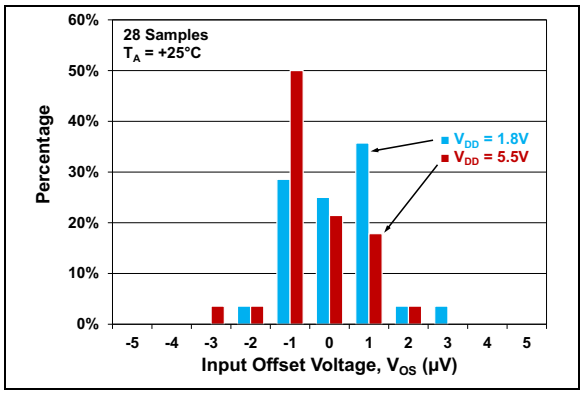


FIGURE 2-1: *Input Offset Voltage.*

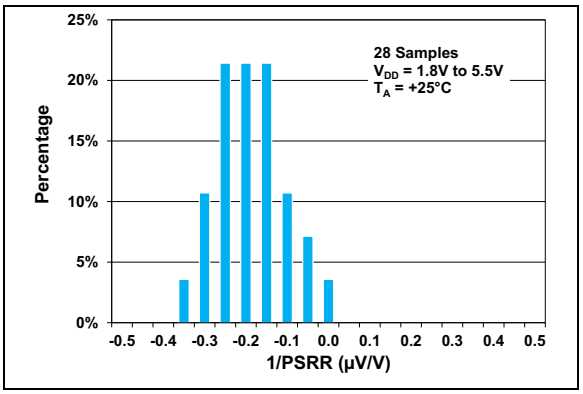


FIGURE 2-4: *Power Supply Rejection Ratio.*

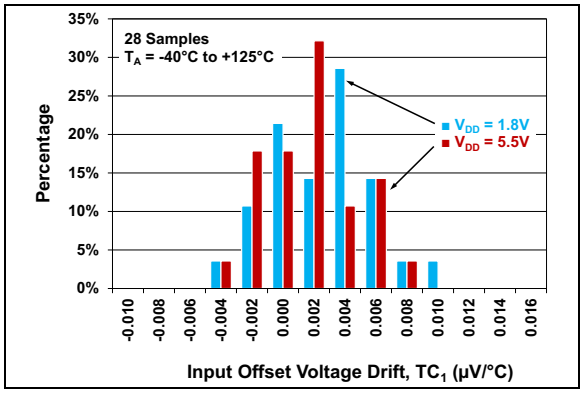


FIGURE 2-2: *Input Offset Voltage Drift.*

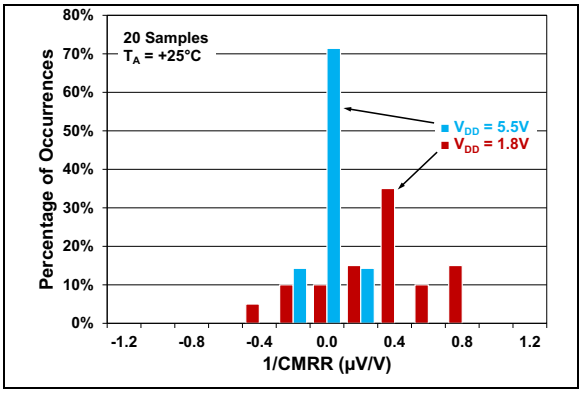


FIGURE 2-5: *Common Mode Rejection Ratio.*

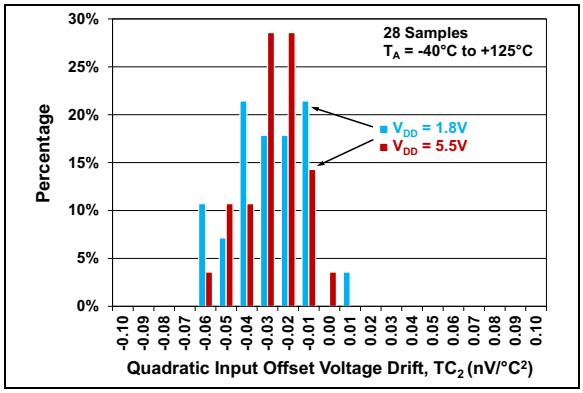


FIGURE 2-3: *Input Offset Voltage Quadratic Temperature Coefficient.*

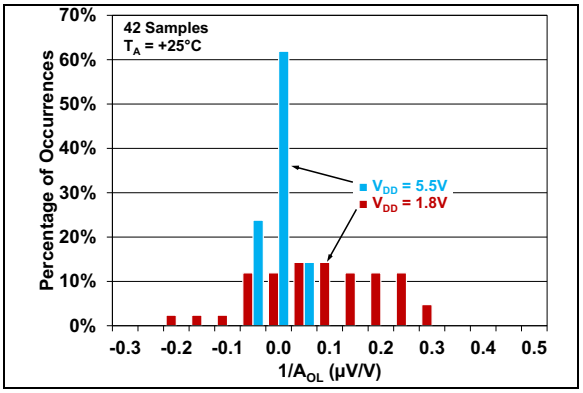


FIGURE 2-6: *DC Open-Loop Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

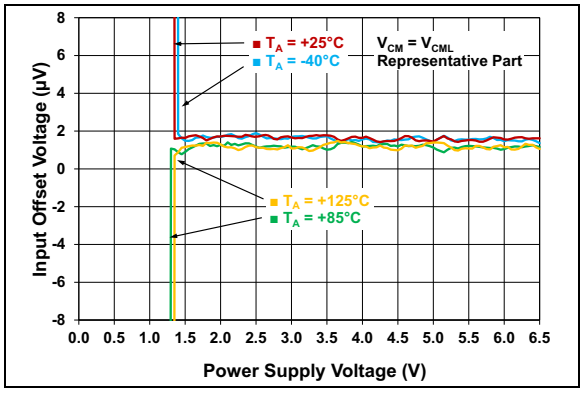


FIGURE 2-7: *Input Offset Voltage vs. Power Supply Voltage, V_{CM} = V_{CML}.*

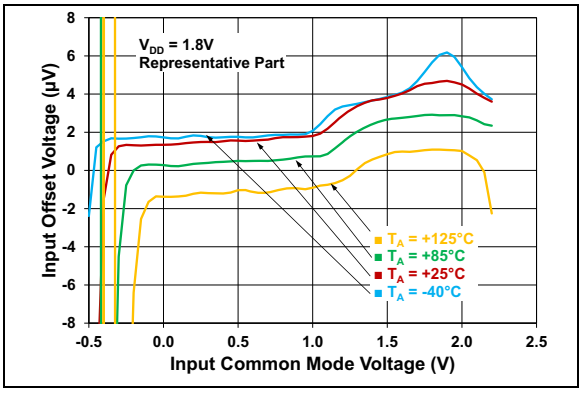


FIGURE 2-10: *Input Offset Voltage vs. Common Mode Voltage, V_{DD} = 1.8V.*

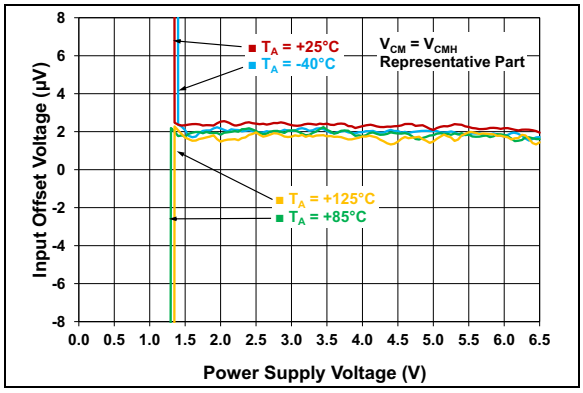


FIGURE 2-8: *Input Offset Voltage vs. Power Supply Voltage, V_{CM} = V_{CMH}.*

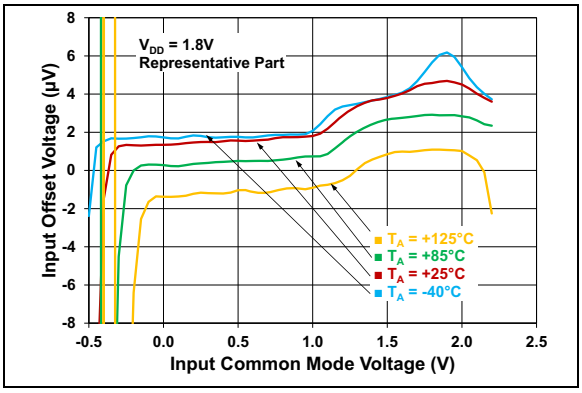


FIGURE 2-11: *Input Offset Voltage vs. Common Mode Voltage, V_{DD} = 5.5V.*

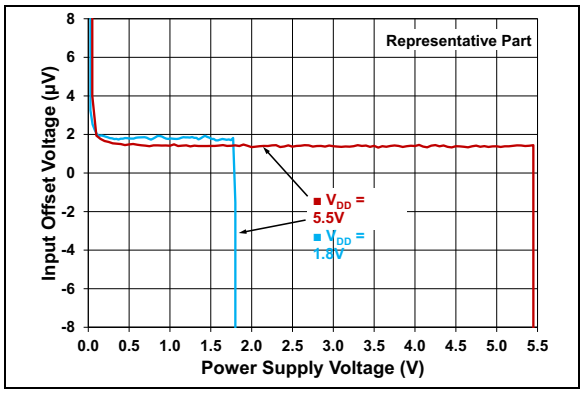


FIGURE 2-9: *Input Offset Voltage vs. Output Voltage.*

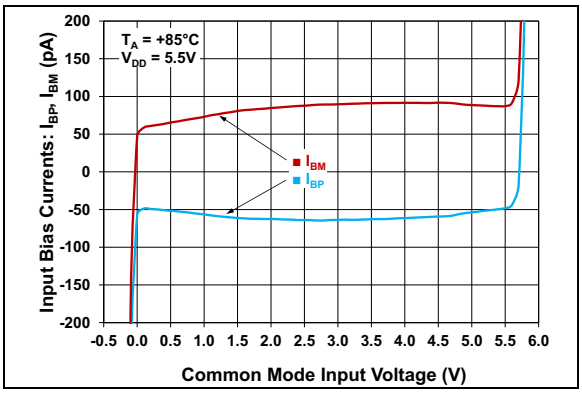


FIGURE 2-12: *Noninverting and Inverting Input Bias Currents vs. Common Mode Input Voltage, T_A = +85°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

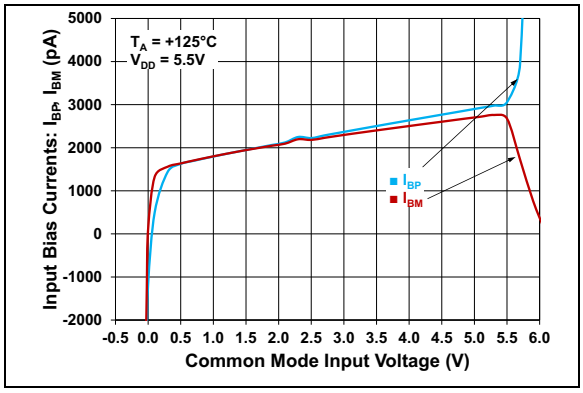


FIGURE 2-13: *Noninverting and Inverting Input Bias Currents vs. Common Mode Input Voltage, T_A = +125°C.*

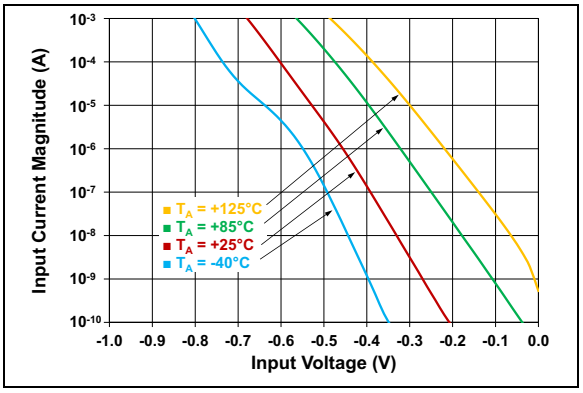


FIGURE 2-15: *Input Bias Current vs. Input Voltage (below V_{SS}).*

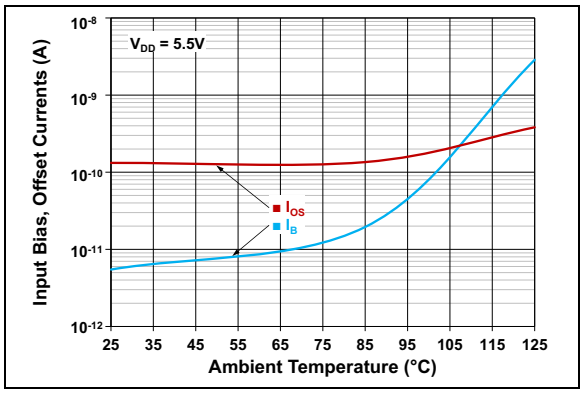


FIGURE 2-14: *Input Bias and Offset Currents vs. Ambient Temperature, V_{DD} = +5.5V.*

2.2 Other DC Voltages and Currents

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

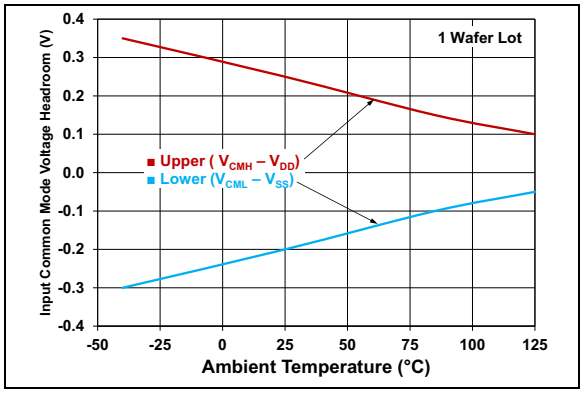


FIGURE 2-16: *Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.*

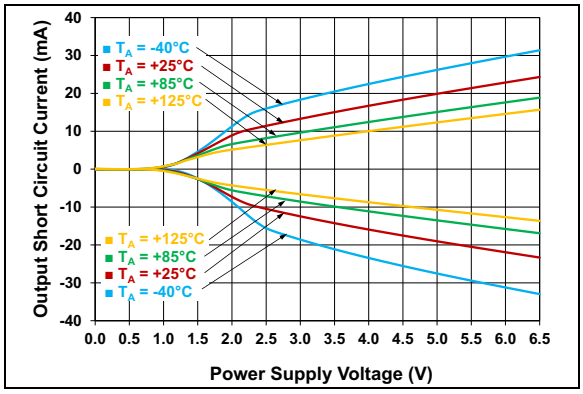


FIGURE 2-19: *Output Short Circuit Current vs. Power Supply Voltage.*

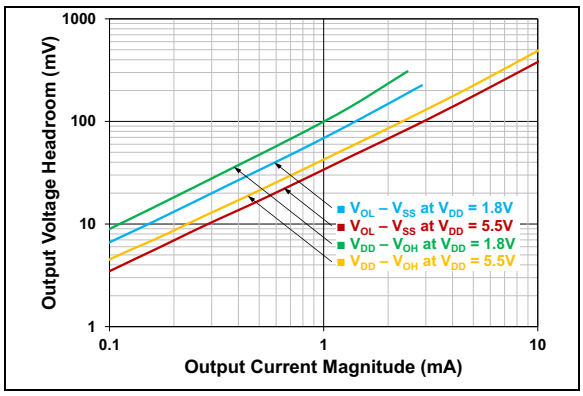


FIGURE 2-17: *Output Voltage Headroom vs. Output Current.*

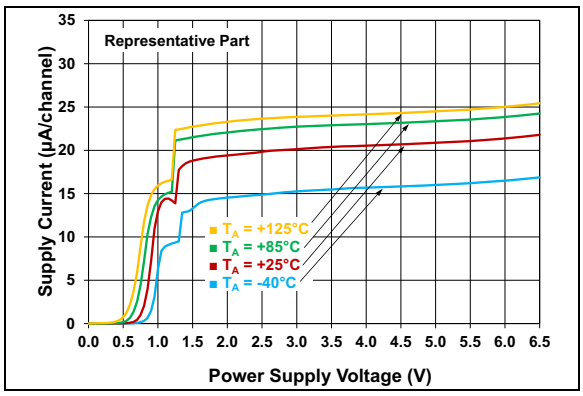


FIGURE 2-20: *Supply Current vs. Power Supply Voltage.*

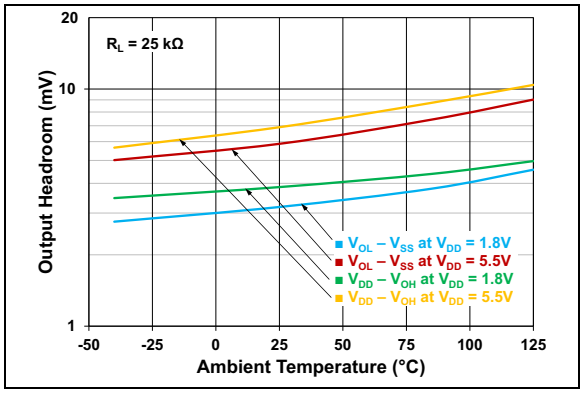


FIGURE 2-18: *Output Voltage Headroom vs. Ambient Temperature.*

2.3 Frequency Response

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

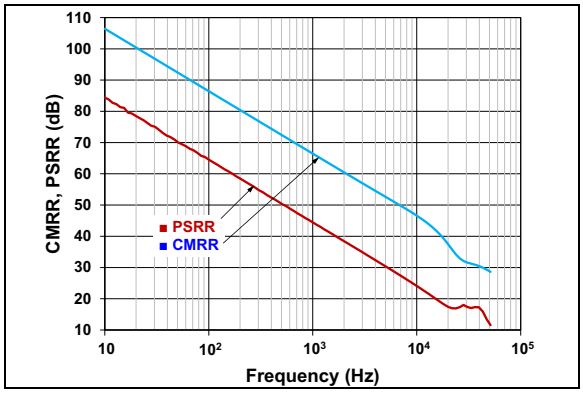


FIGURE 2-21: *CMRR and PSRR vs. Frequency.*

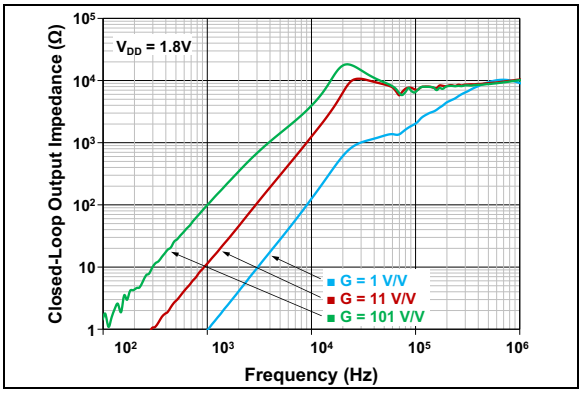


FIGURE 2-24: *Closed-Loop Output Impedance vs. Frequency, V_{DD} = 1.8V.*

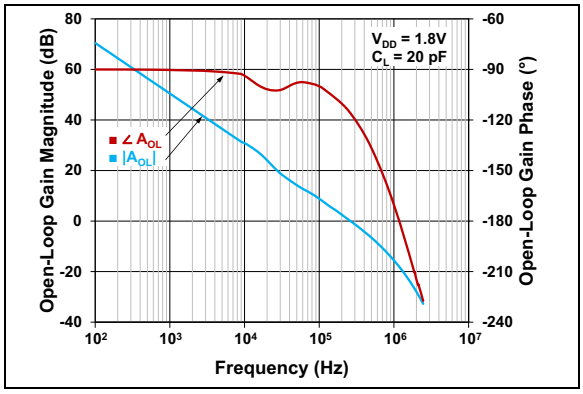


FIGURE 2-22: *Open-Loop Gain vs. Frequency, V_{DD} = 1.8V.*

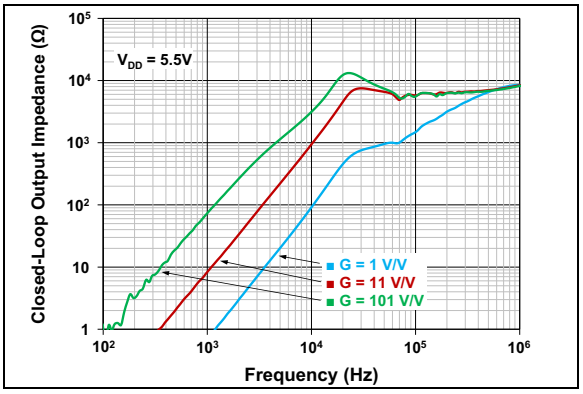


FIGURE 2-25: *Closed-Loop Output Impedance vs. Frequency, V_{DD} = 5.5V.*

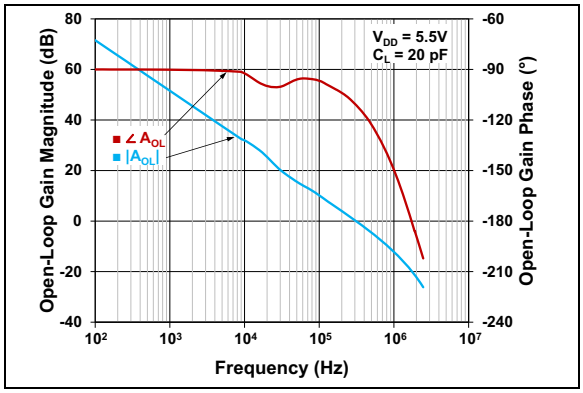


FIGURE 2-23: *Open-Loop Gain vs. Frequency, V_{DD} = 5.5V.*

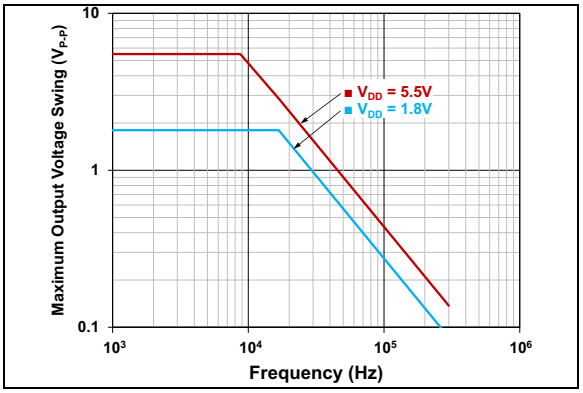


FIGURE 2-26: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

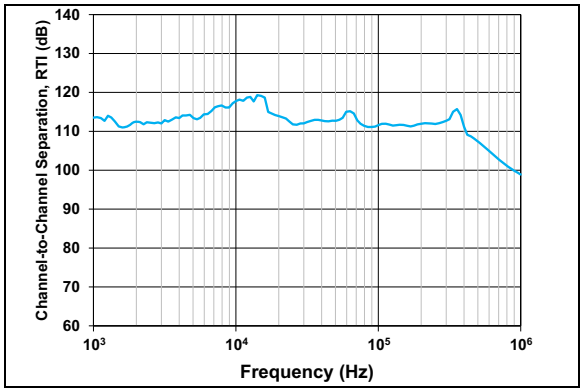


FIGURE 2-27: *Channel-to-Channel Separation vs. Frequency.*

2.4 Input Noise and Distortion

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

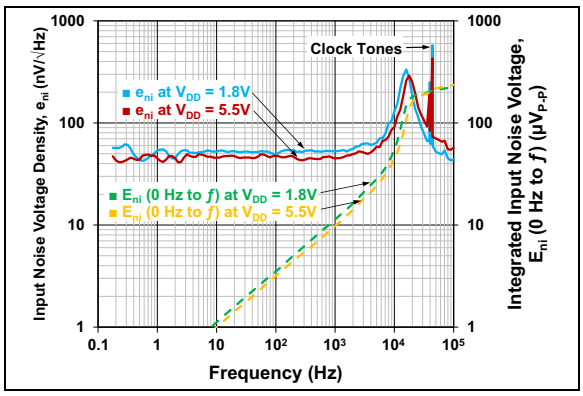


FIGURE 2-28: *Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.*

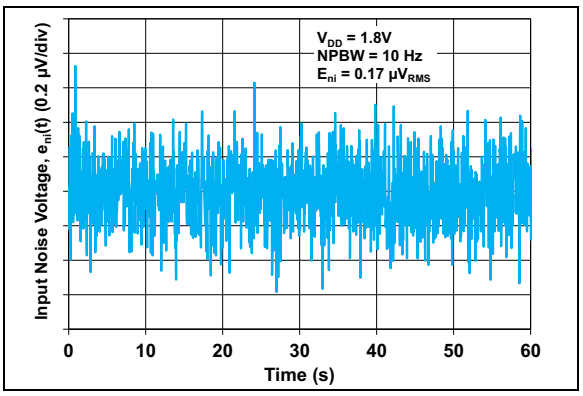


FIGURE 2-31: *Input Noise vs. Time, 10 Hz Filter and V_{DD} = 1.8V.*

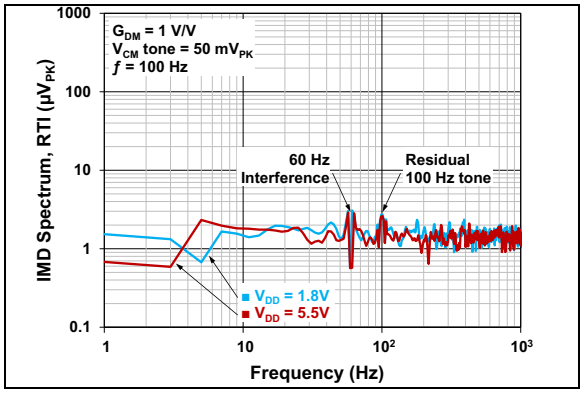


FIGURE 2-29: *Inter-Modulation Distortion vs. Frequency, V_{CM} Disturbance (see Figure 1-6).*

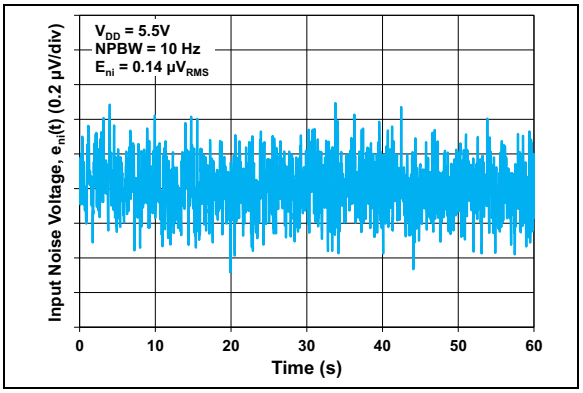


FIGURE 2-32: *Input Noise vs. Time, 10 Hz Filter and V_{DD} = 5.5V.*

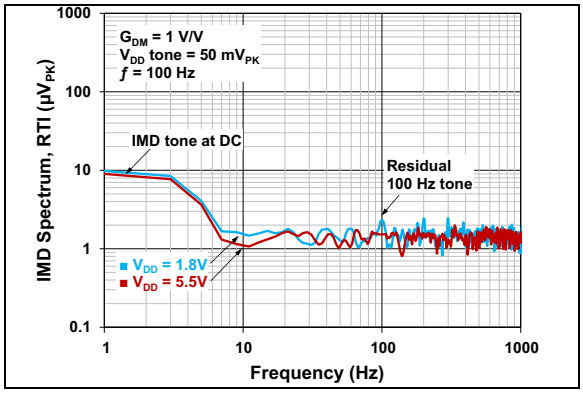


FIGURE 2-30: *Inter-Modulation Distortion vs. Frequency, V_{DD} Disturbance (see Figure 1-6).*

2.5 Time Response

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

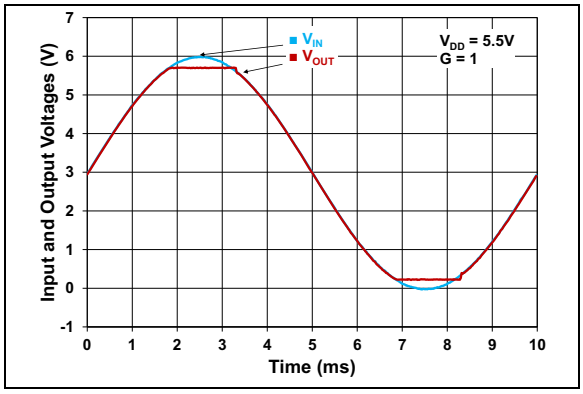


FIGURE 2-33: *MIC333/2333 Shows No Input Phase Reversal with Overdrive.*

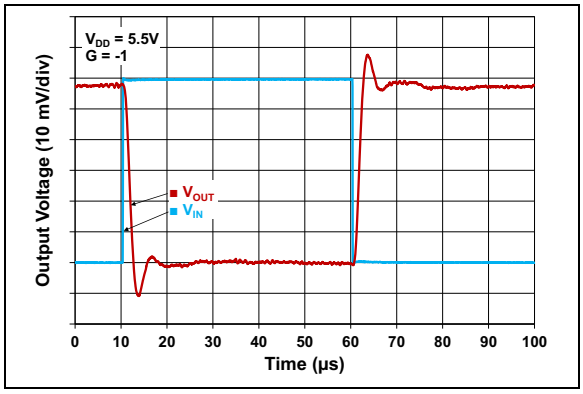


FIGURE 2-36: *Inverting Small Signal Step Response.*

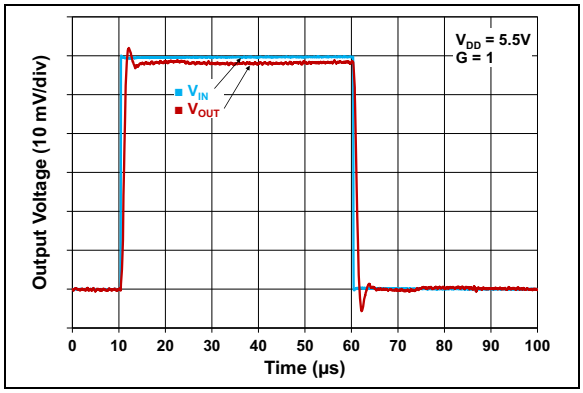


FIGURE 2-34: *Noninverting Small Signal Step Response.*

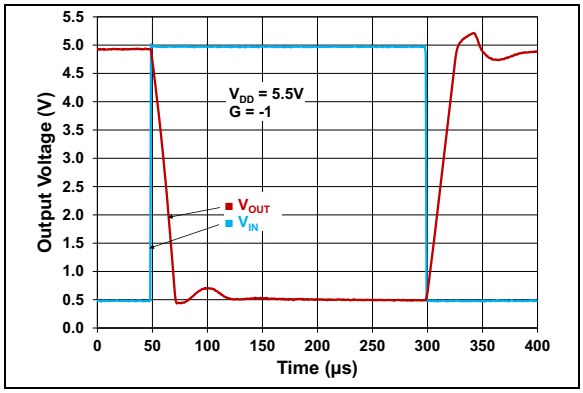


FIGURE 2-37: *Inverting Large Signal Step Response.*

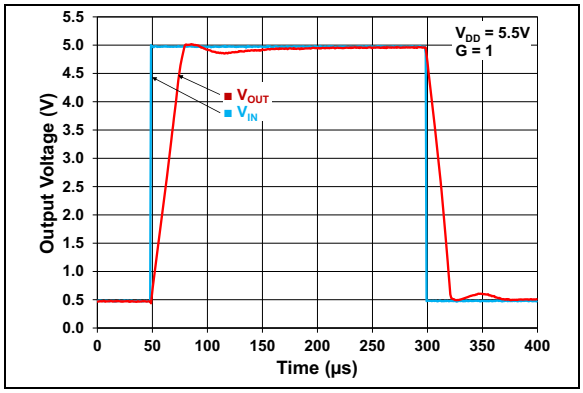


FIGURE 2-35: *Noninverting Large Signal Step Response.*

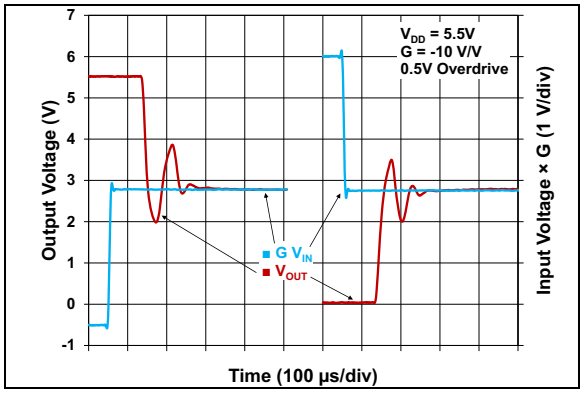


FIGURE 2-38: *Output Overdrive Recovery vs. Time, G = -10 V/V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 20 pF.

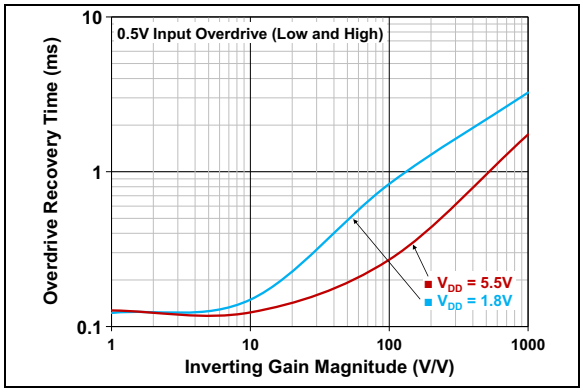


FIGURE 2-39: *Output Overdrive Recovery Time vs. Inverting Gain.*

3.0 PIN DESCRIPTION

The pins of MIC333/2333 are described in Table 3-1.

TABLE 3-1: MIC333 PIN DESCRIPTIONS

MIC333		MIC2333	Symbol	Description
SOT-23	SC70	MSOP		
1	4	1	V_{OUT}/V_{OUTA}	Output of Operational Amplifier A
2	2	4	V_{SS}	Negative Power Supply
3	1	3	$V_{IN}+/V_{INA}+$	Noninverting Input of Operational Amplifier A
4	3	2	$V_{IN}-/V_{INA}-$	Inverting Input of Operational Amplifier A
5	5	8	V_{DD}	Positive Power Supply
—	—	5	$V_{INB}+$	Noninverting Input of Operational Amplifier B
—	—	6	$V_{INB}-$	Inverting Input of Operational Amplifier B
—	—	7	V_{OUTB}	Output of Operational Amplifier B

3.1 Analog Outputs (V_{OUT}, V_{OUTA}, V_{OUTB})

These pins are low impedance voltage sources.

3.2 Analog Inputs ($V_{IN}+$, $V_{IN}-$, $V_{INA}+$, $V_{INA}-$, $V_{INB}+$, $V_{INB}-$)

These inverting and noninverting pins are high impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{DD}, V_{SS})

The positive power supply (V_{DD}) is between +1.8V to +5.5V higher than the negative power supply (V_{SS}). For normal operations, all other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} connects to GND and V_{DD} connects to the power supply.

Note: V_{DD} requires bypass capacitors.

4.0 APPLICATIONS

Manufactured using an advanced CMOS process, the MIC333/2333 family of zero-drift operational amplifiers is designed for precision applications that require small packages and low power. Their low supply voltage and low quiescent current make these devices ideal for battery-powered applications.

4.1 Overview of Zero-Drift Operation

Figure 4-1 shows a simplified functional diagram of MIC333/2333. The architecture shown in this diagram reduces slow voltage errors, resulting in much better V_{OS}, TC_1, TC_2, CMRR, PSRR, A_{OL} and $1/f$ noise.

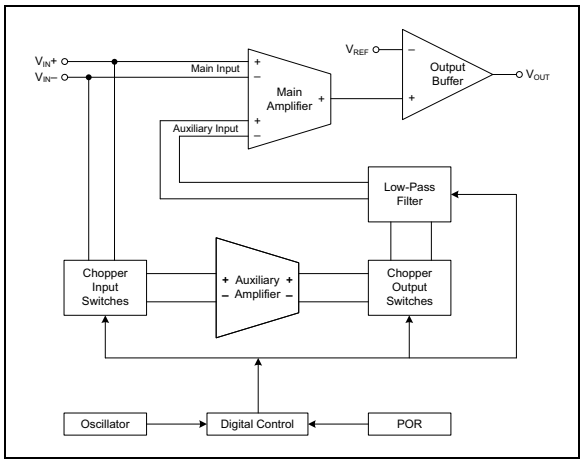


FIGURE 4-1: *Simplified Zero-Drift Operational Amplifier Functional Diagram.*

4.1.1 BUILDING BLOCKS

The Main Amplifier is designed for high bandwidth and gain. Its main input is for high frequency signals, while the auxiliary input is for low frequency signals. Both sets of inputs are combined internally.

The Auxiliary Amplifier together with the Chopper Switches provide high gain to low frequency signals. DC errors and low frequency noise are modulated to higher frequencies and filtered out. The low frequency signal is then modulated back to its frequency band. High frequency white noise is also modulated to low frequency, providing better performance than auto-zeroed parts. The Low-Pass Filter reduces Chopping Clock harmonics.

The Output Buffer drives external loads at V_{OUT} (V_{REF} is an internal reference voltage).

The Oscillator runs at 200 kHz and is halved, producing a Chopping Clock rate of 100 kHz and low level output clock tones at 50 kHz (Figure 2-28).

The internal POR component starts MIC333/2333 in a well-known state that protects the device against power supply brown-outs. The Digital Control component manages switching and POR events.

4.1.2 INTER-MODULATION DISTORTION

When an AC signal is present, MIC333/2333 shows low level inter-modulation distortion (IMD) products. For more details, see Figure 2-29 and Figure 2-30.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the nonlinear response of the zero-drift circuitry to produce IMD tones at sum and difference frequencies. Each harmonic of the square wave clock has a set of IMD tones centered on it.

4.2 Other Functional Blocks

4.2.1 RAIL-TO-RAIL INPUTS

The input stages of MIC333/2333 use two CMOS differential pairs connected in parallel. A pair operates at low common mode input voltage (V_{CM} close to V_{IN}+ and V_{IN}- in normal operation), while the other at high V_{CM}. At +25°C, the input operates with V_{CM} between V_{SS} – 0.15V and V_{DD} + 0.2V (Figure 2-16). The input offset voltage, V_{OS}, is measured at V_{CM} = V_{SS} – 0.15V and V_{CM} = V_{DD} + 0.2V to ensure proper operation.

The transition between the input stages occurs when $V_{CM} \approx V_{DD} - 0.9V$ (Figure 2-10 and Figure 2-11).

4.2.1.1 Phase Reversal

Input devices do not exhibit phase reversal when voltages on the input pins exceed supply voltages. Figure 2-33 shows an input voltage exceeding both supplies with no phase reversal.

4.2.1.2 Input Voltage Limits

To prevent damage and/or improper operation of MIC333/2333, the circuit must limit voltages at the input pins (**Section 1.1, "Absolute Maximum Ratings(†)"**).

Note: This requirement is independent of the current limits detailed in **Section 4.2.1.3, "Input Current Limits"**.

Electrostatic discharge (ESD) protection on the inputs can be implemented as shown in Figure 4-2. This structure protects the input transistors against most, but not all overvoltage conditions and minimizes the input bias current, I_B.

The input ESD diodes clamp the operational amplifier inputs when the pins drop more than one diode below V_{SS}. The input ESD diodes also clamp any voltages that exceed V_{DD}. Their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond V_{DD}) events. Very fast ESD events (that do not exceed the ESD specifications) are limited to prevent damage.

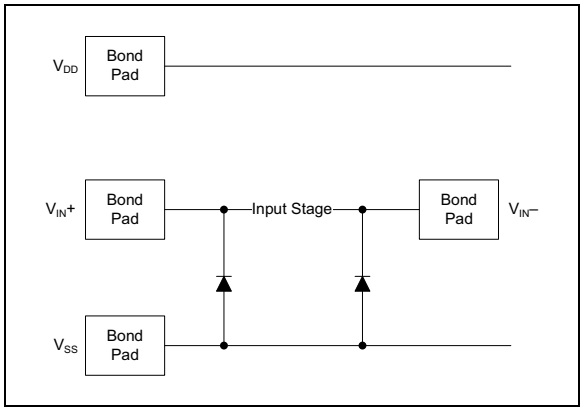


FIGURE 4-2: *Simplified Analog Input ESD Structures.*

Some applications require excessive voltages not reach the inputs of the operational amplifier. Figure 4-3 shows one approach to protect these inputs. D_1 and D_2 can be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode connected field-effect transistors (FETs) for low leakage.

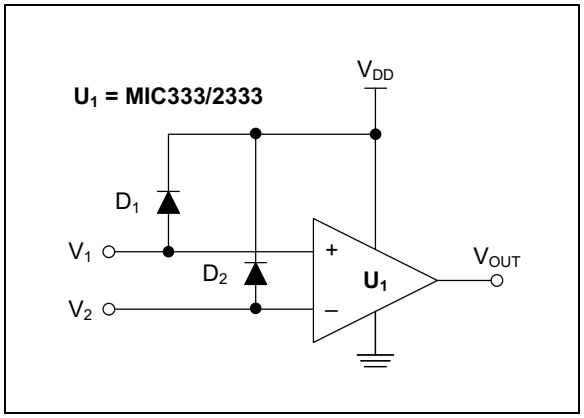


FIGURE 4-3: *Protecting the Analog Inputs Against High Voltages.*

4.2.1.3 Input Current Limits

To prevent damage and/or improper operation of MIC333/2333, the circuit must limit currents at the input pins (**Section 1.1, "Absolute Maximum Ratings(†)"**).

Note: This requirement is independent of the voltage limits detailed in **Section 4.2.1.2, "Input Voltage Limits"**.

Figure 4-4 shows one approach to protect the inputs of the operational amplifier. Resistors R_1 and R_2 limit the possible current in or out of the input pins (and into diodes D_1 and D_2). The diode currents dump into V_{DD}.

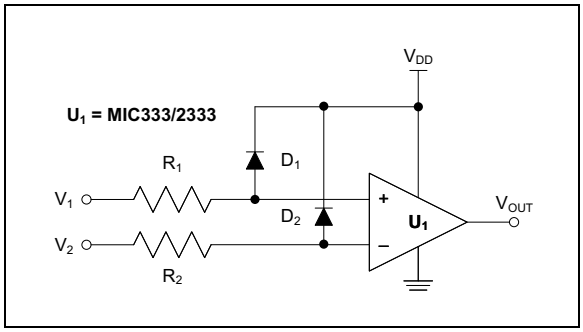


FIGURE 4-4: *Protecting the Analog Inputs Against High Currents.*

Should this be "Equation 4-1:"?

EQUATION 4-1:

$$min(R_1,R_2) > \frac{V_{SS} - min(V_1,V_2)}{2mA}$$

$$min(R_1,R_2) > \frac{max(V_1,V_2) - V_{DD}}{2mA}$$

Instead of connecting between resistors R_1 and R_2 and the operational amplifier inputs as shown in Figure 4-4, diodes D_1 and D_2 can connect between V_1 and R_1 and between V_2 and R_2, respectively. In such configurations, limit the currents through diodes D_1 and D_2 using other mechanisms. Resistors R_1 and R_2 serve as in-rush current limiters: DC current into the operational amplifier inputs (V_{IN}+ and V_{IN}-) is very small.

Note: A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}). See Figure 2-15.

4.2.2 RAIL-TO-RAIL OUTPUT

When R_L = 10 kΩ connects to $V_{DD}/2$ and V_{DD} = 5.5V, the output voltage of MIC333/2333 is V_{DD} – 20 mV at minimum and V_{SS} + 20 mV at maximum. For more details, see Figure 2-17 and Figure 2-18.

Note: MIC333/2333 is designed to drive light loads. Use a second operational amplifier to buffer its output from heavy loads.

4.3 Application Tips

4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1, "DC Electrical Specifications" shows the temperature coefficients (TC_1 and TC_2) of the input offset voltage, V_{OS}. Use Equation 4-2 to determine V_{OS} at any temperature, when in the specified range.

EQUATION 4-2:

$$V_{OS}(T_A) = V_{OS} + TC_1 \times \Delta T + TC_2 \times \Delta T^2$$

Where:

V_{OS} = Input Offset Voltage (µV)
T_A = Ambient Temperature (°C)
TC_1 = Linear Temperature Coefficient (µV/°C)
TC_2 = Quadratic Temperature Coefficient (nV/°C^2)
ΔT = T_A -25°C (°C)

4.3.2 DC GAIN PLOTS

Figure 2-4 through Figure 2-6 are histograms of the reciprocals of the Power Supply Rejection (PSRR), Common-Mode Rejection (CMRR) and DC Open-Loop Gain (A_{OL}), presented in units of µV/V. These figures show the changes in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}) that result when a change input offset voltage occurs.

In Figure 2-6, the $1/A_{OL}$ histogram is centered around 0 µV/V since the input noise of the operational amplifier dominates the measurements. The negative values shown represent noise and tester limitations and *not* unstable behavior. Production tests verify the stability of every MIC333 and MIC2333 operational amplifier.

4.3.3 OFFSET AT POWER-UP

When MIC333/2333 powers up, V_{OS} starts at its uncorrected value (usually between -5 mV and +5 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time required to reach a valid output is delayed by an output overdrive recovery time (t_{ODR}), in addition to the startup time (t_{STR}).

To avoid this extra start-up time, reduce the DC gain or connect a capacitor across the feedback resistor, R_F.

4.3.4 V_{CM} TRANSITION

V_{CM} transition is not an issue present in most designs using MIC333/2333. For the best distortion and gain linearity, avoid this transition region by shifting V_{CM} with higher noninverting and difference gains or by using inverting gains.

4.3.5 INPUT BIAS CURRENTS

Input bias currents have two significant sources: switching glitches that dominate below +105°C and input ESD diode leakage currents that dominate above +105°C. See Figure 2-14.

Input bias currents at the noninverting input (I_{BP} at V_{IN}+) and the inverting input (I_{BM} at V_{IN}-) are positive when they flow into the inputs. Figure 2-12 and Figure 2-13 show how I_{BP} and I_{BM} vary with V_{CM} and T_A.

The traditional representation of input bias currents is calculated using Equation 4-3.

EQUATION 4-3:

$$I_B = \frac{I_{BP} + I_{BM}}{2} \qquad I_{OS} = I_{BP} - I_{BM}$$

Where:

I_B = Input Bias Current (pA)
I_{BP} = Noninverting Input Bias Current (pA)
I_{BM} = Inverting Input Bias Current (pA)
I_{OS} = Input Offset Current (pA)

Table 1-1, "DC Electrical Specifications" specifies I_B and I_{OS}. Figure 2-14 shows how I_B and I_{OS} vary with V_{CM} and T_A. I_{OS} remains constant at low temperatures, because switching glitches dominate under +105°C.

Use Equation 4-4 to convert I_B and I_{OS} back to I_{BP} and I_{BM}.

EQUATION 4-4:

$$I_{BP} = I_B + \frac{I_{OS}}{2} \qquad I_{BM} = I_B - \frac{I_{OS}}{2}$$

Where:

I_{BP} = Noninverting Input Bias Current (pA)
I_B = Input Bias Current (pA)
I_{OS} = Input Offset Current (pA)
I_{BM} = Inverting Input Bias Current (pA)

4.3.6 EQUIVALENT INPUT RESISTANCES

In Figure 4-5, the noninverting operational amplifier input connects to resistor R_N, while the inverting input connects to resistor $R_F||R_G$. For both connections, the resistances are from the input pins, through resistors to the voltage sources.

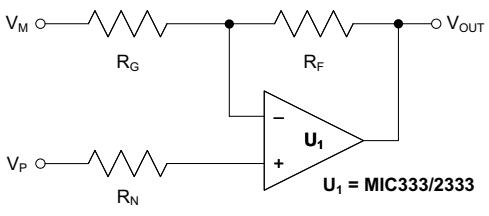


FIGURE 4-5: *Input Resistances.*

To determine the DC voltage error (V_{ERR}) measured at V_{OUT}, use Equation 4-5.

EQUATION 4-5:

$$V_{ERR} = I_{BM} \times R_F - I_{BP} \times R_N\left(1 + \frac{R_F}{R_G}\right)$$

$$= I_{BM} \times R_F\left(1 - \frac{R_N}{R_F \parallel R_G}\right) - I_{OS} \times R_F\left(1 + \frac{R_N}{R_F \parallel R_G}\right)$$

Where:

V_{ERR} = DC Voltage Error (mV)
I_{BM} = Inverting Input Bias Current (pA)
R_F = Feedback Resistance (Ω)
I_{BP} = Noninverting Input Bias Current (pA)
R_N = Noise Resistance (Ω)
R_G = Gain Resistance (Ω)
I_{OS} = Input Offset Current (pA)

To minimize V_{ERR} at all temperatures, the resistances connected to the operational amplifier inputs must be small. To minimize V_{ERR} at high temperatures, these resistances must also be equal, besides being small.

For high frequencies (f > 1 MHz), ensure the inputs are connected to resistances between 10Ω and 1 kΩ. This minimizes the impact of very fast switching glitches on overall performance.

4.3.7 CAPACITIVE LOADS

Driving large capacitive loads can cause stability issues for operational amplifiers. This produces gain peaking in the frequency response and overshoot and ringing in the step response.

Due to their unique topology, MIC333/2333 operational amplifiers have a different output impedance compared to similar devices. When driving a capacitive load with these operational amplifiers, R_{ISO} (as shown in Figure 4-6) improves the stability of the feedback loop by making the output load more resistive at higher frequencies.

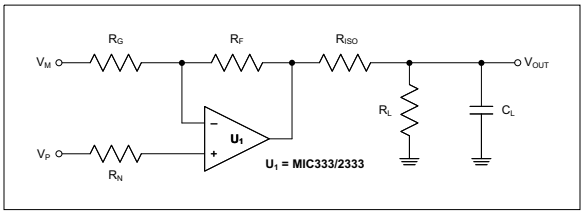


FIGURE 4-6: *R_{ISO} – Output Resistor, Stabilizes Capacitive Loads.*

The noise gain (G_N) of the circuit is usually set by R_F and R_G (see Figure 4-6):

- For noninverting gains, G_N = Signal Gain.
- For inverting gains, G_N = 1 + |Signal Gain|. For example, -1 V/V results in G_N = +2 V/V.

Figure 4-7 shows the recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the load capacitance normalized by $\sqrt{G_N}$ ($C_L/\sqrt{G_N}$) and the y-axis is the recommended R_{ISO}.

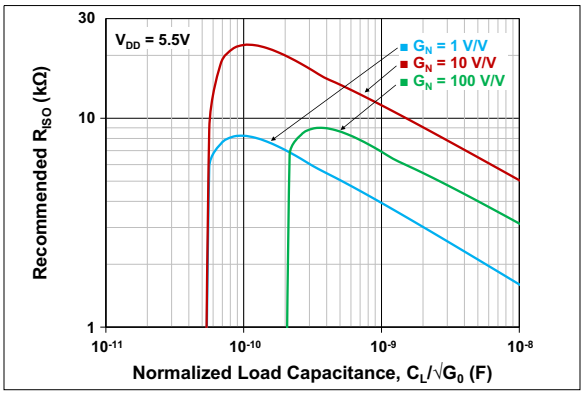


FIGURE 4-7: *Recommended R_{ISO} Values for Capacitive Loads.*

For best performance, maintain $R_L||(R_F + R_G) >> R_{ISO}$, but not too large. For guidance, see **Section 4.3.8, "Gain Peaking"**.

After selecting an appropriate R_{ISO} value for the circuit, verify the resulting frequency response peaking and step response overshoot using simulations and bench measurements. Adjust the value of R_{ISO} until the response is reasonable.

4.3.8 GAIN PEAKING

Figure 4-8 shows an operational amplifier circuit where V_P and V_M can be dynamic inputs or DC voltages. This circuit depicts noninverting, inverting and difference amplifiers. Capacitors C_N and C_G are the total capacitance at the input pins and include the common mode input capacitance (C_{CM}) of the operational amplifier, parasitic board capacitance and any parallel capacitor. Capacitor C_{FP} represents the parasitic capacitance coupling the output and noninverting input pins.

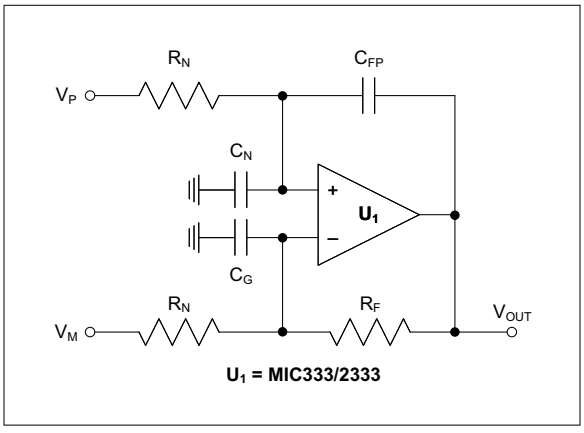


FIGURE 4-8: *Operational Amplifier with Parasitic Capacitance.*

Capacitor C_G acts in parallel with resistor R_G (except at a gain of +1 V/V). This can cause an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. To minimize this effect either:

- Reduce C_G,
- Reduce $R_F||R_G$ or
- Place a capacitor C_F in parallel with R_F, ensuring that $1 + C_G/C_F = 1 + R_F/R_G$.

Capacitor C_N and resistor R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at $1/(2\pi \cdot R_N \cdot C_N)$. At high gains, R_N must be small to prevent positive feedback and oscillations. Larger C_N values also help.

4.3.9 NOISE AND UNDESIRED SIGNALS

Reduce undesired noise and signals using:

- Low bandwidth signal filters:
  - For random analog noise and interference
- Good printed circuit board (PCB) layout techniques:
  - For crosstalk
  - For low interactions with fast switching edges
- Good power supply design:
  - For isolation from other devices
  - For supply line interference

To significantly improve the noise peak and clock tones shown in Figure 2-28, use a two pole low-pass filter with a bandwidth under 5 kHz (see Figure 4-12 for an example circuit).

The input noise current density (i_{ni} in Table 1-2, "AC Electrical Specifications") is negligible for applications using MIC333/2333 devices to amplify small signals. Any input resistance big enough to make i_{ni} noticeable also causes very large input offset shifts due to input currents.

4.3.10 SUPPLY BYPASSING AND FILTERING

For good high frequency performance, MIC333/2333 has a local bypass capacitor (0.01 µF to 0.1 µF) within 2 mm of the power supply pin (V_{DD} for single supply). The device also requires a bulk capacitor (≥ 1 µF) within 20 mm to provide large, slow currents. Usually, this bulk capacitor is not shared with other devices.

In some cases, high frequency power supply noise (for example, switched mode power supplies) may cause undue IMD, with a DC offset shift. Filter this noise. Adding a resistor or a ferrite chip in the supply line before the bypass capacitors can help.

4.3.11 PCB DESIGN FOR PRECISION

To achieve the specified DC precision, multiple physical errors must be minimized. The PCB, the wiring and the thermal environment strongly impact final performance.

4.3.11.1 PCB Layout

Whenever two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (Seebeck or thermojunction effect). While this effect is used to measure the temperature in thermocouples, it causes errors in high DC precision designs. The following are examples of thermojunctions:

- Components (resistors, operational amplifier etc.) soldered to a copper pad
- Wires connected to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermojunctions have temperature-to-voltage conversion coefficients of 1 to 100 µV/°C.

Mechanical connections of any two metal objects add contact potential errors to a design.

Note: For in-depth information on PCB layout techniques that minimize thermojunction effects, refer to the following Microchip Application Note: AN1258, *"Operational Amplifier Precision Design: PCB Layout Techniques"*. It also covers other effects, such as crosstalk, impedances, humidity and mechanical stresses.

4.3.11.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources can affect DC performance. Nonlinear distortion converts these signals to multiple tones, including a DC shift in voltage. When an ADC samples the signal, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding
- Use a ground plane (or a star ground where necessary)
- Place the input signal source near the device under test (DUT)
- Use good PCB layout techniques
- Use a separate power supply filter

4.3.11.3 Miscellaneous Effects

To minimize bias current related offsets, resistances connected to the input pins must be as small and as near to equal as possible.

Trace capacitances connected to the input pins must be small and equal. This helps minimize offset voltages induced by switching glitches.

Bending a coaxial cable with a radius that is too small causes a small voltage drop to appear on the center conductor (triboelectric effect). Ensure the bending radius is large enough to maintain full contact between the conductors and the insulation.

Mechanical stresses can make some capacitor types (such as certain ceramics) output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

4.4 Typical Applications

4.4.1 WHEATSTONE BRIDGE

Many sensors like strain gauges, pressure sensors and thermal sensors like resistance temperature detectors (RTDs) are configured as Wheatstone bridges. The signal is differential and small, while the common mode errors can be large. Designs with high differential gain are desirable.

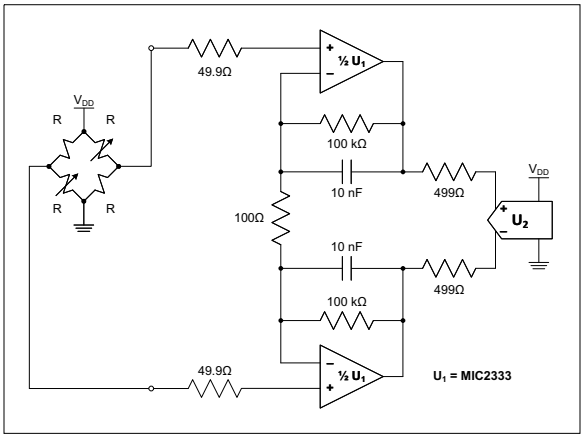


FIGURE 4-9: *Wheatstone Bridge Circuit.*

Figure 4-9 shows the dual MIC2333 configured as a differential input and differential output operational amplifier. Its high input impedances minimize loading errors at the bridge and produce a differential gain of +2001 V/V, which is appropriate for small differential signals. The capacitors set a 16 kHz low-pass pole for the signal.

Note: Since the amplifier has a 0 dB CMRR, use an ADC with differential input (U_2) to provide good overall CMRR. Ensure to drive both the bridge and the ADC using the same clean voltage (V_{DD}).

4.4.2 NONINVERTING AMPLIFIER

Figure 4-10 shows MIC333 (U_2) correcting the input offset voltage of an noninverting amplifier (U_1, R_1, R_2 and R_3).

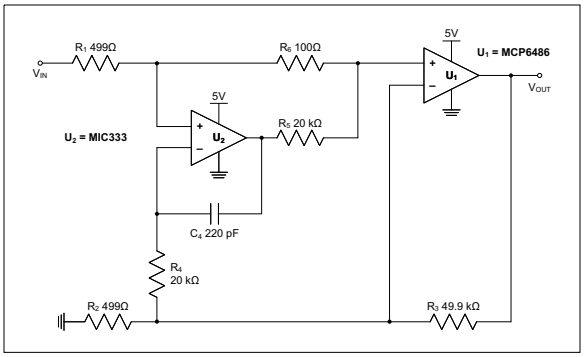


FIGURE 4-10: *Noninverting Amplifier Offset Correction.*

U_2, R_4 and C_4 integrate the offset error encountered at the input of U_1. This integration process must be slow enough to stabilize for the noise gain set by resistors R_2 and R_3 (see **Section 4.3.7, "Capacitive Loads"**).

Resistors R_5 and R_6 attenuate the integrator's output. These resistances slow the integration process, limit the correction at U_1 and reduce the high frequency errors from U_2 (including noise). The correction loop forces the inverting input of U_1 closer to V_{IN}.

U_1, R_2 and R_3 provide a noninverting signal gain of +101 V/V and a bandwidth of 90 kHz. The correction voltage at the noninverting input of U_1 is ±12 mV and prevents overdriving U_1. This attenuation also slows the offset correction loop by a factor of 201.

The integrator reaches a gain of +1 V/V at 36 kHz. This results in the offset correction loop to reach a gain of +1 V/V at 180 Hz and U_2 dominating U_1's input errors below 180 Hz.

4.4.3 INVERTING AMPLIFIER OFFSET CORRECTION

Figure 4-11 shows MIC333 (U_2) correcting the input offset voltage of an inverting amplifier (U_1, R_1 and R_3).

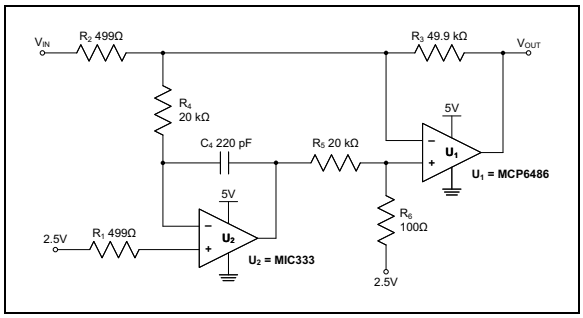


FIGURE 4-11: *Inverting Amplifier Offset Correction.*

The operation of the inverting amplifier offset correction circuit is similar to the operation of the circuit in Figure 4-10. The main difference is that the mid-supply reference voltage (+2.5V) drives the noninverting input of U_2 and resistor R_6 (part of the attenuator). Therefore, the correction loop forces the inverting input of U_1 closer to 2.5V, instead of closer to V_{IN}.

4.4.4 PREAMPLIFIER

Figure 4-12 shows MIC333 operating as a preamplifier. The gain is +500 V/V and the dominant low-pass poles are at 320 Hz and 1.6 kHz. There poles greatly reduce the output noise (Figure 2-28) and undesired signals.

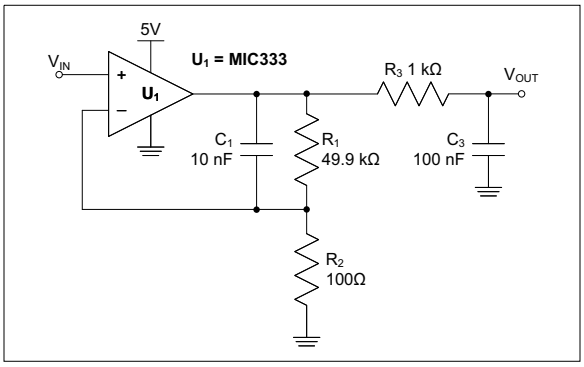


FIGURE 4-12: *Preamplifier.*

U_1, C_1, R_1 and R_2 set an operational amplifier gain of zero at 160 kHz (and a pole near 300 kHz), where the signal gain approaches +1 V/V. This pole is significantly smaller than U1's gain bandwidth product (GBWP) of 300 kHz, resulting in a very stable operational amplifier.

4.4.5 LOW-SIDE CURRENT MONITOR

Figure 4-13 shows a low-side current monitor with a gain of +100 V/V and a low-pass filter pole at 0.8 kHz. Z_L is the load and R_{SH} is the shunt resistor.

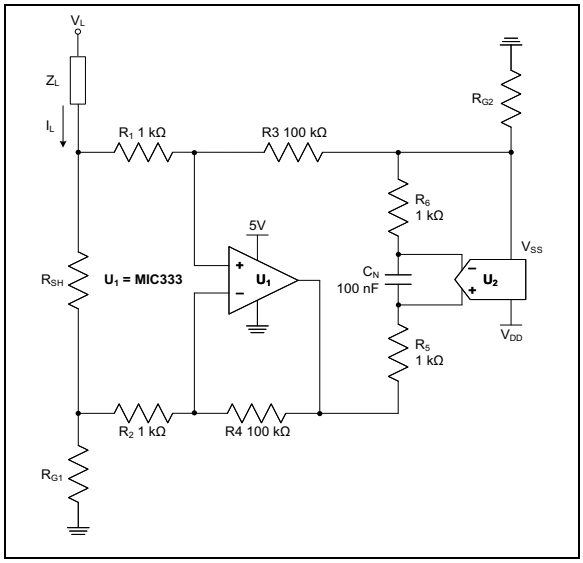


FIGURE 4-13: *Low-Side Current Monitor.*

R_{G1} and R_{G2} are parasitic ground resistances that produce different reference voltages at R_{SH} and at the inverting input of U_2 when currents flow through these components. R_{G1} must be placed near Z_L, R_{SH} and the inputs of U_1. R_{G2} must be placed near the reference voltage point for both R_3 and the inverting input of U_2.

To minimize crosstalk caused by R_{G1} and R_{G2}, keep traces short and wide, keep the path for I_L away from U_2 and use a solid ground plane in the PCB.

4.4.6 PRECISION NONINVERTING COMPARATOR

Figure 4-14 shows MIC333 used as an operational amplifier (U_1) to provide a very low DC offset and high difference gain, increasing the overall device precision. U_2 behaves as the comparator.

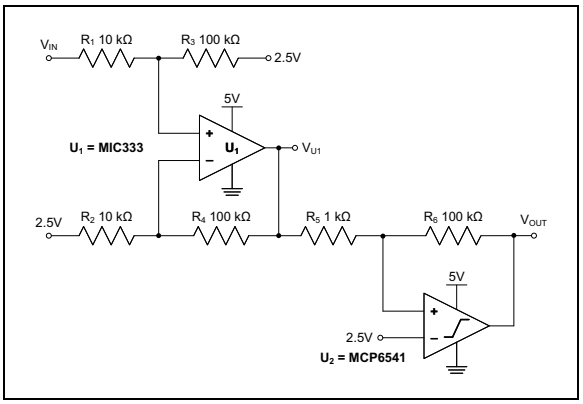


FIGURE 4-14: *Precision Noninverting Comparator.*

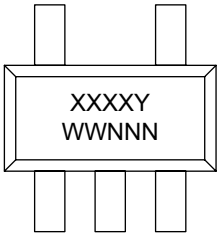
U_1 has a difference gain of +10 V/V, from V_{IN} – 2.5V to V_{U1} – 2.5V. Resistors R_5 and R_6 increase hysteresis at V_{U1} by 5 mV to ~8 mV. The total hysteresis referred back to V_{IN} is ~0.8 mV.

Because the internal V_{OS} correction circuitry does not operate properly without an appropriate negative feedback loop, MIC333 cannot behave as a comparator by itself.

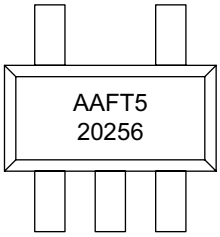
5.0 PACKAGE INFORMATION

5.1 Package Marking Information

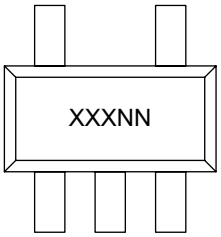
5-Lead SOT-23 (MIC333 only)



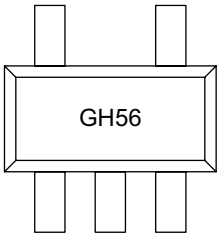
Example:



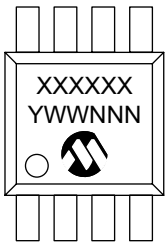
5-Lead SC70 (MIC333 only)



Example:



8-Lead MSOP (MIC2333 only)



Example:

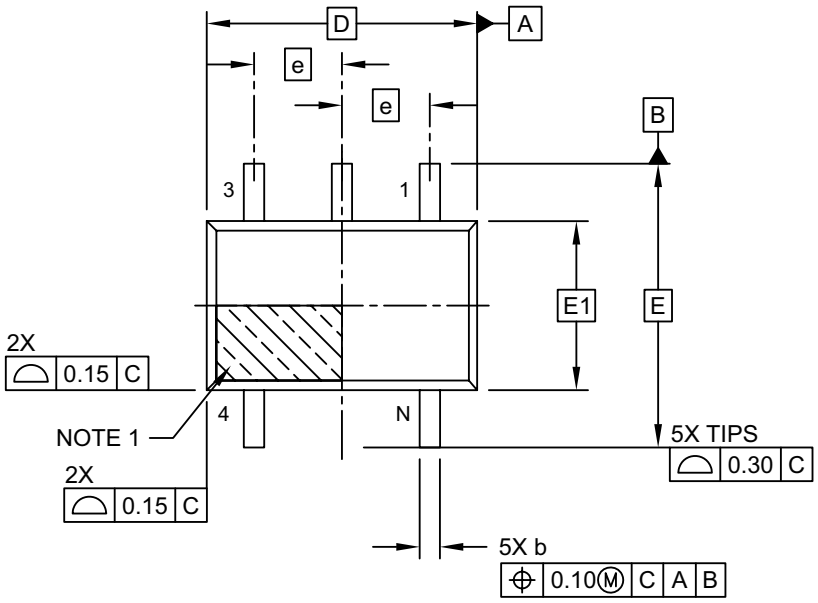
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

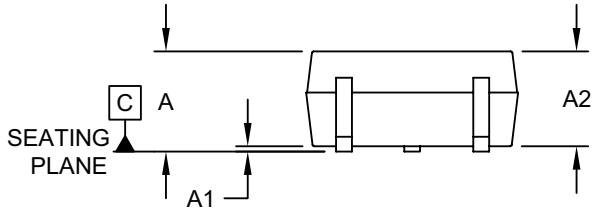
5.2 Package Drawings

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

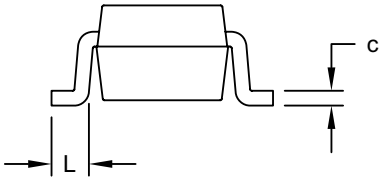
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

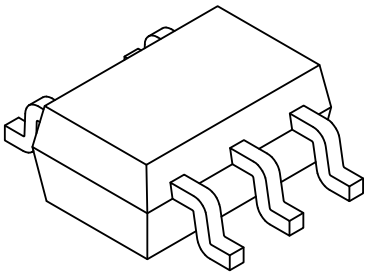


END VIEW

Microchip Technology Drawing C04-061-LTY Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

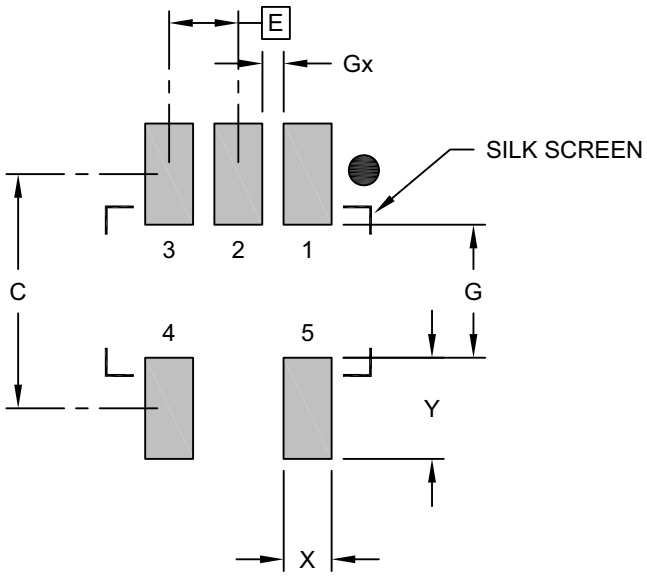
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LTY Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

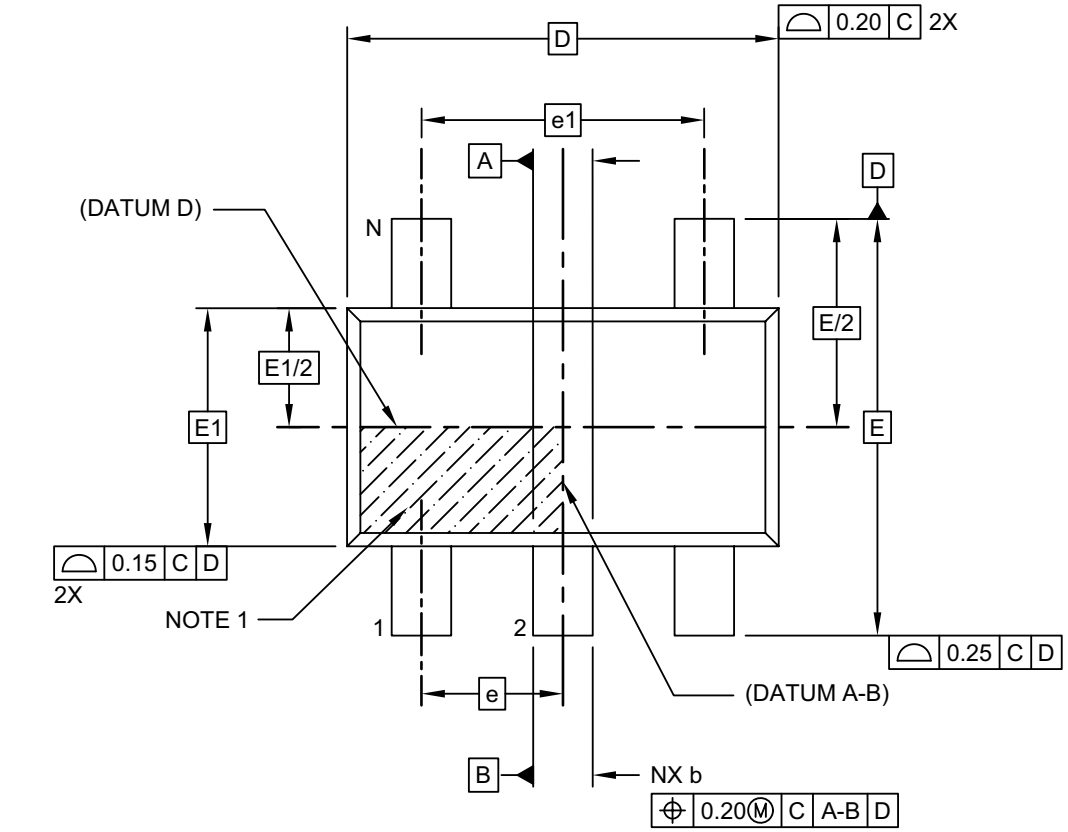
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

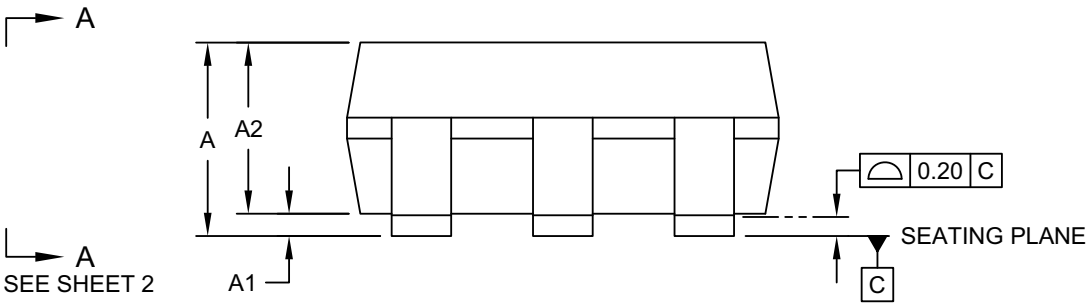
Microchip Technology Drawing No. C04-2061-LTY Rev E

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

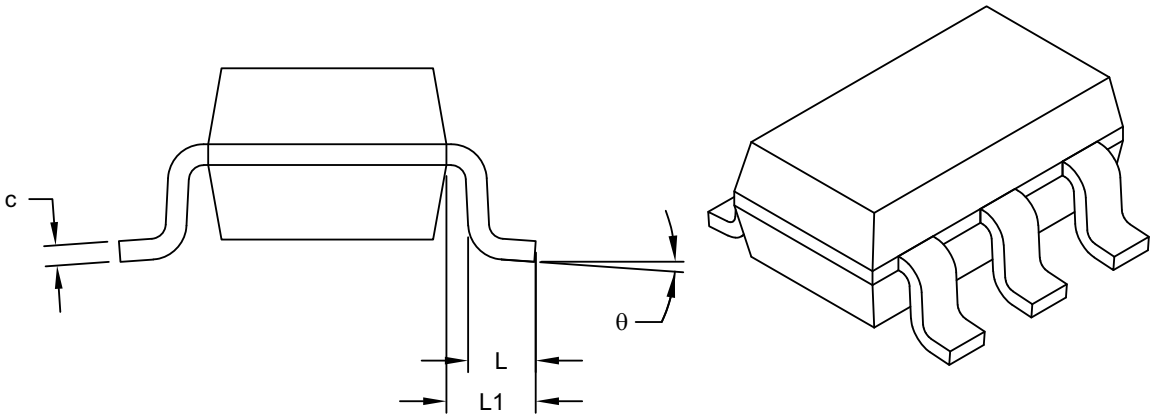


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

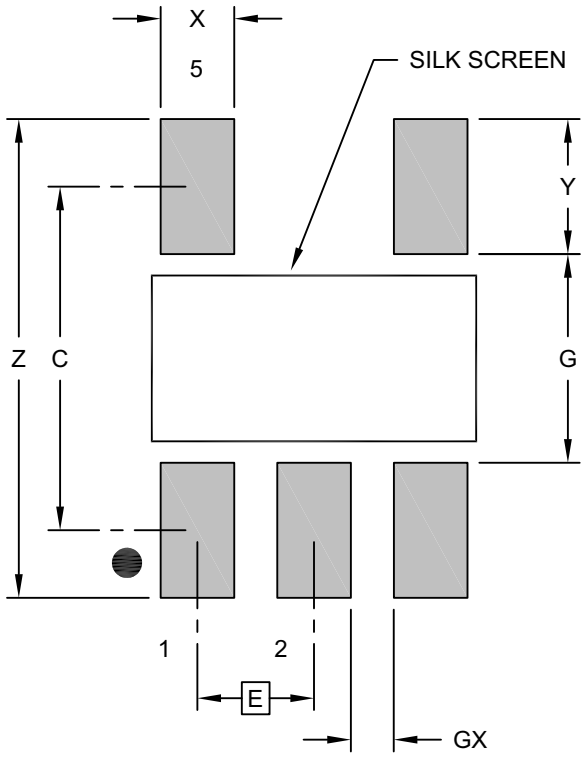
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

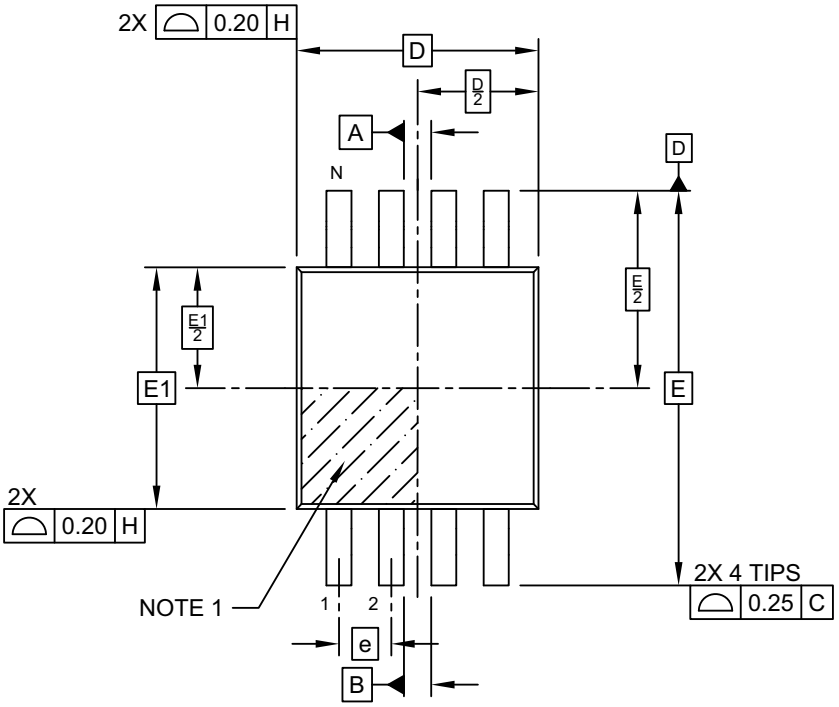
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

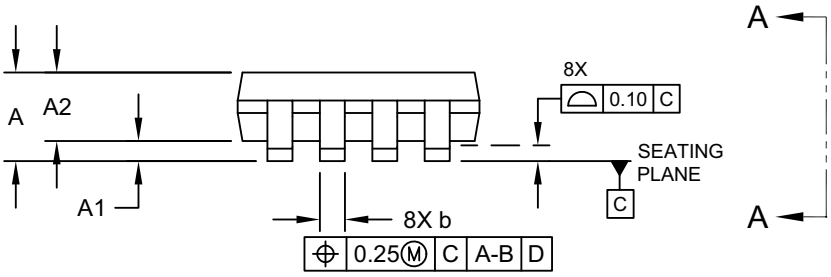
Microchip Technology Drawing No. C04-2091-OT Rev H

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

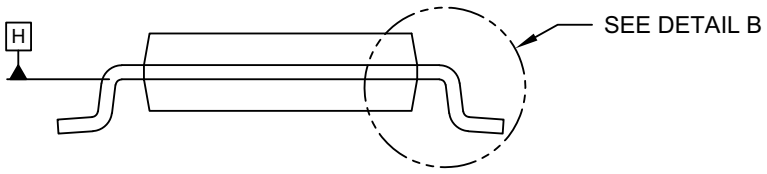
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

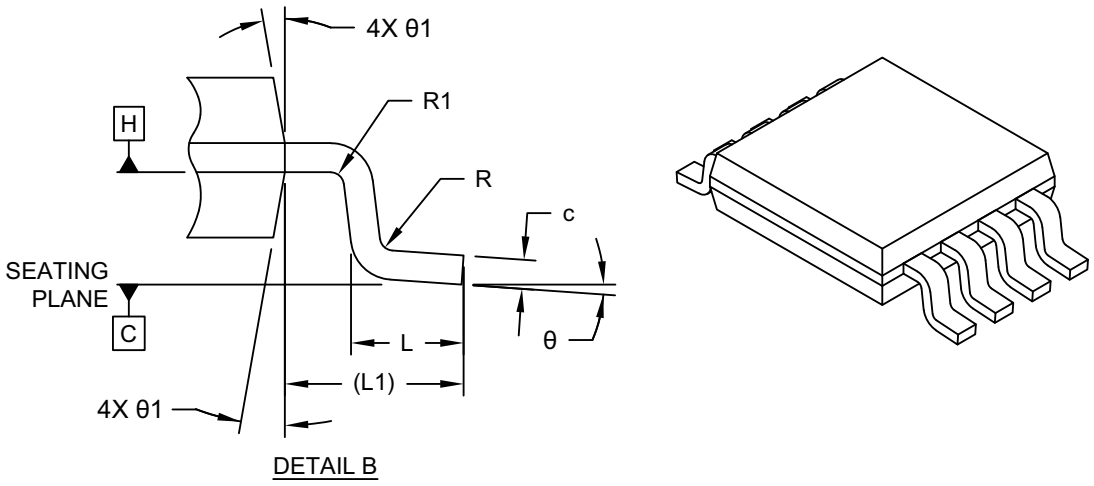


VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

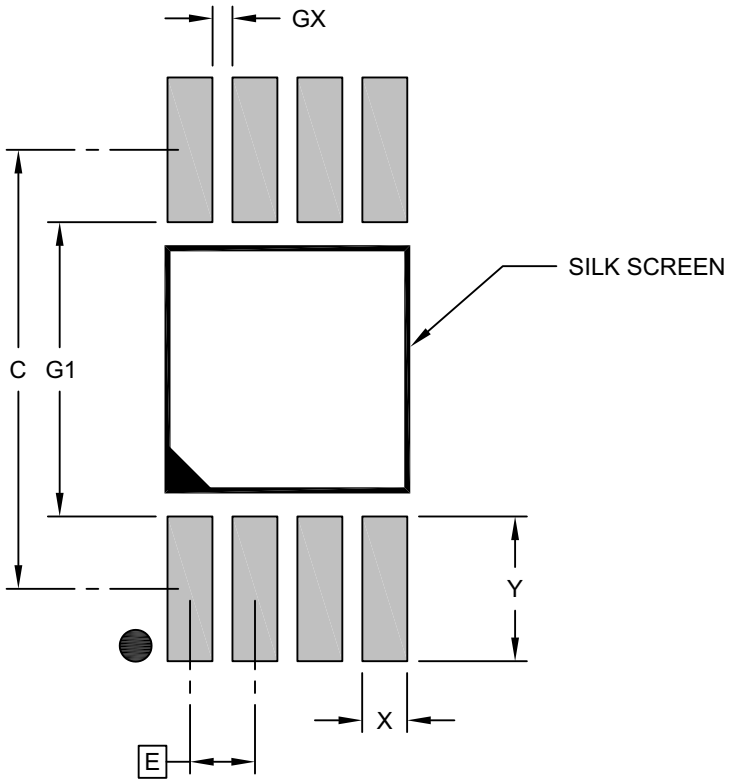
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

APPENDIX A: REVISION HISTORY

Revision A (June 2025)

- Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[(1)]	-X	/XX	[XXX]
Device	Tape and Reel	Temperature Range	Package	Class

Device:	MIC333	= Single Zero-Drift Operational Amplifier
	MIC2333	= Dual Zero-Drift Operational Amplifier
Tape and Reel Option:	T	= Tape and Reel[(1)]
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	LTY*	= 5-Lead Plastic Small Outline, SC70
	OT	= 5-Lead Plastic Small Outline, SOT-23
	MS	= 8-Lead Plastic Micro Small Outline, MSOP
	*Y	= Nickel-Palladium-Gold (NiPDAu) Manufacturing Designator (SC70 only)
Class:	Blank	= Non-automotive
	VAO	= Automotive

Examples:

a) MIC333T-E/LTY = Single Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 5-Lead SC70, NiPdAu Designator

b) MIC333T-E/OT = Single Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 5-Lead SOT-23

c) MIC2333T-E/MS = Dual Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 8-Lead MSOP

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	-X	/XX	[XXX]
Device	Tape and Reel	Temperature Range	Package	Class

Device:	MIC333	= Single Zero-Drift Operational Amplifier
	MIC2333	= Dual Zero-Drift Operational Amplifier
Tape and Reel Option:	T	= Tape and Reel[1]
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	LTY*	= 5-Lead Plastic Small Outline, SC70
	OT	= 5-Lead Plastic Small Outline, SOT-23
	MS	= 8-Lead Plastic Micro Small Outline, MSOP
	*Y	= Nickel-Palladium-Gold (NiPDAu) Manufacturing Designator (SC70 only)
Class:	Blank	= Non-automotive
	VAO	= Automotive

Examples:

a) MIC333T-E/LTYVAO = Single Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 5-Lead SC70, NiPdAu Designator, Automotive

b) MIC333T-E/OTVAO = Single Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

c) MIC2333T-E/MSVAO = Dual Zero-Drift Operational Amplifier, Tape and Reel, Extended Temperature, 8-Lead MSOP, Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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