QUALITY SEMICONDUCTOR, INC.

Programmable Skew PLL Clock Driver

TurboClock™

QS5991
QS5992
QS5993

FEATURES/BENEFITS

- 4 pairs of programmable skew outputs
- Low skew: 200ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization: Excellent for DSP applications
- Synchronous output enable
- Output frequency: 3.75MHz to 110MHz
- 2x, 4x, 1/2, and 1/4 outputs
- QS599X family provides following products:
  QS5991: 5V, with TTL outputs in PLCC
  QS5992: 5V, with CMOS outputs in PLCC
  QS5993: 5V, with TTL outputs in QSOP
- 3 skew grades:
  QS599X-2: t_{SKEW0}<250ps
  QS599X-5: t_{SKEW0}<500ps
  QS599X-7: t_{SKEW0}<750ps
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 46mA I_{OL} high drive outputs
- Low Jitter: < 200ps peak-to-peak
- Outputs drive 50Ω terminated lines
- Pin-compatible with Cypress CY7B991 and CY7B992
- Industrial temperature range
- Available in 32-pin PLCC and 28-pin QSOP

DESCRIPTION

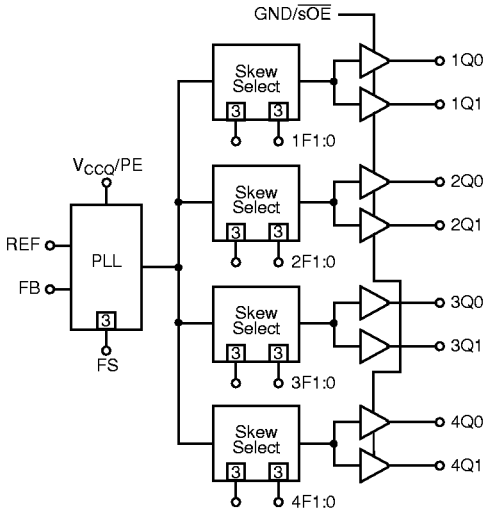
The QS599X family is a high fanout PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The QS5991 and QS5992 each have 8 programmable skew outputs in 4 banks of 2, while the QS5993 has 6 programmable skew outputs and 2 zero skew outputs. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

The QS599X family maintains Cypress CY7B99X compatibility while providing two additional features: Synchronous Output Enable (GND/$\overline{sOE}$), and Positive/Negative Edge Synchronization (V_{CCQ}/PE). When the GND/$\overline{sOE}$ pin is held low, all the outputs are synchronously enabled (CY7B99X compatibility). However, if GND/$\overline{sOE}$ is held high, all the outputs except 3Q0 and 3Q1 are synchronously disabled.

Furthermore, when the V_{CCQ}/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input (CY7B99X compatibility). When V_{CCQ}/PE is held low, all the outputs are synchronized with the negative edge of REF.

Figure 1. Logic Block Diagram

QS5991, QS5992



QS5993

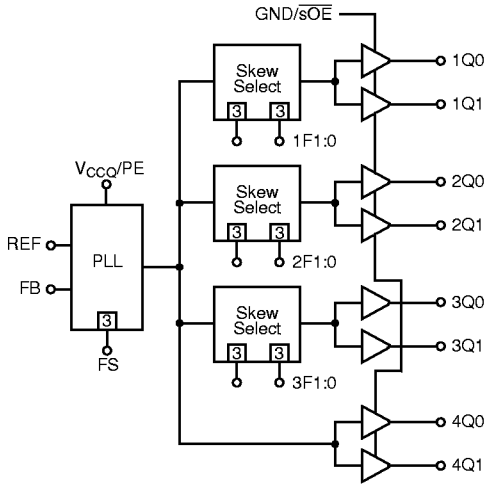
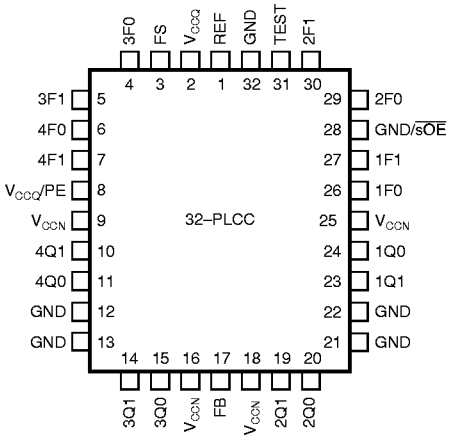


Figure 2. Pin Configuration (All Pins Top View)

QS5991, QS5992



QSOP, QS5993

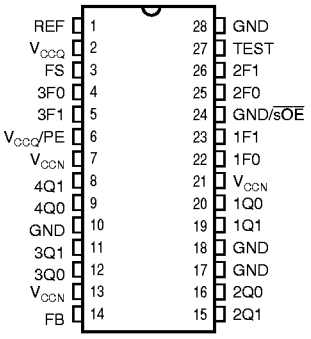


Table 1. Pin Definitions

Pin Name	Type	Definition
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST(1)	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew selections (see Table 3) remain in effect. Set LOW for normal operation.
GND/$\overline{sOE}$(1)	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 3Q0 and 3Q1) in a LOW state - 3Q0 or 3Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and GND/$\overline{sOE}$ is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0]=LL. Set GND/$\overline{sOE}$ LOW for normal operation.
V_{CCQ}/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
nF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. See Table 2.
nQ[1:0]	OUT	4 banks of 2 outputs, with programmable skew. On the QS5993, 4Q1:0 are fixed zero skew outputs.
V_{CCN}	PWR	Power supply for output buffers
V_{CCQ}	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

Note:
1. When TEST=MID and GND/$\overline{sOE}$=HIGH, PLL remains active with nF[1:0]=LL functioning as an output disable control for individual output banks. Skew selections (see Table 3) remain in effect unless nF[1:0]=LL.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit t_U which is of the order of a nanosecond (see Table 2). There are 9 skew configurations available for each output pair. These configurations are choosen by the nF1:0 control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Skew Selection Table (Table 3) shows how to select specific skew taps by using the nF1:0 control pins.

EXTERNAL FEEDBACK

By providing external feedback, the QS599X family gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

Table 2. PLL Programmable Skew Range and Resolution Table

	FS = Low	FS = Mid	FS = High	Comments
Timing unit calculation (t_U)	$1/(44xF_{NOM})$	$1/(26xF_{NOM})$	$1/(16xF_{NOM})$	
VCO Frequency range (F_{NOM})(1,2)	15 to 35MHz	25 to 60MHz	40 to 110MHz	
Skew adjustment range(3) Max adjustment:	±9.09ns ±49°, ±14%	±9.23ns, ±83°, ±23%	±9.38ns, ±135°, ±37%	ns Phase degrees % of cycle time
Example 1, F_{NOM} = 15MHz	t_U = 1.52 ns	—	—	
Example 2, F_{NOM} = 25MHz	t_U = 0.91 ns	t_U = 1.54 ns	—	
Example 3, F_{NOM} = 30MHz	t_U = 0.76 ns	t_U = 1.28 ns	—	
Example 4, F_{NOM} = 40MHz	—	t_U = 0.96 ns	t_U = 1.56 ns	
Example 5, F_{NOM} = 50MHz	—	t_U = 0.77 ns	t_U = 1.25 ns	
Example 6, F_{NOM} = 80MHz	—	—	t_U = 0.78 ns	

Notes:
1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FS value based on input frequency range allows the PLL to operate in its 'sweet spot' where jitter is lowest.
2. The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at 1Q1:0, 2Q1:0, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as the VCO when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $-4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where $\pm 6\,t_U$ skew adjustment is possible and at the lowest F_{NOM} value.

Table 3. Skew Selection Table for Output Pairs

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)(1)
LL(2)	$-4t_U$	Divide by 2	Divide by 2
LM	$-3t_U$	$-6t_U$	$-6t_U$
LH	$-2t_U$	$-4t_U$	$-4t_U$
ML	$-1t_U$	$-2t_U$	$-2t_U$
MM	Zero skew	Zero skew	Zero skew
MH	$1t_U$	$2t_U$	$2t_U$
HL	$2t_U$	$4t_U$	$4t_U$
HM	$3t_U$	$6t_U$	$6t_U$
HH	$4t_U$	Divide by 4	Inverted(3)

Notes:
1. Programmable skew on pair #4 is not applicable for the QS5993.
2. LL disables outputs if TEST=MID and GND/$\overline{sOE}$=HIGH.
3. When pair #4 is set to HH (inverted), GND/$\overline{sOE}$ disables pair #4 HIGH when V_{CCQ}/PE=HIGH, GND/$\overline{sOE}$ disables pair #4 LOW when V_{CCQ}/PE=LOW.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Input Voltage V_I	–0.5V to 7.0V
Maximum Power Dissipation at T_A = 85°C, PLCC	0.80W
QSOP	0.66W
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 5. Recommended Operating Range

Symbol	Descrioption	QS599X-5,-7 (Industrial) Min	QS599X-5,-7 (Industrial) Max	QS599X-2 (Commercial) Min	QS599X-2 (Commercial) Max	Units
V_{CC}	Power Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Ambient Operating Temperature	–40	85	0	70	°C

Table 6. DC Characteristics Over Operating Range

Symbol	Parameter	Test Condition		QS5991/993 Min	QS5991/993 Max	QS5992 Min	QS5992 Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB inputs only)		2.0	—	V_{CC}–1.35	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB inputs only)		—	0.8	—	1.35	V
V_{IHH}	Input HIGH Voltage[1]	3-level inputs only		V_{CC}–1.0	—	V_{CC}–1.0	—	V
V_{IMM}	Input MID Voltage[1]	3-level inputs only		V_{CC}/2–0.5	V_{CC}/2+0.5	V_{CC}/2–0.5	V_{CC}/2+0.5	V
V_{ILL}	Input LOW Voltage[1]	3-level inputs only		—	1.0	—	1.0	V
$\|I_{IN}\|$	Input Leakage Current (REF, FB inputs only)	V_{IN} = V_{CC} or GND V_{CC} = Max		—	5	—	5	µA
$\|I_3\|$	3-level Input DC Current (TEST, FS, *n*F1:0)	V_{IN} = V_{CC}	HIGH level	—	200	—	200	µA
		V_{IN} = V_{CC}/2	MID level	—	50	—	50	
		V_{IN} = GND	LOW level	—	200	—	200	
$\|I_{PU}\|$	Input Pull-up Current (V_{CCQ}/PE)	V_{CC} = Max, V_{IN} = GND		—	100	—	100	µA
$\|I_{PD}\|$	Input Pull-down Current (GND/$\overline{sOE}$)	V_{CC} = Max, V_{IN} = V_{CC}		—	100	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –16mA		2.4	—	—	—	V
		V_{CC} = Min, I_{OH} = –40mA		—	—	V_{CC}–0.75	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 46mA		—	0.45	—	0.45	V
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND		—	–250	—	N/A	mA

Notes:
1. These inputs are normally wired to V_{CC}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. QS5991/QS5993 are to be measured at 25°C with 10:1 duty cycle, one output at a time, and one second maximum. QS5992 outputs are not to be shorted. Guaranteed by characterization but not production tested.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max, TEST=Mid, REF=Low, GND/$\overline{sOE}$ = Low, all outputs unloaded	10	40	mA
ΔI_{CC}	Power Supply Current Per Input HIGH(1)	V_{CC} = Max, V_{IN}=3.4V	0.4	1.5	mA
I_{CCD}	Dynamic Power Supply Current Per Output(1)	V_{CC} = Max, C_L=0pF	100	160	uA/ MHz
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 20MHz, C_L=240pF(2)	43		mA
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 33MHz, C_L=240pF(2)	63		mA
I_C	Total Power Supply Current(1)	V_{CC} = 5.0V, F_{REF} = 66MHz, C_L=240pF(2)	117		mA

Notes:
1. Guaranteed by characterization but not production tested.
2. For 8 outputs each loaded with 30pF.

Table 8. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

	QSOP		PLCC		Units
	Typ	Max	Typ	Max	
C_{IN}	4	6	5	7	pF

Note: Capacitance applies to all inputs except TEST, FS, *n*F1:0. It is characterized but not tested.

Figure 3. AC Test Loads and Waveforms

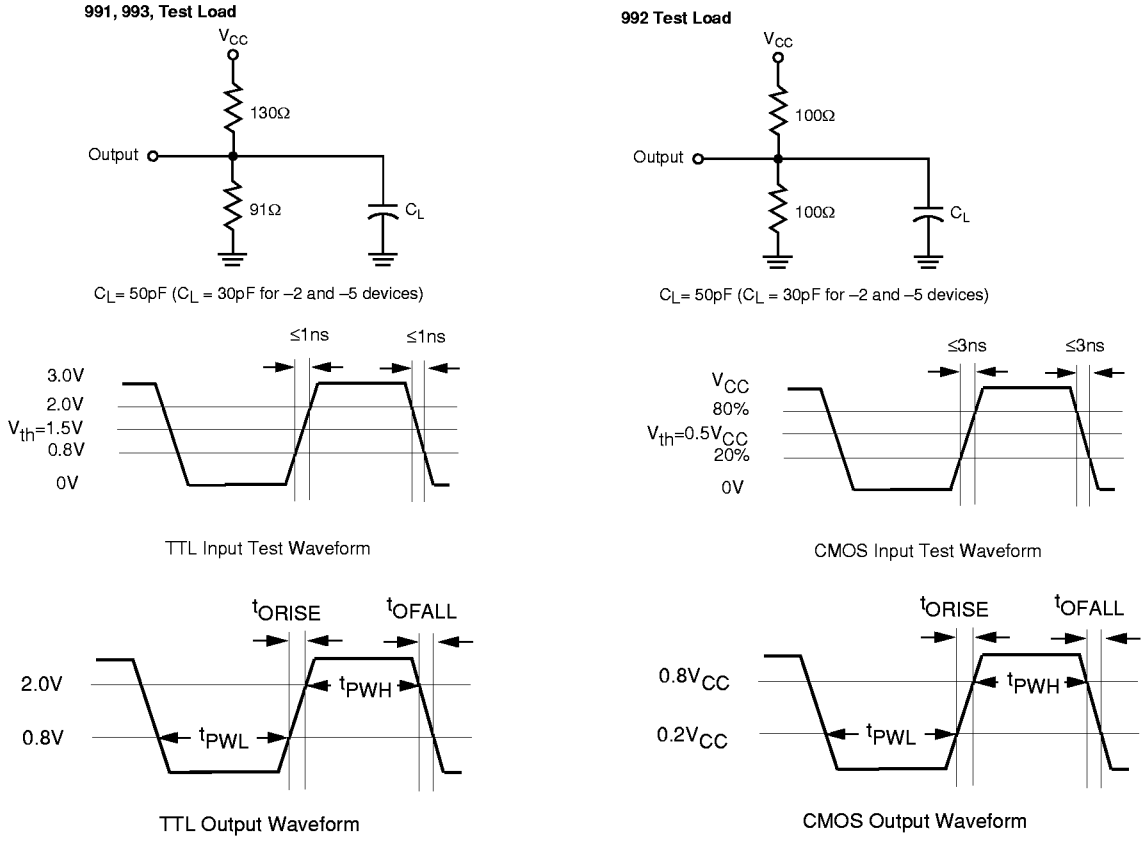


Table 9. Switching Characteristics Over Operating Range

Symbol	Description		QS5991/3-2 Min	QS5991/3-2 Typ	QS5991/3-2 Max	QS5992-2 Min	QS5992-2 Typ	QS5992-2 Max	Unit
F_{NOM}	VCO frequency range		See Table 2						
t_{RPWH}	REF pulse width HIGH(1)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1)		3.0	—	—	3.0	—	—	ns
t_U	Programmable skew time unit		See Table 3						
t_{SKEWPR}	Zero output matched-pair skew (xQ0, xQ1)(1,2,3)		—	0.05	0.20	—	0.05	0.20	ns
t_{SKEW0}	Zero output skew (all outputs) C_L=0pF(1,4)		—	0.1	0.25	—	0.1	0.25	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)(1,5)		—	0.25	0.50	—	0.25	0.50	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)(1,5)		—	0.5	1.2	—	0.5	1.2	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)(1,5)		—	0.25	0.50	—	0.25	0.50	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)(1,2)		—	0.50	0.90	—	0.50	0.90	ns
t_{DEV}	Device-to-device skew(1,2,6)		—	—	0.75	—	—	0.75	ns
t_{PD}	REF input to FB propagation delay(1,8)		–0.25	0	0.25	–0.25	0	0.25	ns
t_{ODCV}	Output duty cycle variation from 50%(1)		–1.2	0	1.2	–1.2	0	1.2	ns
t_{PWH}	Output HIGH time deviation from 50%(1,9)		—	—	2.0	—	—	3.0	ns
t_{PWL}	Output LOW time deviation from 50%(1,10)		—	—	2.5	—	—	3.0	ns
t_{ORISE}	Output rise time(1)		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{OFALL}	Output fall time(1)		0.15	1.0	1.5	0.5	2.0	2.5	ns
t_{LOCK}	PLL lock time(7)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	ps

Notes:

1. All timing tolerances apply for $F_{NOM} \geq 25$MHz. Guaranteed by design and characterization, not subject to 100% production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
4. t_{SKEW0} is the skew between outputs when they are selected for $0t_U$.
5. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
6. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)
7. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
8. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
9. Measured at 2.0V for the QS5991 and QS5993, $0.8V_{CC}$ for the QS5992.
10. Measured at 0.8V for the QS5991 and QS5993, $0.2V_{CC}$ for the QS5992.
11. Refer to Table 10 for more detail.

Table 9. Switching Characteristics Over Operating Range (Cont'd)

Symbol	Description		QS5991/3-5 Min	QS5991/3-5 Typ	QS5991/3-5 Max	QS5992-5 Min	QS5992-5 Typ	QS5992-5 Max	Unit
F_{NOM}	VCO frequency range		See Table 2						
t_{RPWH}	REF pulse width HIGH(1)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1)		3.0	—	—	3.0	—	—	ns
t_U	Programmable skew time unit		See Table 3						
t_{SKEWPR}	Zero output matched-pair skew (xQ0, xQ1)(1,2,3)		—	0.1	0.25	—	0.1	0.25	ns
t_{SKEW0}	Zero output skew (all outputs)(1,4)		—	0.25	0.5	—	0.25	0.5	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)(1,5)		—	0.6	0.7	—	0.6	0.7	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)(1,5)		—	0.5	1.2	—	0.6	1.5	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)(1,5)		—	0.5	0.7	—	0.5	0.7	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)(1,2)		—	0.5	1.0	—	0.6	1.7	ns
t_{DEV}	Device-to-device skew(1,2,6)		—	—	1.25	—	—	1.25	ns
t_{PD}	REF input to FB propagation delay(1,8)		–0.5	0	0.5	–0.5	0	0.5	ns
t_{ODCV}	Output duty cycle variation from 50%(1)		–1.2	0	1.2	–1.2	0	1.2	ns
t_{PWH}	Output HIGH time deviation from 50%(1,9)		—	—	2.5	—	—	4.0	ns
t_{PWL}	Output LOW time deviation from 50%(1,10)		—	—	3.0	—	—	4.0	ns
t_{ORISE}	Output rise time(1)		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{OFALL}	Output fall time(1)		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{LOCK}	PLL lock time(7)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	ps

Notes:

1. All timing tolerances apply for $F_{NOM} \geq 25$MHz. Guaranteed by design and characterization, not subject to 100% production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
4. t_{SKEW0} is the skew between outputs when they are selected for $0t_U$.
5. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
6. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)
7. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
8. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
9. Measured at 2.0V for the QS5991 and QS5993, $0.8V_{CC}$ for the QS5992.
10. Measured at 0.8V for the QS5991 and QS5993, $0.2V_{CC}$ for the QS5992.
11. Refer to Table 10 for more detail.

Table 9. Switching Characteristics Over Operating Range (Cont'd)

Symbol	Description		QS5991/3-7 Min	QS5991/3-7 Typ	QS5991/3-7 Max	QS5992-7 Min	QS5992-7 Typ	QS5992-7 Max	Unit
F_{NOM}	VCO frequency range		See Table 2						
t_{RPWH}	REF pulse width HIGH(1)		3.0	—	—	3.0	—	—	ns
t_{RPWL}	REF pulse width LOW(1)		3.0	—	—	3.0	—	—	ns
t_U	Programmable skew time unit		See Table 3						
t_{SKEWPR}	Zero output matched-pair skew (xQ0, xQ1)(1,2,3)		—	0.1	0.25	—	0.1	0.25	ns
t_{SKEW0}	Zero output skew (all outputs)(1,4)		—	0.3	0.75	—	0.3	0.75	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)(1,5)		—	0.6	1.0	—	0.6	1.0	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)(1,5)		—	0.5	1.5	—	0.5	1.5	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)(1,5)		—	0.7	1.2	—	0.7	1.2	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)(1,2)		—	1.2	1.7	—	1.2	1.7	ns
t_{DEV}	Device-to-device skew(1,2,6)		—	—	1.65	—	—	1.65	ns
t_{PD}	REF input to FB propagation delay(1,8)		–0.7	0	0.7	–0.7	0	0.7	ns
t_{ODCV}	Output duty cycle variation from 50%(1)		–1.2	0	1.2	–1.5	0	1.5	ns
t_{PWH}	Output HIGH time deviation from 50%(1,9)		—	—	3.0	—	—	5.5	ns
t_{PWL}	Output LOW time deviation from 50%(1,10)		—	—	3.5	—	—	5.5	ns
t_{ORISE}	Output rise time(1)		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output fall time(1)		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL lock time(7)		—	—	0.5	—	—	0.5	ms
t_{JR}	Cycle-to-cycle output jitter(1)	RMS	—	—	25	—	—	25	ps
		Peak-to-peak	—	—	200	—	—	200	ps

Notes:

1. All timing tolerances apply for $F_{NOM} \geq 25$MHz. Guaranteed by design and characterization, not subject to 100% production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
4. t_{SKEW0} is the skew between outputs when they are selected for $0t_U$.
5. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
6. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)
7. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
8. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
9. Measured at 2.0V for the QS5991 and QS5993, $0.8V_{CC}$ for the QS5992.
10. Measured at 0.8V for the QS5991 and QS5993, $0.2V_{CC}$ for the QS5992.
11. Refer to Table 10 for more detail.

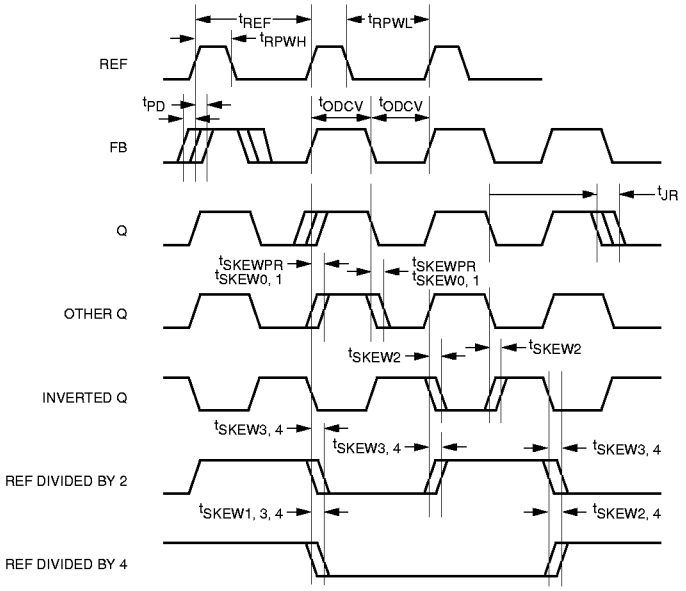
Table 10. Input Timing Requirements

Symbol	Description(1)	Min	Max	Units
t_R, t_F	Maximum input rise and fall times, 0.8V to 2.0V	—	10	ns/V
t_{PWC}	Input clock pulse, high or low	3	—	ns
D_H	Input duty cycle	10	90	%

Note:

1. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

Figure 4. AC Timing Diagram



Notes:

V_{CCQ}/PE: Figure 4 applies to V_{CCQ}/PE=Vcc. For V_{CCQ}/PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50pF (30pF for -2 and -5) and terminated with 50Ω to 2.06V (991/3) or V_{CC}/2 (992).

t_{SKEWPR}: The skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.

t_{SKEW0}: The skew between outputs when they are selected for $0t_U$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

t_{PWH} is measured at 2.0V for the 991/3 and $0.8V_{CC}$ for 992.

t_{PWL} is measured at 0.8V for the 991/3 and $0.2V_{CC}$ for 992.

t_{ORISE} and t_{OFALL} are measured between 0.8V and 2.0V for 991/3 and $0.2V_{CC}$ and $0.8V_{CC}$ for 992.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.